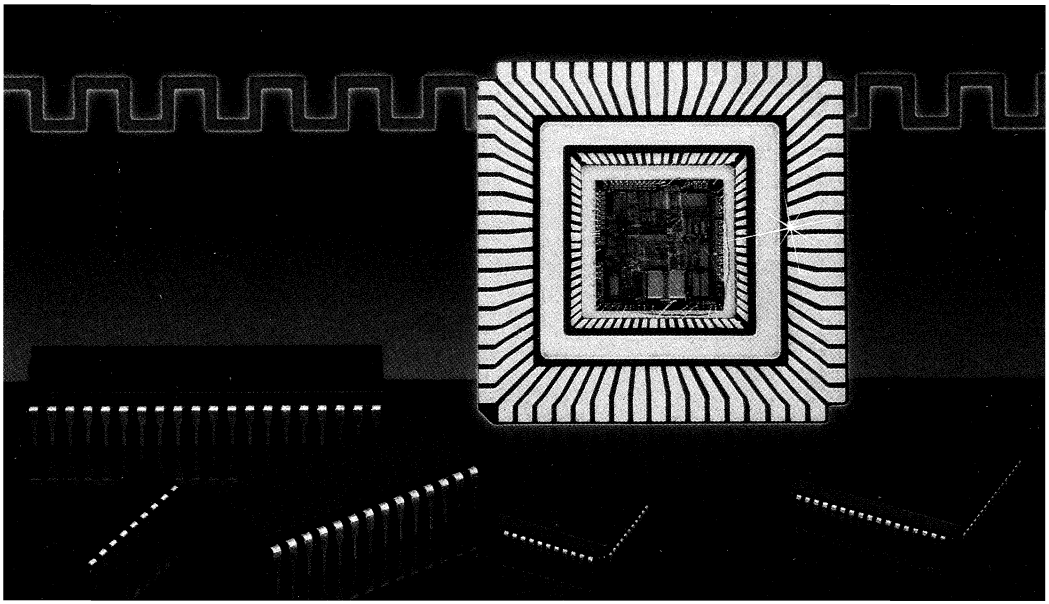
SIEMENS



PC Peripherals
System Components

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SIEMENS

Microcomputer Components

PC-Peripherals
System Components

Data Catalog 1990

Edition 10.90

Published by Siemens AG, Bereich Halbleiter, Marketing-Kommunikation Balanstraße 73, D-8000 München 80.

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8-/16-Bit Microprocessors

SAB 8085AH	8-bit Microprocessor (3 MHz, 5 MHz)
SAB 8086	16-bit Microprocessor (5 MHz, 8 MHz, 10 MHz)
SAB 8088	8-bit Microprocessor (5 MHz, 8 MHz, 10 MHz)
SAB 80186	High-Integration 16-bit Microprocessor (8 MHz, 10 MHz)
SAB 80188	High-Integration 8-bit Microprocessor (8 MHz, 10 MHz)
SAB 80286	High-Performance 16-bit Microprocessor with Memory Management and Protection (8 MHz, 10 MHz or 12.5 MHz)

32-Bit Microprocessors

SAB-R2000A	High-Performance 32-bit RISC Microprocessor
SAB-R2010A	High-Performance Floating-Point Coprocessor
SAB-R3000	High-Performance 32-bit RISC Microprocessor
SAB-R3010	High-Performance Floating-Point Coprocessor

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SAB-R3020/SAB-R2020	Write Buffer

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SAB 82284	Clock Generator for SAB 80286 Processor Family
SAB 82288	Bus Controller for SAB 80286 Processor Family
SAB 82289	Bus Arbiter for SAB 80286 Processor Family
SAB 82C250/SAB 82C251	Advanced Peripheral Interface Controller
SAB 8282A/8283A	Octal Latch
SAB 8284B/SAB 8284B-1	Clock Generator and Driver for SAB 8086 Processor Family
SAB 8286A/8287A	Octal Bus Transceiver
SAB 8288A	Bus Controller for SAB 8086 Processor Family
SAB 8289	Bus Arbiter for SAB 8086/8088 Processor Family

Memory Components

HYB 41256-10/-12/-15	256K × 1-bit Dynamic RAM
HYB 514256B-60/-70/-80 HYB 514256BL-60/-70	256K × 4-bit Dynamic RAM
HYB 51100B -60/-70/-80 HYB 51100BL-60/-70	1M × 1-bit Dynamic RAM
HYB 514100 -80/-10	4M × 1-bit Dynamic RAM
HYB 514400 -80/-10	1M × 4-bit Dynamic RAM

Memory Modules

HYM 39500S -80	256K × 9-bit Dynamic RAM Modul
HYM 91000S -60/-70 HYM 91000L-60/-70/-80 HYM 91000SL-60/-70 HYM 91000LL-60/-70/-80	1M × 9-bit Dynamic RAM Modul
HYM 94000S -80/-10	4M × 9-bit Dynamic RAM Modul
HYM 362500S-80	256K × 36-bit Dynamic RAM Module
HYM 365120S-80	512K × 36-bit Dynamic RAM Module
HYM 361020S-80/-10	1M × 36-bit Dynamic RAM Module
HYM 362020S-80/-10	2M × 36-bit Dynamic RAM Module

General Information

General Information

Type designation code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15, edition 1985, available at:

Pro Electron, Avenue Louise, 430 (B. 12)
B-1060 Brussels, Belgium

Mounting instructions

Plastic Package

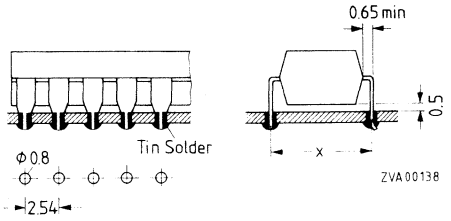
The 90° pins fit into holes with a diameter of 0.7 to 0.9 mm, spaced 2.54 mm apart. See spacing x in figure 1.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see figure 1)**.

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for hand soldering and 260 °C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Dimensions in mm

Plastic packages (SO and PLCC) for surface mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s
Wave soldering: (pins and package are dipped into the tin bath)	soldering temperature 260 °C, max. soldering time 8 s

Storage, pretreatment before processing

The components are to be stored in a dry environment. When solder methods causing solder heat shock stresses are used (reflow soldering where the component is dipped into the solder bath, vapor-phase soldering) it is recommendable to subject IC's in plastic packages to a 24-hour drying phase at 125 °C.

Other points to note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When the pins are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances should the components be removed or inserted while the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

Processing guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (**ESS**) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (**ESD**).

Of the multiple of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resistive discharges it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
Means which are effective here are an increase in relative humidity to ≥ 60 % and the replacement of highly charging plastics by antistatic materials.

b) With every king of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^8\ \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer:

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to $10^9\ \Omega$/cm.
3. With humidity of > 50 % a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 Ω.
4. If conductive floors, $R = 5 \times 10^4$ to $10^7\ \Omega$ are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to $10^7\ \Omega$).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to $10^8\ \Omega$.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

Example 1) Conductive (black) tubes.
The devices may be destroyed in the tube by charged persons or come out of the tube charged if this in emptied by a charged person.
Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

Example 2) Anti-static (transparent) tubes.
The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins).
The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx 10^6$ to $10^8\ \Omega$/cm) between the tube and the machine.

The use of metal tubes – especially of anodized aluminum – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. Thestorage temperature should not exceed 60 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are likewise unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6\ \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming inspection

In incoming inspection the above guidelines should be observed. Otherwise any right for refund or replacement if devices fail inspection may be lost.

Material and mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control cannot be used. Siemens EMI-suppression capacitors of the type B 81711-B31 ... -B36 have propen very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting ring.
2. Test sockets must not be conducting any voltage when individual devices or assembled circuit boards and inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

Packing of assembled PC boards or flatpack units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases - especially with humidity of > 40 % - this requirement is fulfilled using simple currugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

It must always be ensured that boards do not touch.

In special cases it may be necessary to provide potection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping of our devices, are available from Laber of Munich.

Ultrasonic cleaning of ICs

In incoming inspection the above guidelines should be observed. Otherwise any right for refund or replacement if devices fail inspection may be lost.

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	f > 40 kHz
exposure	t > 2 min
alternating sound pressure	p > 0.29 bar
sound power	N > 0.5 W/cm²/liter

Data classification

Maximum ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at T_A = 25 °C and for the given supply voltage.

Operating range

In the operating range the functions given in the circuit description will be fulfilled.

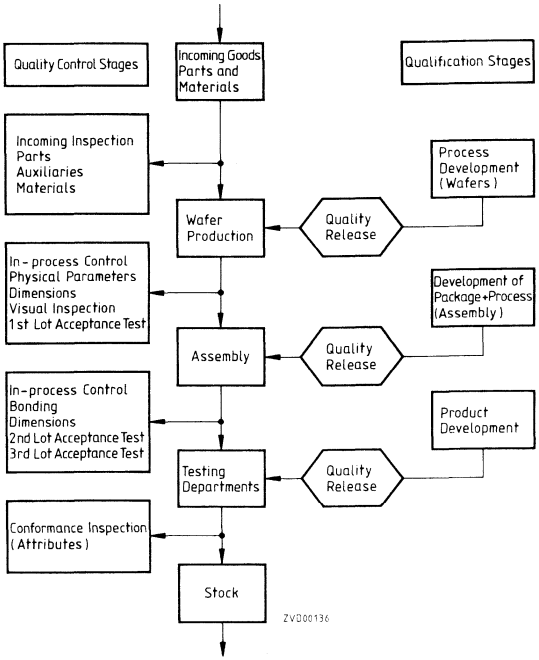
Quality assurance system

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure "Siemens Quality Assurance System - Integrated Circuits" (SQS-IC).

Figure 4 shows the most important stages of the "SQS-IC". A quality assurance (QA) department which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

Figure 4



The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with hundreds of thousands of ICs in 1985. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Inoperatives AOQ (DPM)	**Sum of electrical defectives AOQ (DPM)**	**Sum of mechanical defectives AOQ (DPM)**
SSI/MSI ≤ 1000 gate functions	40	200	100
LSI/MSI ≤ 1000 gate functions	120	400	200

Reliability

Measures taken during development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

In-process control during production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

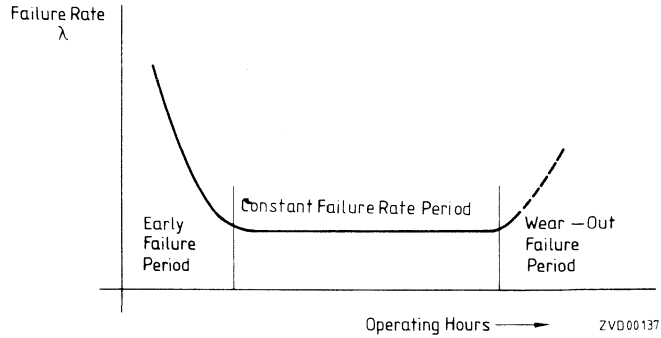
The decreasing failure rates reflect the never ending effort in this direction; they have been reduced considerably despite an immense rise in the IC's complexity.

So in 1985 the typical random failure rates estimated for accelerated life tests with almost 2 million ICs of all complexities are found to be around 80 fit.

Reliability monitoring

The general course of the ICsfailurerateversustimeis'shown by a so-called "bathtub" curve (**figure 5**). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Figure 5



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp \frac{E_A}{k}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of T_A = 40 °C, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line - this is described in the brochure "SQS-IC". Such tests are e.g. humidity test at 85 °C and 85 % relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

Summary of Types (incl. ordering codes)

Summary of Types

Type	Ordering Code	Package	Description	Page
PC-Peripheral Components				
SAB 82C171-35-P	Q67120-P289	P-DIP-28	CMOS Color Palette, 35 MHz	
SAB 82C171-50-C	Q67120-P305	C-DIP-28	CMOS Color Palette, 50 MHz	
SAB 82C171-50-P	Q67120-P306	P-DIP-28	CMOS Color Palette, 50 MHz	
SAB 82C176-40-P	Q67120-P308	P-DIP-28	CMOS Color Palette, 40 MHz	
SAB 82C176-50-P	Q67120-P309	P-DIP-28	CMOS Color Palette, 50 MHz	
SAB 82C206-N	Q67120-P286	PL-CC-84	Integrated Peripheral Controller	
SAB 82C211-12-N	Q67120-P291	PL-CC-84 SMD	CPU/Bus Controller for Siemens PC-AT Chipset, 12 MHz	
SAB 82C211-16-N	Q67120-P292	PL-CC-84 SMD	PU/Bus Controller for Siemens PC-AT Chipset, 16 MHz	
SAB 82C212-12-N	Q67120-P294	PL-CC-84 SMD	Page/Interleaved Memory Controller for Siemens PC-AT Chipset, 12 MHz	
SAB 82C212-16-N	Q67120-P295	PL-CC-84 SMD	Page/Interleaved Memory Controller for Siemens PC-AT Chipset, 16 MHz	
SAB 82C215-12-N	Q67120-P297	PL-CC-84 SMD	Data/Address Buffer of Siemens PC-AT Chipset, 12 MHz	
SAB 82C215-16-N	Q67120-P298	PL-CC-84 SMD	Data/Address Buffer of Siemens PC-AT Chipset, 16 MHz	

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
System Components				
SAB 16C450-N	Q67120-P285	PL-CC-44	Programmable Communication Interface	
SAB 16C450-P	Q67120-P284	P-DIP-40	Programmable Communication Interface	
SAB 16C550A-N	Q67120-P318	PL-CC-44	Programmable Communication Interface with FIFOs	
SAB 16C550A-P	Q67120-P319	P-DIP-40	Programmable Communication Interface with FIFOs	
SAB 7201A-P	Q67120-P143	P-DIP-40	Multi-Protocol Serial Communication Controller, MPSC	
SAB 8155-2-C	Q67120-Q85	C-DIP-40	RAM, stat., with I/O Ports and Timer, Access Time 400 ns	
SAB 8155-2-P	Q67120-Q86	P-DIP-40	RAM, stat., with I/O Ports and Timer, Access Time 300 ns	
SAB 8155-C	Q67120-Q43	C-DIP-40	RAM, stat., with I/O Ports and Timer, Access Time 400 ns	
SAB 8155-P	Q67120-Q42	P-DIP-40	RAM, stat., with I/O Ports and Timer, Access Time 300 ns	
SAB 82257-6-N	Q67120-P179	PL-CC-68	High-Performance DMA Controller, 6 MHz	
SAB 82257-N	Q67120-P176	PL-CC-68	High-Performance DMA Controller, 8 MHz	
SAB 82258A-1-A	Q67120-P247	C-PGA-68	Advanced DMA Controller, 10 MHz	
SAB 82258A-1-N	Q67120-P245	PL-CC-68	Advanced DMA Controller, 10 MHz	
SAB 82258A-1-R	Q67120-P249	C-CC-68	Advanced DMA Controller, 10 MHz	
SAB 82258A-A	Q67120-P248	C-PGA-68	Advanced DMA Controller, 8 MHz	
SAB 82258A-N	Q67120-P246	PL-CC-68	Advanced DMA Controller, 8 MHz	
SAB 82258A-R	Q67120-P250	C-CC-68	Advanced DMA Controller, 8 MHz	

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
System Components (cont'd)				
SAB 8237A-P	Q67120-Y49	P-DIP-40	Programmable DMA Controller, 3 MHz	
SAB 8237P-5-P	Q67120-Y72	P-DIP-40	Programmable DMA Controller, 5 MHz	
SAB 82511-1-N	Q67120-P55	PL-CC-44	Token Bus Modem	
SAB 82511-1-NE	Q67120-P58	PL-CC-68	Token Bus Modem	
SAB 82511-5-N	Q67120-P51	PL-CC-44	Token Bus Modem	
SAB 82511-5-NE	Q67120-P57	PL-CC-68	Token Bus Modem	
SAB 82556-N	Q67120P287	PL-CC-68	Universal System Interface Controller	
SAB 8256A-2-P	Q67120-Y59	P-DIP-40	Programmable Multifunction UART,5 MHz System Clock	
SAB 8256A-P	Q67120-Y43	P-DIP-40	Programmable Multifunction UART,3 MHz System Clock	
SAB 8259A	Q67120-P46	P-DIP-28	Programmable Interrupt Controller, 5 MHz	
SAB 8259A-2P	Q67120-P81	P-DIP-28	Programmable Interrupt Controller, 8 MHz	
SAB 82C258A-1-N	Q67120-P312	PL-CC-68	Advanced DMA Controller, 10 MHz	
SAB 82C258A-12-N	Q67120-P313	PL-CC-68	Advanced DMA Controller, 12.5 MHz	
SAB 82C258A-16-N	Q67120-P314	PL-CC-68	Advanced DMA Controller, 16 MHz	
SAB 82C258A-20-N	Q67120-P323	PL-CC-68	Advanced DMA Controller, 20 MHz	

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
System Components (cont'd)				
SAB 82C37A-5-P	Q67120-P215	P-DIP-40	Programmable DMA Controller, 5 MHz	
SAB 82C37A-8-P	Q67120-P239	P-DIP-40	Programmable DMA Controller, 8 MHz	
SAB 82C37B-5-P	Q67120-P243	P-DIP-40	Programmable DMA Controller, 5 MHz	
SAB 82C37B-8-P	Q67120-P244	P-DIP-40	Programmable DMA Controller, 8 MHz	
SAB 82C50-N	Q67120-P283	PL-CC-44	Programmable Communication Interface	
SAB 82C50-P	Q67120-P282	P-DIP-40	Programmable Communication Interface	
SAB 82C51A-P	Q67120-P216	P-DIP-28	Programmable Communications Interface	
SAB 82C53-5-P	Q67120-P264	P-DIP-24	Programmable CMOS Interval Timer, Command Width 300 ns	
SAB 82C53-P	Q67120-P217	P-DIP-24	Programmable CMOS Interval Timer, Command Width 400 ns	
SAB 82C54-2-P	Q67120-P253	P-DIP-24	Programmable CMOS Interval Timer, 10 MHz	
SAB 82C54-P	Q67120-P212	P-DIP-24	Programmable CMOS Interval Timer, 8 MHz	
SAB 82C551-N	Q67120-P321	PL-CC-68 (SMD)	Advanced Peripheral Interface Controller with FIFOs	
SAB 82C552-N	Q67120-P322	PL-CC-68 (SMD)	Advanced Peripheral Interface Controller with FIFOs	
SAB 82C55A-2-P	Q67120-P213	P-DIP-40	Programmable Peripheral Interface	
SAB 82C59A-2-P	Q67120-P238	P-DIP-28	Programmable Interrupt Controller, 8 MHz	

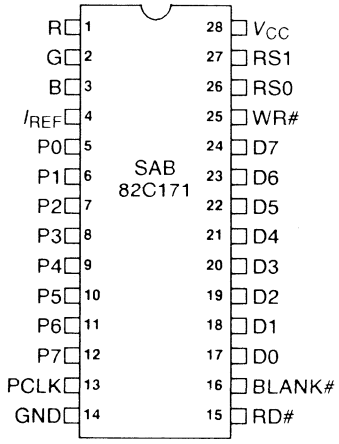
PC-Peripherals

SAB 82C171
CMOS Color Palette

Advance Information

- 50 MHz maximum pixel rate
- 256 colors out of 262144 possible colors
- Monolithic CMOS
- Three 6-bit DACs
- Analog RGB composite blank output to drive directly into doubly terminated 75 Ω cable
- Compatible with RS343A / RS170A video standard
- Pixel address input mask function
- Read back of lookup table and register contents
- 28-pin plastic dual-in-line package, P-DIP-28 (600 mil)
- Single 5V power supply
- Fully pin and function compatible with industry standard color palette for VGA and MCGA systems

Pin Configuration



Pin Names

D0 - D7	Data Bus
RD#	Read
WR#	Write
RS0, RS1	Register Select
P0 - P7	Pixel Address
R, G, B	Red, Green, Blue
I_{REF}	Reference Current
BLANK#	Blanking
PCLK	Pixel Clock
V_{CC}	Power Supply (+ 5V)
GND	Ground (0V)

The SAB 82C171 is a monolithic CMOS color palette including a color lookup table and a digital to analog converter. The analog outputs are designed to drive an analog 75 Ω doubly terminated input of a RS170A or RS343A standard monitor (37.5 Ω load).

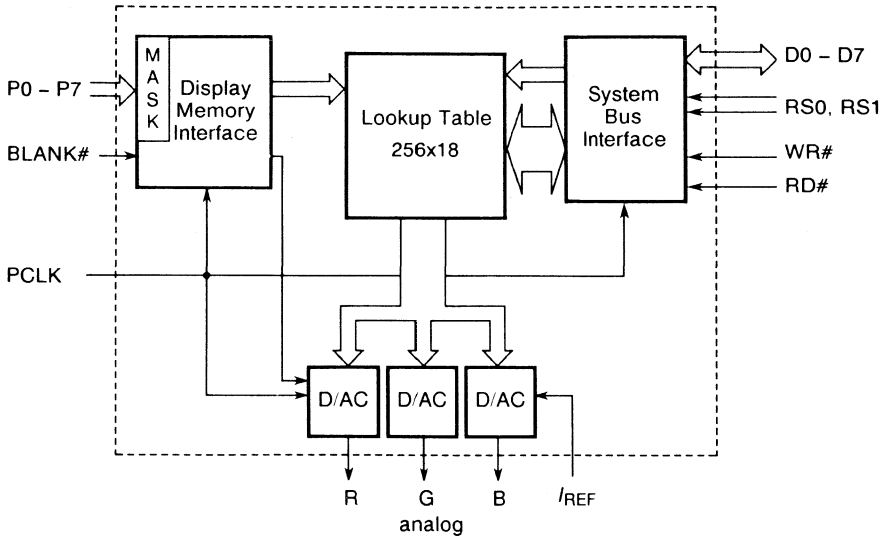
The SAB 82C171 is used in graphics systems working with up to 256 colors, which may independently be taken from a total of 262144 colors.

The SAB 82C171 is pin and functional compatible to the industry standard color palette for VGA and MCGA systems.

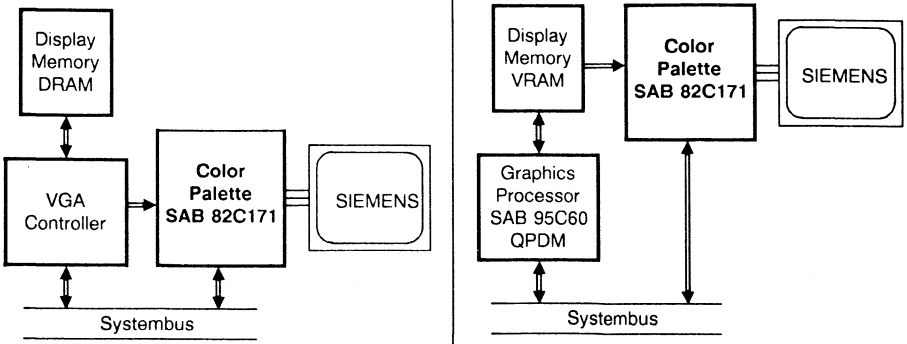
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
PCLK	13	I	**Pixel Clock** provides the video timing control of the SAB 82C171 through the three pipeline stages from pixel address and blank inputs to the three analog outputs.
P0-P7	5-12	I	**Pixel Address** value ANDed with the pixel mask register is used as direct address to the color lookup table (these inputs are sampled with the rising edge of PCLK).
BLANK#	16	I	**BLANK** input (active low) forces the DACs of the SAB 82C171 to the value zero, delayed by 3 clocks according to the pipeline (this input is sampled with the rising edge of PCLK).
R, G, B	1, 2, 3	O	**Red, Green, Blue** Analog outputs of the three 6-bit DACs to drive a doubly terminated 75 Ω input of a RS343A or RS170A standard monitor.
I_{REF}	4	I	**Current Reference** Reference analog input for the DACs reference current, is drawn from V_{CC}.
D0-D7	17-24	I/O	**Databus** (bidirectional) The SAB 82C171 color palette is programmed via this 8-bit data bus.
RS0, RS1	26, 27	I	**Register Select** These pins select the register to be accessed during a system bus read or write cycle.
WR#	25	I	**Write#** A active low value on this pin performs a write access of the register, selected by RS0, RS1.
RD#	15	I	**Read#** A active low value on this pin performs a read access of the register, selected by RS0, RS1.
V_{CC}	28	-	**Power supply** (+ 5V)
GND	14	-	**Ground** (0V)

Block Diagram



Two Typical Applications



Functional Description

General

The SAB 82C171 color palette is a device designed for use as the output stage of raster scan video systems. It contains a high speed lookup table (RAM) of 256 x 18-bit, three 6-bit DACs, a systembus interface and a display memory interface including a pixel word mask.

Typically the color palette is placed between the monitor and the display controller with its display memory.

Pixel rates of up to 50 MHz are achieved by pipelining the memory access over three clock periods.

Video Path

The video path is the path, where the pixel information is brought through the color palette from the display memory interface via the lookup table to the analog outputs. The video path is designed for a very high throughput.

An 8-bit value, written to the pixel address input of the display memory interface, is used by the palette as a read address for the lookup table.

On the rising edge of pixel clock the pixel address and BLANK inputs are sampled, after three further rising edges of pixel clock the relevant analog outputs appear.

The color palette includes a pixel word mask, which is controlled via the systembus and is used for masking the pixel address inputs of the display memory interface.

Each location of the lookup table, addressed by the pixel address inputs, contains an 18-bit word. Partitioned into three 6-bit words, the 18-bit data coming out of the lookup table is converted by three 6-bit DACs. The resulting three analog signals, red, green and blue, directly drive the R, G, B output for a RS 170A / RS 343A standard color or monochrome monitor.

The analog outputs of the DACs are designed for driving a doubly terminated 75 Ω cable. Due to this the effective analog output load ($R_{EFFECTIVE}$) is 37.5 Ω. With an I_{REF} of 8.88 mA the DACs are capable of producing an amplitude of 0.7 volts for peak white.

The BLANK signal input acts on all three of the analog outputs driving them to 0V when active. An internal delay on the BLANK signal is used to correct the relationship of the BLANK signal and the pipelined pixel stream at the analog outputs.

The corresponding I_{REF} for various peak white voltages and effective output loading combinations may be calculated according to the following expression:

$$I_{REF} = \frac{V_{PEAK\ WHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note
For all values of I_{REF} and output loading: $V_{BLACK\ LEVEL}$ = 0 volts

Systembus Interface

The system bus interface is used for initialization and controlling the device. It contains an 8-bit bidirectional databus, two register select lines, a read line and a write line.

With the falling edge of the read or write signal the register select input is latched and decoded for selecting a register, with the rising edge data is transferred.

An internal synchronizing circuit enables access the lookup table asynchronous to the video path without any visable shnow effect on the screen.

Register Description

The list below shows the three systembus interface registers of the SAB 82C171 and the four register addresses through which they can be accessed. All registers are able to perform read and write accesses.

RS1	RS0	Register Name
0	0	Pixel address (preparing a color value write access)
1	1	Pixel address (preparing a color value read access)
0	1	Color value
1	0	Pixel mask

Pixel Address Register

There is a single pixel address register within the SAB 82C171. It is used for addressing the lookup table for read and write accesses by the systembus interface.

A write to the pixel address register via register select 00 is preparing a write access to the color-value-register (see"Writing to the lookup table").
A write to the pixel address register via register select 11 is preparing a read access from the color-value register (see"Reading from the lookup table").

The contents of the pixel address register can be read from both, register select 00 and 11.

Color Value Register

This 18-bit wide register is used as a buffer between the systembus and the lookup table. An 18-bit value can be written to or read from this register in three sequential accesses of 6-bit for each color. The sequence is: red-green-blue. The 6-bit value is transferred via the pins D0 - D5 of the systembus interface. Pins D6 and D7 are not used in write operations and are set to logical zero at read cycles.

Pixel Mask Register

The pixel mask register is accessed via the systembus and is independent of the color value and the pixel address register. The pixel address inputs of the video path are-bitwise ANDed with the contents of the pixel mask register. In other words the logical value of a pin of the pixel address input is ignored and driven to "0" if the equivalent bit in the mask register is "0".

There are two ways of writing to the pixel mask register: synchronously to the pixel clock and asynchronously to the pixel clock.

If writing to the pixel mask register is done asynchronously to the pixel clock, there is a possibility that the contents of the lookup table are corrupted at the addressed locations. Such a corruption does not matter if the pixel mask register is only written before loading the lookup table as it is done in VGA and MCGA systems. In this case the pixel mask can be used to ignore unused pixel address inputs.

If writing to the pixel mask register is done synchronously to the pixel clock, as shown in the AC characteristics, the contents of the lookup table are never corrupted. The synchronization is only necessary if the mask register is changed after loading the lookup table, for example, if the mask register is used to create blinking or flashing objects (not in VGA and MCGA systems).

Accessing the Lookup Table

The color palette SAB 82C171 is designed for fast access to the lookup table via the system bus interface. Therefore it can be set into two different modes: read mode for lookup table read access and write mode for lookup table write access. The modes are set and changed by writing into the pixel address register: for setting read mode the pixel address register is written via register select 11 and for setting write mode the pixel address register is written via register select 00.

Whenever the pixel address register is updated any unfinished color value read or write sequence is aborted and a new one may begin.

Writing to the Lookup Table

To set a new color definition, a value specifying a location in the color lookup table is first written to the pixel address register (register select 00). By this the color palette is set into write mode and automatically performs the following operation:

1. Specifying of an address within the lookup table.
2. Initializing of the color value register.

The values for the red, green and blue intensities are then written sequentially to the color value register (register select 01). After the blue data is written to the color value register the new color definition is transferred to the color lookup table and the pixel address register is automatically incremented pointing to the next location.

Due to this increment mechanism, it is simple to write a set of consecutive locations with new color definitions. First the start address of the set is written to the pixel address register. Then the color values for each location are written sequentially to the color value register.

Reading from the Lookup Table

In order to read a color definition a value specifying the location in the lookup table to be read is written to the pixel address register (register select 11). By this the color palette is set into read mode and automatically performs the following operation:

1. Addressing one 18-bit word of the lookup table.
2. Loading the color value register with the contents of that word.
3. Increment of the address from operation 1.

The red, green and blue intensity values then can be read by a sequence of three reads from the color value register (register select 01). After the blue value has been read, the location in the lookup table, currently specified by the pixel address register, is copied to the color value register and the pixel address register is again incremented automatically.

Thus a set of color definitions in consecutive locations can be read simply by writing the start address of the set to the pixel address register and then sequentially reading the color values for each location in the set.

Due to the increment mechanism, during each read access of the color value register containing the value of location 'n', the pixel address register contains the value 'n + 1'.

Asynchronous Lookup Table Access

The pixel address and color value registers may be accessed totally asynchronous to the high speed timing of the pixel stream being processed by the SAB 82C171. Data transfers between the lookup table and the color value register are internally synchronized to the pixel clock in the period between microprocessor interface accesses. Due to this logic , various minimum periods are specified between systembus interface accesses, to allow for the appropriate transfers to take place.

Reading from the Pixel Address Register

There is no difference from a read from address 1.1 to a read from address 0.0. In both ways the actual contents of the pixel address register are put out to the systembus interface. The contents of the pixel address register are not changed by this operation. But if a value 'n 'was written by register select 11 to the pixel address register, in a following read access the value 'n + 1' is put out, due to the increment.

Absolute Maximum Ratings

Voltage on V_{CC}	7.0 V
Voltage on any other pin	V_{SS} – 1.0 V to V_{CC} + 0.5 V
Temperature under bias	– 45 to 85 °C
Storage temperature (ambient)	– 65 to 150 °C
Power dissipation	1W
Reference current	–15 mA
Analog output current (per output)	45 mA
DC digital output current	25 mA

Note: *Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

DC Operating Conditions

Parameter	Symbol	Limit values			Unit
		min.	typ.	max.	
Positive supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	–	0	–	V
Input logic "1"voltage	V_{IH}	2.0	–	V_{CC} + 0.5	V
Input logic "0"voltage	V_{IL}	-0.5	–	0.8	V
Ambient operating temperature	T_A	0	–	70	°C
Reference current	I_{REF}	-7.0	–	–10	mA

DC Characteristics

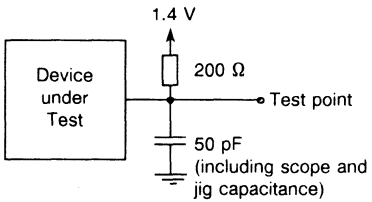
Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Average power supply current	I_{CC}	–	160	mA	SAB 82C171-50 1)
Average power supply current	I_{CC}	–	150	mA	SAB 82C171-35 1)
Voltage at I_{REF} input (pin 4)	V_{REF}	V_{CC} – 3	V_{CC}	V	$V_{SS} \leq V_{IN} \leq V_{CC}$
Digital input current (any input)	I_{IN}	–	± 10	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Off state digital output current	I_{OZ}	–	± 50	µA	–
Output logic "1"	V_{OH}	2.4	–	V	I_{OUT} = – 5mA
Output logic "0"	V_{OL}	–	0.4	V	I_{OUT} = 5mA
Digital input capacitance	C_{IN}	–	7	pF	2)
Digital output capacitance	C_{OUT}	–	7	pF	2) 3)

Notes see next page.

DAC Characteristics 4) 5)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Resolution		6	–	bits	–
Maximum output voltage	V_{OUT} (max)	1.5	–	V	$I_{OUT} \leq 10mA$
Maximum output current	I_{OUT}	21	–	mA	$V_{OUT} \leq 1V$
Full scale error		–	±5	%	6)
DAC to DAC correlation		±2	–	%	7)
Integral linearity		±0.5	–	LSB	8)
Rise time(10% to 90%)		–	8	ns	9)
Full scale settling time		–	20	ns	SAB 82C171-50, 9) 2) 10)
Full scale settling time		–	28	ns	SAB 82C171-35, 9) 2) 10)
Glitch energy		–	200	pVsec	9) 2)
Analog Output Capacitance	C_{AOUT}	–	10	pF	2) 11)

Test load for digital outputs



AC Test Conditions

Input pulse levels	V_{SS} to 3 V
Typical input rise and fall times (10 to 90%)	3 ns
Digital input timing reference level	1.5 V
Digital output timing reference level	0.8 and 2.4 V

Notes

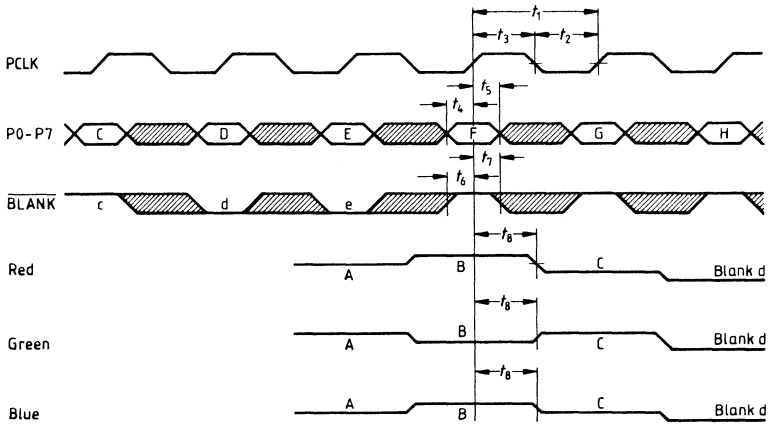
1) I_{CC} is dependent on digital output loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated pixel clock frequency. $I_{OUT} \eqsim I_{OUT}$ (max.).
2) This parameter is sampled, not 100% tested.
3) Voltage on READ# pin $\geq V_{IH}$ (min.) to disable D0 – D7).
4) Tested with $I_{REF} = -8.88$ mA.
5) To assure the quality of the DACs, the power supply and I_{REF} must be absolutly constant.
6) Full scale error from the value predicted by the design equations.
7) About the mid point of the distribution of the three DACs measured at full scale deflection
8) Linearity measured from the least squares best fit line through the DAC characteristics. Monotonicity guaranteed.
9) Load = 37.5 Ω + 30 pF.
10) From a 2% change in the output voltage until settling to within 2% of the final value.
11) Voltage on BLANK# $\leq V_{IL}$(max) to disable R, G, B output.

AC Characteristics

Video Path

Parameter	Symbol	SAB 82C171-35		SAB 82C171-50		Unit	Test condition
		min.	max.	min.	max.		
PCLK Period	t_1	28	10000	20	10000	ns	
PCLK jitter	Δt_1	–	±2.5	–	±2.5	%	
PCLK width low	t_2	9	10000	6	10000	ns	
PCLK width high	t_3	7	10000	6	10000	ns	
Pixel word setup time	t_4	5	–	4	–	ns	1)
Pixel word hold time	t_5	5	–	4	–	ns	1)
BLANK setup time	t_6	5	–	4	–	ns	
BLANK hold time	t_7	5	–	4	–	ns	
PCLK to valid DAC output	t_8	5	30	5	30	ns	2)
Differential output delay between the analog outputs of the same device	Δt_8	–	2	–	2	ns	
PCLK transition time	–	–	50	–	50	ns	

Video Path



1) The pixel address input has to be setup as a valid logic level with the appropriate setup and hold times to each rising edge of the PCLK (this requirement includes the blanking period).

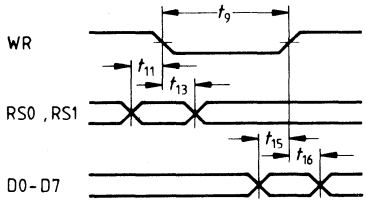
2) A valid analog output is defined as when the changing analog signal is 50% between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions

AC Characteristics (continued)

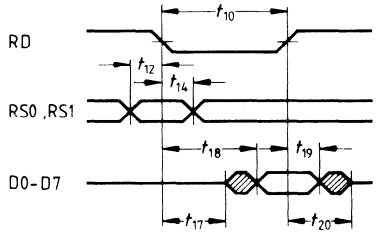
Parameter	Symbol	SAB 82C171-35		SAB 82C171-50		Unit	Test condition
		min.	max.	min.	max.		
Systembus Interface							
WR# pulse width low	t_9	50	–	50	–	ns	
RD# pulse width low	t_{10}	50	–	50	–	ns	
Register select setup time to WR# low	t_{11}	15	–	10	–	ns	
Register select setup time to RD# low	t_{12}	15	–	10	–	ns	
Register select hold time to WR# low	t_{13}	15	–	10	–	ns	
Register select hold time to RD# low	t_{14}	15	–	10	–	ns	
Write data setup time	t_{15}	15	–	10	–	ns	
Write data hold time	t_{16}	15	–	10	–	ns	
Output turn-on delay	t_{17}	5	–	5	–	ns	
Read enable access time	t_{18}		40		40	ns	
Output hold time	t_{19}	5	–	5	–	ns	
Output turn-off delay	t_{20}		20		20	ns	1)
Successive write interval	t_{21}	$3 * t_1$	–	$3 * t_1$	–	ns	
Write followed by read interval	t_{22}	$3 * t_1$	–	$3 * t_1$	–	ns	2)
Successive read interval	t_{23}	$3 * t_1$	–	$3 * t_1$	–	ns	3)
Read followed by write interval	t_{24}	$3 * t_1$	–	$3 * t_1$	–	ns	4)
Write after color write	t_{25}	$3 * t_1$	–	$3 * t_1$	–	ns	
Read after color write	t_{26}	$3 * t_1$	–	$3 * t_1$	–	ns	
Read after read blue color value	t_{27}	$6 * t_1$	–	$6 * t_1$	–	ns	
Write after read blue color value	t_{28}	$6 * t_1$	–	$6 * t_1$	–	ns	
Read after read-address write	t_{29}	$6 * t_1$	–	$6 * t_1$	–	ns	
Write/Read enable transition time	–	–	50	–	50	ns	
WR# low to next PCLK high	t_{30}	12	t_1	12	t_1	ns	5)
Data setup time to WR# low	t_{31}	15		15		ns	5)

1) Measured ±200 mV from steady state output voltage
2) Except after writing to pixel address register with RS = 1,1 (see t_{29})
3) Except after writing blue color value (see t_{27})
4) Except after reading blue color value (see t_{28})
5) These values are only important, if the pixel mask register write has to be synchronized to the pixel clock

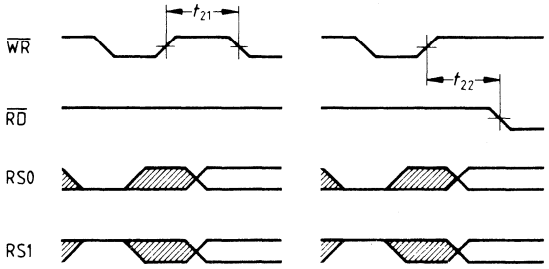
Basic Write Cycle



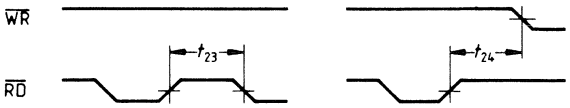
Basic Read Cycle



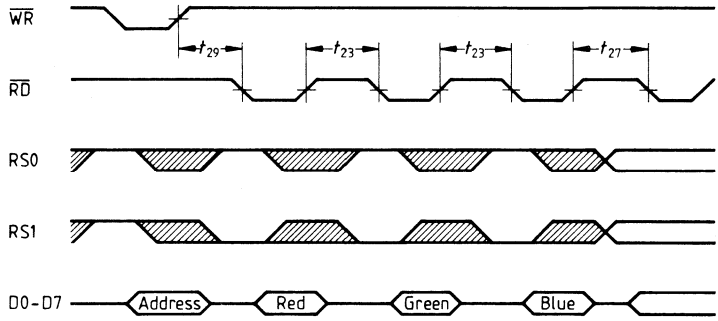
Write to Pixel Mask Register Followed by any Access



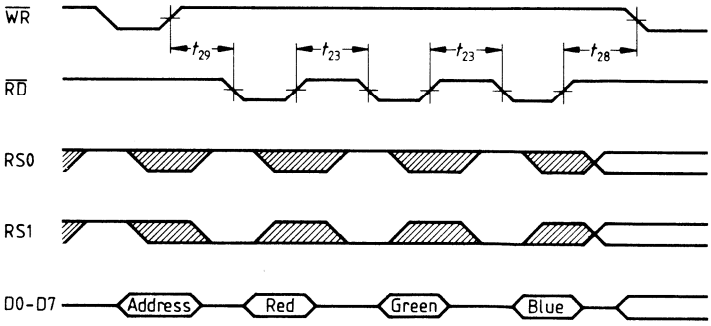
Read from Pixel Mask or Pixel Address Register Followed by any Access



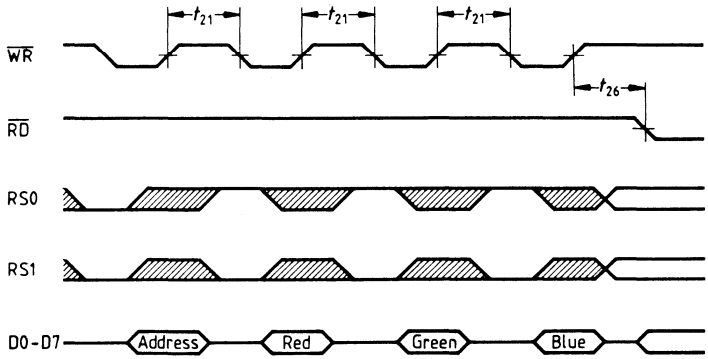
Color Value Read Followed by any Read



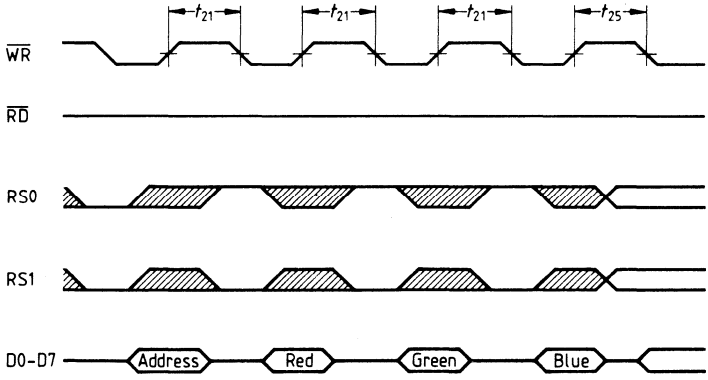
Color Value Read Followed by any Write



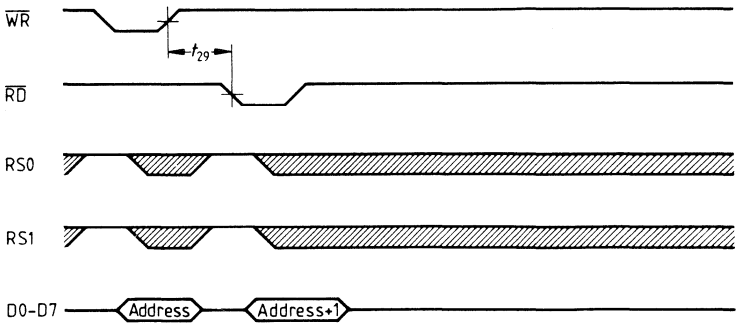
Color Value Write Followed by any Read



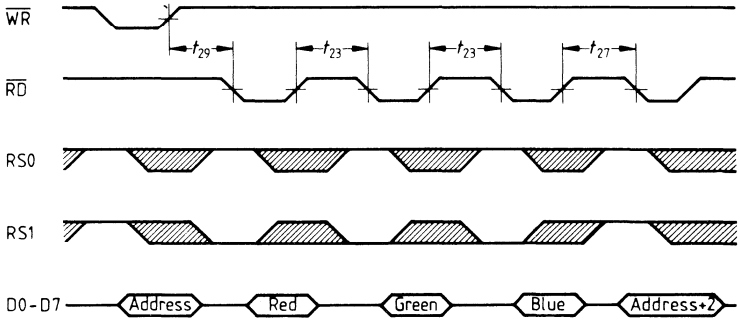
Color Value Write Followed by any Write



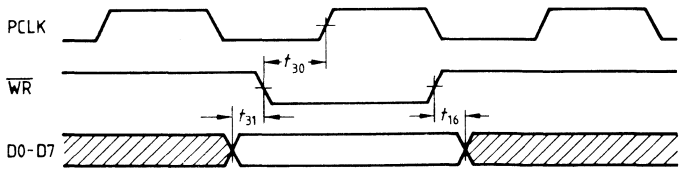
Color Value Read Followed by Address Register Read



Address Register Write Followed by Address Register Read



Synchronized Pixel Mask Register Write



Ordering Information

Type	Ordering code	Package	Function
SAB 82C171-35-P	Q67120-P289	P-DIP-28	CMOS Color Palette, 35MHz
SAB 82C171-50-C	Q67120-P305	C-DIP-28	CMOS Color Palette, 50MHz
SAB 82C171-50-P	Q67120-P306	P-DIP-28	CMOS Color Palette, 50MHz

SIEMENS

CMOS Color Palette SAB 82C176

Advanced Information

- 50 MHz maximum pixel rate
- 256 colors out of 262144 possible colors
- Monolithic CMOS
- Three 6-bit DACs
- Analog RGB composite blank output to drive directly into doubly terminated 75 Ω cable
- Compatible with RS343A / RS170A video standard
- Pixel address input mask function
- Read back of lookup table and register contents
- 28-pin plastic dual-in-line package, P-DIP-28 (600 mil)
- Single 5V power supply
- Fully pin and function compatible with industry standard color palette for VGA and MCGA systems

The SAB 82C176 is a monolithic CMOS color palette including a color lookup table and a digital to analog converter. The analog outputs are designed to drive an analog 75 Ω doubly terminated input of a RS170A or RS343A standard monitor (37.5 Ω load).

The SAB 82C176 is used in graphics systems working with up to 256 colors, which may independently be taken from a total of 262144 colors.

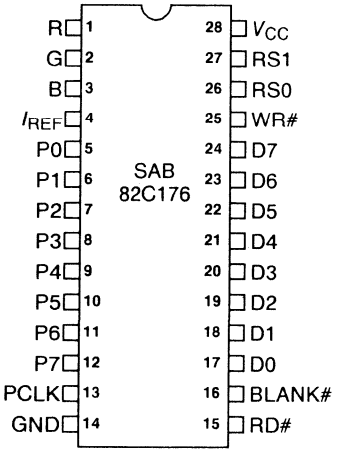
The SAB 82C176 is pin and functional compatible to the industry standard color palette for VGA and MCGA systems.

Ordering Information

Type	Ordering code	Package	Description
SAB 82C176-40-P	Q67120-P308	P-DIP-28	CMOS Color Palette, 40MHz
SAB 82C176-50-P	Q67120-P309	P-DIP-28	CMOS Color Palette, 50MHz

Pin Configuration

P-DIP-28



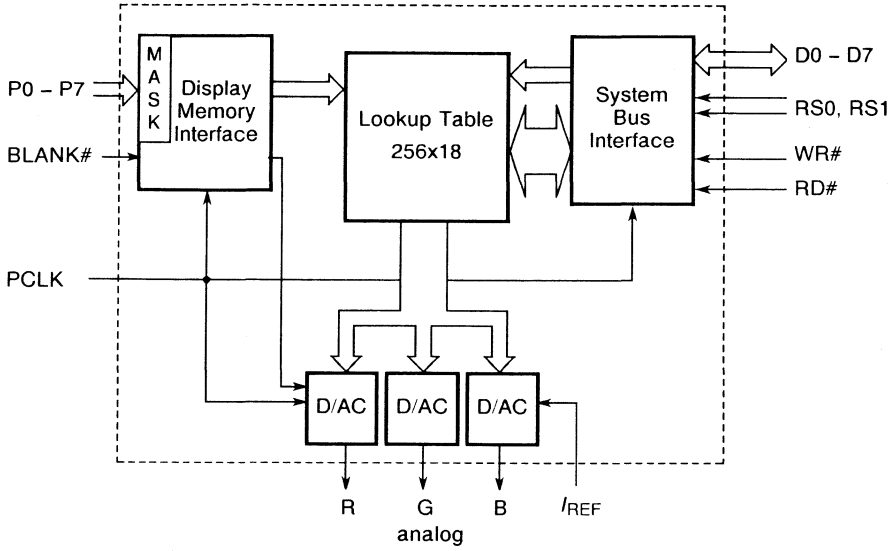
Pin Names

D0 - D7	Data Bus
RD#	Read
WR#	Write
RS0, RS1	Register Select
P0 - P7	Pixel Address
R, G, B	Red, Green, Blue
I_{REF}	Reference Current
BLANK#	Blanking
PCLK	Pixel Clock
V_{CC}	Power Supply (+ 5V)
GND	Ground (0V)

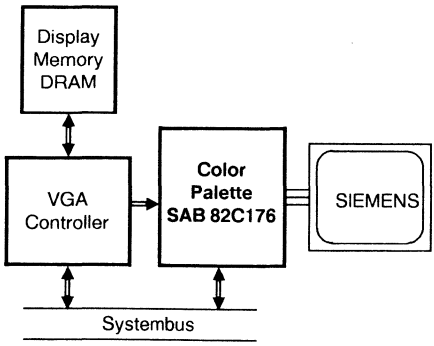
Pin Definitions and Functions

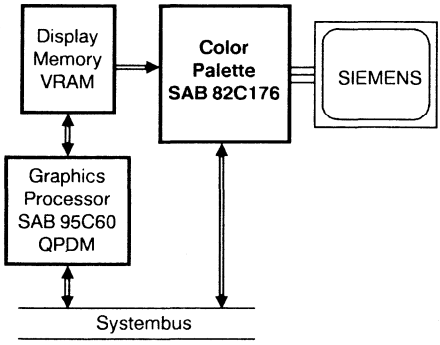
Symbol	Pin	Input (I) Output(O)	Function
PCLK	13	I	**Pixel Clock** provides the video timing control of the SAB 82C176 through the three pipeline stages from pixel address and blank inputs to the three analog outputs.
P0-P7	5-12	I	**Pixel Address** value ANDed with the pixel mask register is used as direct address to the color lookup table (these inputs are sampled with the rising edge of PCLK).
BLANK#	16	I	**BLANK** input (active low) forces the DACs of the SAB 82C176 to the value zero, delayed by 3 clocks according to the pipeline (this input is sampled with the rising edge of PCLK).
R, G, B	1, 2, 3	O	**Red, Green, Blue** Analog outputs of the three 6-bit DACs to drive a doubly terminated 75 Ω input of a RS343A or RS170A standard monitor.
I_{REF}	4	I	**Current Reference** Reference analog input for the DACs reference current, is drawn from V_{CC}.
D0-D7	17-24	I/O	**Databus** (bidirectional) The SAB 82C176 color palette is programmed via this 8-bit data bus.
RS0, RS1	26, 27	I	**Register Select** These pins select the register to be accessed during a system bus read or write cycle.
WR#	25	I	**Write#** A active low value on this pin performs a write access of the register, selected by RS0, RS1.
RD#	15	I	**Read#** A active low value on this pin performs a read access of the register, selected by RS0, RS1.
V_{CC}	28	-	**Power supply** (+ 5V)
GND	14	-	**Ground** (0V)

Block Diagram



Two Typical Applications





Functional Description

General

The SAB 82C176 color palette is a device designed for use as the output stage of raster scan video systems. It contains a high speed lookup table (RAM) of 256 x 18-bit, three 6-bit DACs, a systembus interface and a display memory interface including a pixel word mask.

Typically the color palette is placed between the monitor and the display controller with its display memory.

Pixel rates of up to 50 MHz are achieved by pipelining the memory access over three clock periods.

Video Path

The video path is the path, where the pixel information is brought through the color palette from the display memory interface via the lookup table to the analog outputs. The video path is designed for a very high throughput.

An 8-bit value, written to the pixel address input of the display memory interface, is used by the palette as a read address for the lookup table.

On the rising edge of pixel clock the pixel address and BLANK inputs are sampled, after three further rising edges of pixel clock the relevant analog outputs appear.

The color palette includes a pixel word mask, which is controlled via the systembus and is used for masking the pixel address inputs of the display memory interface.

Each location of the lookup table, addressed by the pixel address inputs, contains an 18-bit word. Partitioned into three 6-bit words, the 18-bit data coming out of the lookup table is converted by three 6-bit DACs. The resulting three analog signals, red, green and blue, directly drive the R, G, B output for a RS170A / RS343A standard color or monochrome monitor.

The analog outputs of the DACs are designed for driving a doubly terminated 75 Ω cable. Due to this the effective analog output load ($R_{EFFECTIVE}$) is 37.5 Ω. With an I_{REF} of 8.88 mA the DACs are capable of producing an amplitude of 0.7 V for peak white.

The BLANK signal input acts on all three of the analog outputs driving them to 0V when active. An internal delay on the BLANK signal is used to correct the relationship of the BLANK signal and the pipelined pixel stream at the analog outputs.

The corresponding I_{REF} for various peak white voltages and effective output loading combinations may be calculated according to the following expression:

$$I_{REF} = \frac{V_{PEAK\ WHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note: For all values of I_{REF} and output loading: $V_{BLACK\ LEVEL} = 0\ V$

Systembus Interface

The system bus interface is used for initialization and controlling the device. It contains an 8-bit bidirectional databus, two register select lines, a read line and a write line.

With the falling edge of the read or write signal the register select input is latched and decoded for selecting a register, with the rising edge data is transferred.

An internal synchronizing circuit enables access the lookup table asynchronous to the video path without any visable shnow effect on the screen.

Register Description

The list below shows the three systembus interface registers of the SAB 82C176 and the four register addresses through which they can be accessed. All registers are able to perform read and write accesses.

RS1	RS0	Register Name
0	0	Pixel address (preparing a color value write access)
1	1	Pixel address (preparing a color value read access)
0	1	Color value
1	0	Pixel mask

Pixel Address Register

There is a single pixel address register within the SAB 82C176. It is used for addressing the lookup table for read and write accesses by the systembus interface.

A write to the pixel address register via register select 00 is preparing a write access to the color-value-register (see"Writing to the lookup table").
A write to the pixel address register via register select 11 is preparing a read access from the color-value register (see"Reading from the lookup table").

The contents of the pixel address register can be read from both, register select 00 and 11.

Color Value Register

This 18-bit wide register is used as a buffer between the systembus and the lookup table. An 18-bit value can be written to or read from this register in three sequential accesses of 6-bit for each color. The sequence is: red-green-blue. The 6-bit value is transferred via the pins D0 - D5 of the systembus interface. Pins D6 and D7 are not used in write operations and are set to logical zero at read cycles.

Pixel Mask Register

The pixel mask register is accessed via the systembus and is independent of the color value and the pixel address register. The pixel address inputs of the video path are bitwise ANDed with the contents of the pixel mask register. In other words the logical value of a pin of the pixel address input is ignored and driven to "0" if the equivalent bit in the mask register is "0".

Writes to the pixel mask register are synchronized internally to the pixel clock. Thus any access to the pixel mask register can be asynchronous to the pixel clock.

The pixel mashing function can be used to create blinking or flashing objects and to ignore unused pixel address inputs.

Accessing the Lookup Table

The color palette SAB 82C176 is designed for fast access to the lookup table via the system bus interface. Therefore it can be set into two different modes: read mode for lookup table read access and write mode for lookup table write access. The modes are set and changed by writing into the pixel address register: for setting read mode the pixel address register is written via register select 11 and for setting write mode the pixel address register is written via register select 00.

Whenever the pixel address register is updated any unfinished color value read or write sequence is aborted and a new one may begin.

Writing to the Lookup Table

To set a new color definition, a value specifying a location in the color lookup table is first written to the pixel address register (register select 00). By this the color palette is set into write mode and automatically performs the following operation:

1. Specifying of an address within the lookup table.
2. Initializing of the color value register.

The values for the red, green and blue intensities are then written sequentially to the color value register (register select 01). After the blue data is written to the color value register the new color definition is transferred to the color lookup table and the pixel address register is automatically incremented pointing to the next location.

Due to this increment mechanism, it is simple to write a set of consecutive locations with new color definitions. First the start address of the set is written to the pixel address register. Then the color values for each location are written sequentially to the color value register.

Reading from the Lookup Table

In order to read a color definition a value specifying the location in the lookup table to be read is written to the pixel address register (register select 11). By this the color palette is set into read mode and automatically performs the following operation:

1. Addressing one 18-bit word of the lookup table.
2. Loading the color value register with the contents of that word.
3. Increment of the address from operation 1.

The red, green and blue intensity values then can be read by a sequence of three reads from the color value register (register select 01). After the blue value has been read, the location in the lookup table, currently specified by the pixel address register, is copied to the color value register and the pixel address register is again incremented automatically.

Thus a set of color definitions in consecutive locations can be read simply by writing the start address of the set to the pixel address register and then sequentially reading the color values for each location in the set.

Due to the increment mechanism, during each read access of the color value register containing the value of location 'n', the pixel address register contains the value 'n + 1'.

Asynchronous Lookup Table Access

The pixel address and color value registers may be accessed totally asynchronous to the high speed timing of the pixel stream being processed by the SAB 82C176. Data transfers between the lookup table and the color value register are internally synchronized to the pixel clock in the period between microprocessor interface accesses. Due to this logic, various minimum periods are specified between systembus interface accesses, to allow for the appropriate transfers to take place.

Reading from the Pixel Address Register

There is no difference from a read from address 1.1 to a read from address 0.0. In both ways the actual contents of the pixel address register are put out to the systembus interface. The contents of the pixel address register are not changed by this operation. But if a value 'n 'was written by register select 11 to the pixel address register, in a following read access the value 'n + 1' is put out, due to the increment.

Absolute Maximum Ratings

Voltage on V_{CC}	7.0 V
Voltage on any other pin	V_{SS} – 1.0 V to V_{CC} + 0.5 V
Temperature under bias	– 45 to 85 °C
Storage temperature (ambient)	– 65 to 150 °C
Power dissipation	1W
Reference current	–15 mA
Analog output current (per output)	45 mA
DC digital output current	25 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{CC}[12)] = 5 V ±10 %; V_{SS} = 0 V

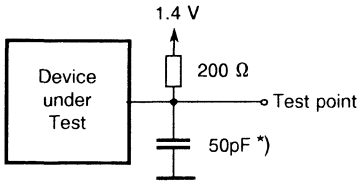
Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Average power supply current	I_{CC}	–	160	mA	SAB 82C176-50 1)
Average power supply current	I_{CC}	–	155	mA	SAB 82C176-40 1)
Digital input current (any input)	I_{IN}	–	±10	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Reference current	I_{REF}	-7.0	–	–10	mA
Off state digital output current	I_{OZ}	–	±50	µA	–
Input logic "1" voltage	V_{IH}	2.0	–	V_{CC} + 0.5	V
Input logic "0" voltage	V_{IL}	-0.5	–	0.8	V
Output logic "1"	V_{OH}	2.4	–	V	I_{OUT} = – 5 mA
Output logic "0"	V_{OL}	–	0.4	V	I_{OUT} = 5 mA
Voltage at I_{REF} input (pin 4)	V_{REF}	V_{CC} – 3	V_{CC}	V	$V_{SS} \leq V_{IN} \leq V_{CC}$
Digital input capacitance	C_{IN}	–	7	pF	2)
Digital output capacitance	C_{OUT}	–	7	pF	2) 3)

Notes see page 13.

D/A Converter Characteristics 4) 5)

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Resolution		6	–	–	bits	–
Maximum output voltage	V_{OUT} (max)	1.5	–	–	V	$I_{OUT} \leq 10$ mA
Maximum output current	I_{OUT}	21	–	–	mA	$V_{OUT} \leq 1$ V
Full scale error		–	–	±5	%	6)
DAC to DAC correlation		±2	–	–	%	7)
Integral linearity		±0.5	–	–	LSB	8)
Rise time (10% to 90%)		–	–	8	ns	9)
Full scale settling time		–	–	20	ns	SAB 82C176-50, 9) 2) 10)
Full scale settling time		–	–	25	ns	SAB 82C176-40, 9) 2) 10)
Glitch energy		–	120	–	pVsec	9) 2)
Analog Output Capacitance	C_{AOUT}	–	–	10	pF	2) 11)

Test load for digital outputs



*) including scope and jig capacitance

AC Test Conditions

Input pulse levels . . . . . V_{SS} to 3 V

Typical input rise and fall times (10 to 90%) . . . . . 3 ns

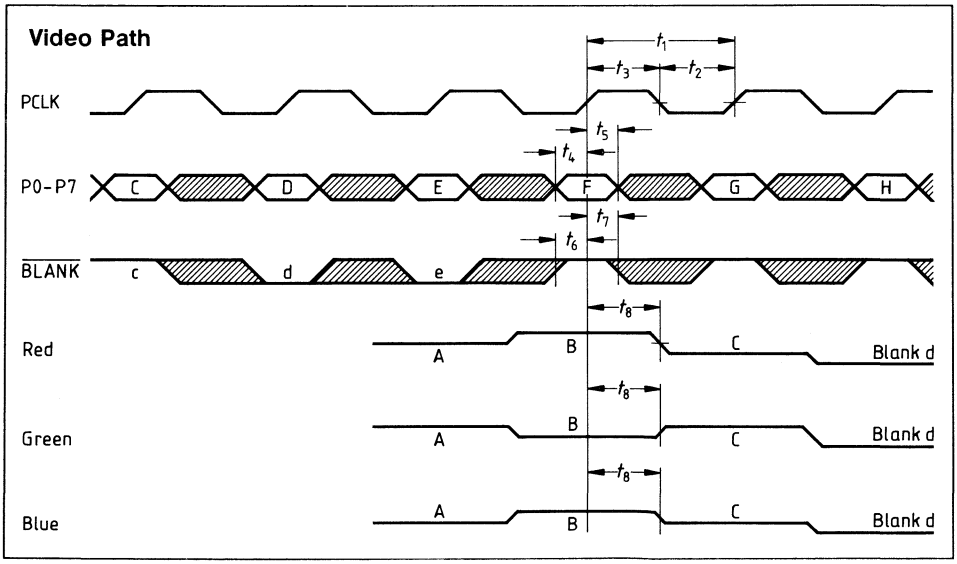
Digital input timing reference level . . . . . 1.5 V

Digital output timing reference level . . . . . 0.8 and 2.4 V

Notes see page 13.

AC Characteristics

Parameter	Symbol	Limit values				Unit	Test condition
		SAB 82C176-40		SAB 82C176-50			
		min.	max.	min.	max.		
Video Path							
Video Path PCLK Period	t_1	25	10000	20	10000	ns	
PCLK jitter	Δt_1	–	±2.5	–	±2.5	%	
PCLK width low	t_2	9	10000	6	10000	ns	
PCLK width high	t_3	7	10000	6	10000	ns	
Pixel word setup time	t_4	5	–	4	–	ns	13)
Pixel word hold time	t_5	5	–	4	–	ns	13)
BLANK setup time	t_6	5	–	4	–	ns	
BLANK hold time	t_7	5	–	4	–	ns	
PCLK to valid DAC output	t_8	5	30	5	30	ns	14)
Differential output delay between the analog outputs of the same device	Δt_8	–	2	–	2	ns	
PCLK transition time	–	–	50	–	50	ns	



Notes see page 13.

AC Characteristics (cont'd)

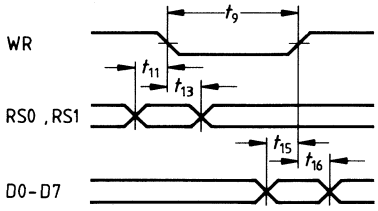
Parameter	Symbol	Limit values				Unit	Test condition
		SAB 82C176-40		SAB 82C176-50			
		min.	max.	min.	max.		
Systembus Interface							
WR# pulse width low	t_9	50	–	50	–	ns	
RD# pulse width low	t_{10}	50	–	50	–	ns	
Register select setup time to WR# low	t_{11}	15	–	10	–	ns	
Register select setup time to RD# low	t_{12}	15	–	10	–	ns	
Register select hold time to WR# low	t_{13}	15	–	10	–	ns	
Register select hold time to RD# low	t_{14}	15	–	10	–	ns	
Write data setup time	t_{15}	15	–	10	–	ns	
Write data hold time	t_{16}	15	–	10	–	ns	
Output turn-on delay	t_{17}	5	–	5	–	ns	
Read enable access time	t_{18}		40		40	ns	
Output hold time	t_{19}	5	–	5	–	ns	
Output turn-off delay	t_{20}		20		20	ns	15)
Successive write interval	t_{21}	$3 * t_1$	–	$3 * t_1$	–	ns	
Write followed by read interval	t_{22}	$3 * t_1$	–	$3 * t_1$	–	ns	16)
Successive read interval	t_{23}	$3 * t_1$	–	$3 * t_1$	–	ns	17)
Read followed by write interval	t_{24}	$3 * t_1$	–	$3 * t_1$	–	ns	18)
Write after color write	t_{25}	$3 * t_1$	–	$3 * t_1$	–	ns	
Read after color write	t_{26}	$3 * t_1$	–	$3 * t_1$	–	ns	
Read after read blue color value	t_{27}	$6 * t_1$	–	$6 * t_1$	–	ns	
Write after read blue color value	t_{28}	$6 * t_1$	–	$6 * t_1$	–	ns	
Read after read-address write	t_{29}	$6 * t_1$	–	$6 * t_1$	–	ns	
Write/Read enable transition time	–	–	50	–	50	ns	

Notes see page 13.

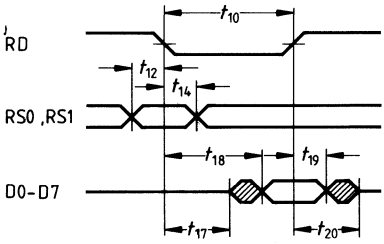
Notes for pages 9), 10), 11 and 12)

1) I_{CC} is dependent on digital output loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated pixel clock frequency. $I_{OUT} = I_{OUT}$ (max.).
2) This parameter is sampled, not 100% tested.
3) Voltage on READ# pin $\geq V_{IH}$ (min.) to disable D0 – D7).
4) Tested with $I_{REF} = -8.88$ mA.
5) To assure the quality of the DACs, the power supply and I_{REF} must be absolutly constant.
6) Full scale error from the value predicted by the design equations.
7) About the mid point of the distribution of the three DACs measured at full scale deflection
8) Linearity measured from the least squares best fit line through the DAC characteristics. Monotonicity guaranteed.
9) Load = 37.5 Ω + 30 pF.
10) From a 2% change in the output voltage until settling to within 2% of the final value.
11) Voltage on BLANK# $\leq V_{IL}$(max) to disable R, G, B output.
12) This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.
13) The pixel address input has to be setup as a valid logic level with the appropriate setup and hold times to each rising edge of the PCLK (this requirement includes the blanking period).
14) A valid analog output is defined as when the changing analog signal is 50% between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions
15) Measured ±200 mV from steady state output voltage
16) Except after writing to pixel address register with RS = 1,1 (see t_{29})
17) Except after writing blue color value (see t_{27})
18) Except after reading blue color value (see t_{28})

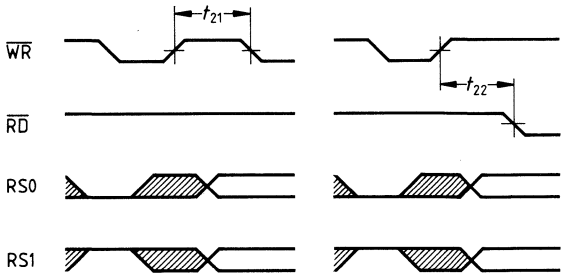
Basic Write Cycle



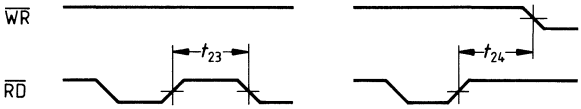
Basic Read Cycle



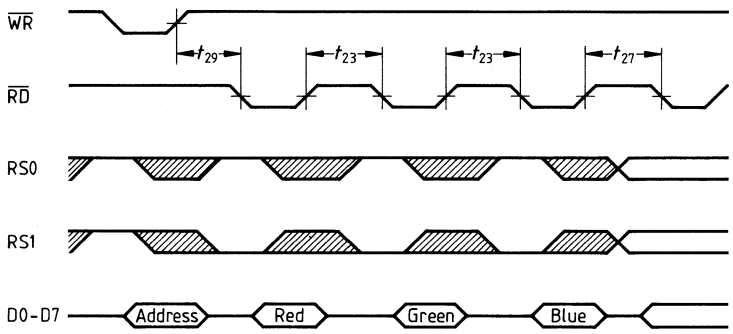
Write to Pixel Mask Register Followed by any Access



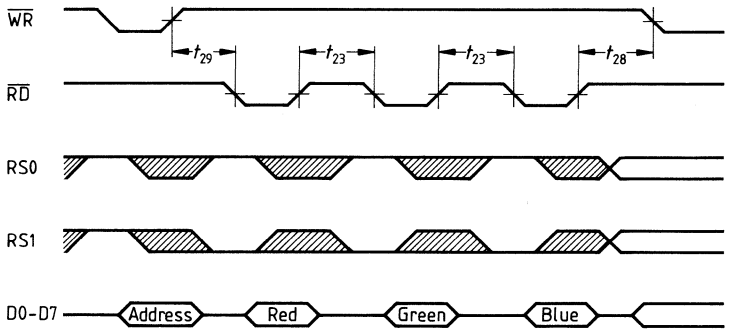
Read from Pixel Mask or Pixel Address Register Followed by any Access



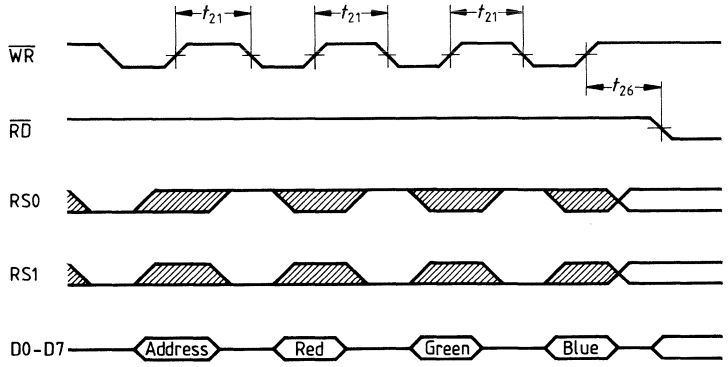
Color Value Read Followed by any Read



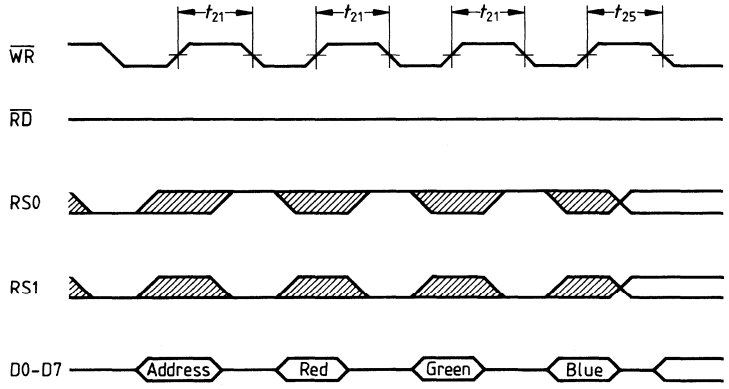
Color Value Read Followed by any Write



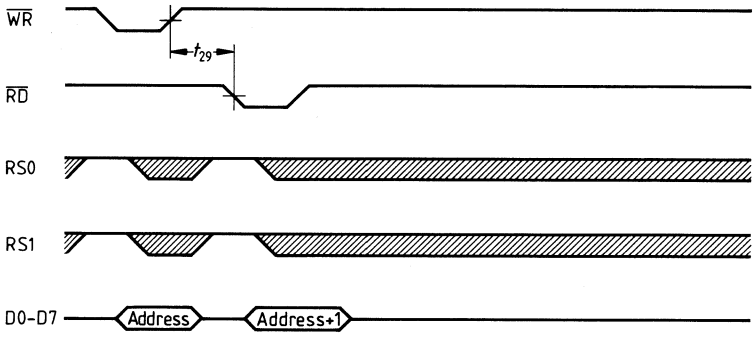
Color Value Write Followed by any Read



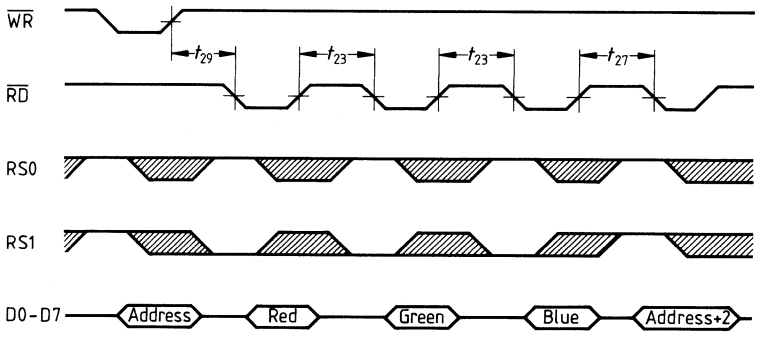
Color Value Write Followed by any Write



Color Value Read Followed by Address Register Read



Address Register Write Followed by Address Register Read

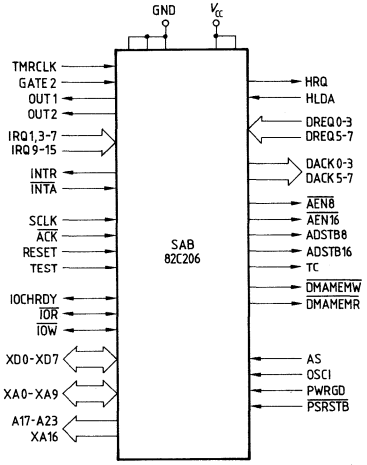


SAB 82C206
Integrated Peripheral Controller

Preliminary

- 100% compatible to PC/AT designs
- Fully compatible to SAB 8237 DMA controller, SAB 8259 interrupt controller, SAB 8254 timer/counter, and 146818 real time clock
- 7 DMA channels, 13 interrupt request channels, 2 timer/counter channels, and a real time clock
- Reduced recovery time (120 ns) between control signals
- Programmable wait states for the DMA cycle and internal register access
- 8 MHz DMA clock
- 16 Mbytes of DMA address space
- 114 Bytes of CMOS RAM memory
- Full static design
- PL-CC-84 package
- Advanced CMOS (ACMOS) technology
- Compatible with the standard 82C206

Logic Symbol



The SAB 82C206 integrated peripheral controller incorporates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, one 146818 real time clock, one 74LS612 memory mapper, in addition to several other TTL/SSI interface logic chips to provide a single-chip integration of all the peripherals attached to the peripheral bus (X-bus) in the IBM PC/AT. While offering complete compatibility to the IBM PC/AT architecture, the chip exhibits enhanced features and improved speed performance. These include additional 64 bytes of user RAM for the real time clock and drastically reduced recovery specifications for the 8237, 8259 and 8254.

Variable wait state option is provided for the DMA cycles. Programmable delays are possible for CPU access to the internal registers of the chip. The chip allows selection of an 8 or 4 MHz DMA clock.

The SAB 82C206 provides a highly integrated high-performance system solution for PC/AT compatible implementations. It is compatible with the standard 82C206 IPC and offers compatibility to the CS8220, CS8221 and CS8230 PC chip sets.

The SAB 82C206 is fabricated in Siemens ACMOS technology and packaged in an 84-pin plastic leaded chip carrier (PL-CC-84) package.

Figure 1
Pin Configuration (Top View)

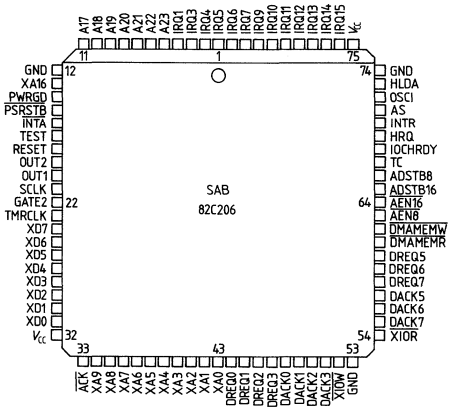
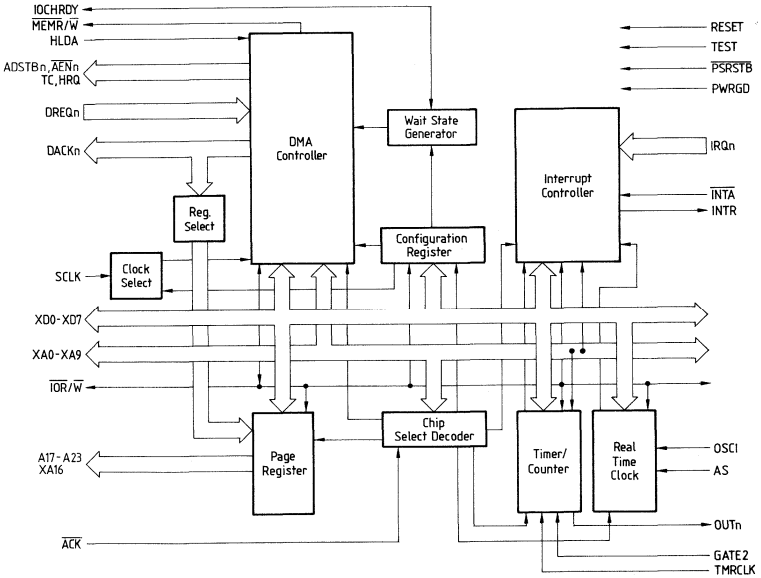


Figure 2
Block Diagram



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
IRQ1 IRQ3-IRQ5 IRQ6, IRQ7 IRQ9-IRQ15	4 3–1 84, 83 82–76	I I I I	**Interrupt requests** Asynchronous inputs. An interrupt request is executed by raising an IRQ input low to high and holding it high until it is acknowledged (edge-triggered mode) or just by a high level on an IRQ input (level-triggered mode).
A23-A17 XA16	5–11 13	O O	**DMA page register address** XA16 and A17-A23 are tristate output pins. XA16 is the least significant bit of the DMA page register and is used for DMA transfers to 8-bit peripherals only (channel 0-3). XA16 is not used for DMA transfers to 16-bit peripherals (channel 5-7) as XA9-XA16 is provided by demultiplexing the data bus. A17-A23 are the upper 7 bits of the DMA page register.
PWRGD	14	I	**Power good** The power good pin must be high for bus cycles in which the CPU accesses the RTC. When PWRGD is low, all address, data, data strobe and R/W pins are disconnected from the processor.
$\overline{\text{PSRSTB}}$	15	I	This input is used to establish the condition of the control registers when power is applied to the device. In a PC/AT compatible design, this pin should be tied to the battery back-up circuit. When $\overline{\text{PSRSTB}}$ and TEST are both low, the following occurs: (a) Periodic interrupt enable (PIE) bit is cleared to zero. (b) Alarm interrupt enable (AIE) bit is cleared to zero. (c) Uptdate ended interrupt enable (UIE) bit is cleared to zero. (d) Update ended interrupt flag (UF) bit is cleared to zero. (e) Interrupt request status flag (IRQF) is cleared to zero. (f) Periodic interrupt flag (PF) bit is cleared to zero. (g) The part is not accessible. (h) Alarm interrupt flag (AF) bit is cleared to zero. (i) Square wave output enable list is cleared to zero.
$\overline{\text{INTA}}$	16	I	**$\overline{\text{Interrupt acknowledge}}$** This pin is used to enable the interrupt vector data of the interrupt controllers to the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
TEST	17	I	**Test** Test is an active high input. It initializes various internal registers so that a device test program starts in a known state. It should be tied low for normal operation.
RESET	18	I	**Reset** Reset is an active high input which affects the following registers: DMA controllers: clears the command, status, DMA request, temporary register, first/last flipflop; sets the mask register. Following reset, the DMA controller is in an idle state. Interrupt controllers: clears the edge sense circuit, the interrupt mask register, all ICW4 functions, IRQ0 is assigned highest priority, slave address is set to 7, special mask mode is disabled and status read is set to IRR.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
OUT 2	19	O	**Out 2** Output of timer 2. In a PC/AT compatible design, OUT 2 is used to drive the speaker.
OUT 1	20	O	**Out 1** Output of timer 1. In a PC/AT compatible design, timer 1 is programmed as a rate generator to produce 15 µsec period signals used for interrupt request to initiate refresh cycles.
SCLK	21	I	**Clock input** The clock input is used to generate the timing signals which control DMA operations. This input may be driven from DC to 16 MHz. The clock may be stopped in either state for standby operation. The internal clock used for DMA is either the SCLK or SCLK/2 depending on the setting of DMA clock select bit in the configuration register.
GATE2	22	I	**Gate 2** Gate input for counter 2. In a PC/AT compatible design, the counter 2 is used for tone generation for speaker. In this design, the Gate 2 input is driven by bit 0 of I/O port 61H (called TIM2GATE SPK).
TMRCLK	23	I	**Timer clock** Clock input for counter 0, counter 1 and counter 2.
XD7-XD0	24–31	I/O	**Data bus** The data bus lines are tristate bidirectional lines connected to the system data bus (XD bus in a PC/AT design). The outputs are enabled in the program condition during the I/O read to output the contents of the DMA controller registers (address register, status register, the temporary register or a word count register), the three interrupt controller registers (interrupt request register, in service register and the interrupt mask register), the timer/counters registers (namely the contents of these counters or states of the counters), the real time clock's internal registers and page registers of the memory mapper. During an I/O write cycle, the outputs are disabled and the CPU can program the DMA controller registers, the interrupt controller registers, the timer/counters registers, the DMA page register and the real time clock registers and internal RAM. During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB8 or ADSTB16. During memory-to-memory operations, data from the memory comes into the DMA controller on the data bus during read from the memory. In the write to memory transfer, the data bus outputs the data for the new memory location. During the interrupt acknowledge sequence, the interrupt controllers output the interrupt vector byte on the data bus. Data bus XD7-XD0 also acts as the multiplexed address/data bus for the real time clock.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{ACK}$ (MSE)	33	I	**Module select enable** When high, it enables the chip select function on one of the modules (DMA controller, INT controller, timer, RTC, DMA page register or the configuration register) for the programming function, i.e. CPU read or write of the command, status or other register of various modules of the SAB 82C206. When low, the SAB 82C206 is essentially disconnected from the system bus. The SAB 82C206 at this time could be performing an active DMA or an interrupt cycle. In a PC/AT compatible design, this pin is tied to $\overline{ACK}$ signal.
XA9 XA8-XA0	34 35-43	I I/O	**Address bus** This is the system address bus used to address various registers of the SAB 82C206. It is tied to the external bus (XA bus) in a PC/AT compatible design. During a non-DMA cycle, A3-A0 act as inputs and are used by the CPU to address the registers of the DMA controller corresponding to DMA channels 0-3. A4-A1 address the registers of the DMA controller corresponding to DMA channels 5-7. In the active DMA cycle, A7-A0 are outputs and carry address information for DMA channels 0-3. Correspondingly, A8-A1 are address outputs for 16-bit DMA channels 5-7. During program condition, A9-A0 are used to address the configuration register and the internal registers of DMA controller, INT controller, timer, RTC and memory mapper.
DREQ0-3 DREQ5-7	44-47 60-58	I I	**DMA request** The DMA request pins (DREQ) are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed priority, DREQ0 has the highest priority and DREQ7 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the DMA clock is stopped. Unused DREQ inputs should be pulled high or low (inactive) and the corresponding mask bit set. DREQ0-DREQ3 support 8-bit transfers between 8-bit I/O and 8 or 16-bit system memory. DREQ5-DREQ7 support 16-bit data transfers between 16-bit peripheral and 16-bit system memory. DREQ4 is not available because it is used to cascade DREQ0-DREQ3.
DACK0-3 DACK7-5	48-51 55-57	O O	**DMA acknowledge** DMA acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The active polarity of these lines is programmable. Reset initializes them to active low. Because these signals are used internally for cascading the DMA channels and for DMA page register selection, these signals must be programmed to be active low.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{XIOW}}$	52	I/O	**$\overline{\text{I/O write}}$** I/O write is a bidirectional active low tristate signal. In an idle cycle (non-DMA, non-interrupt), it is an input control signal used by the CPU to load information to the SAB 82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA controller to load data to the peripheral devices during a DMA read transfer.
$\overline{\text{XIOR}}$	54	I/O	**$\overline{\text{I/O read}}$** I/O read is a bidirectional active low tristate line. In an idle cycle (non-DMA, non-interrupt), it is an input control signal used by the CPU to read the SAB 82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA controller to access data from a peripheral device during a DMA write transfer.
$\overline{\text{DMAMEMR}}$	61	O	**$\overline{\text{DMA memory read}}$** This an active low tristate output used to access data from the selected memory location during DMA read or memory-to-memory transfer.
$\overline{\text{DMAMEMW}}$	62	O	**$\overline{\text{DMA memory write}}$** This is an active low tristate output used to write data to the selected memory location during DMA write or a memory-to-memory transfer. In a PC/AT compatible design, this signal is connected to $\overline{\text{XMEMW}}$.
$\overline{\text{AEN8}}$	63	O	**$\overline{\text{Address enable}}$** for 8-bit DMA transfers. This signal is the output enable for the 8-bit latch containing the upper 8 address bits (A8-A15). It enables A8-A15 to the system address bus. It is inactive when the external bus master controls the system bus. $\overline{\text{AEN8}}$ is active low.
$\overline{\text{AEN16}}$	64	O	**$\overline{\text{Address enable}}$** for 16-bit DMA transfers. This signal enables the 8-bit latch containing the upper 8 address bits (A9-A16) on to system address bus. It is inactive when external bus master controls the system bus. $\overline{\text{AEN16}}$ is active low.
ADSTB16	65	O	**Address strobe for 16-bit transfers** This is an active high signal used to control latching of the upper address byte A9-A16 for 16-bit DMA transfers. Its function is just like ADSTB8. ADSTB16 is active for DMA channels 5-7.
ADSTB8	66	O	**Address strobe for 8-bit transfers** This is an active high signal used to control latching of the upper address byte (A8-A15) for 8-bit peripherals. It will drive directly the strobe input of external transparent octal latches. During block operations, ADSTB8 will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. ADSTB8 is active for DMA channels 0-3.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
TC	67	O	**Terminal count** Terminal count (TC) is an active high signal. Information concerning the completion of DMA services is available at the TC output pin. A pulse is generated by the DMA controller when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers TC will be output when the TC for channel 1 occurs. When a TC pulse occurs, the DMA controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel unless the channel is programmed for auto-initialize. In that case, the mask bit remains clear.
IOCHRDY	68	I/O	**I/O channel ready** In the input mode, a low on IOCHRDY causes the internal DMA ready signal to go low asynchronously. When IOCHRDY goes high, one DMA clock cycle will elapse before internal DMA ready goes up. This signal is used to extend memory read and write pulses for the DMA controllers to accommodate slow memories or I/O devices. IOCHRDY must satisfy set-up and hold times with respect to SCLK in order to work reliably. In the output mode, this pin is an open drain output and provides an active low output whenever any SAB 82C206 register is addressed for read or write. This output will remain low for a programmed number of SCLK cycles (as configured by bits 6 and 7 of the SAB 82C206 configuration register) and then goes high, if pulled up by an external resistor. IOCHRDY provides a means of introducing a programmed number of wait-states (as counted by SCLK cycles) for I/O read/write cycles to SAB 82C206. In a PC/AT architecture based design this pin should be wire-ored to PC/AT's IOCHRDY signal.
HRQ	69	O	**Hold request** The hold request output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the DMA controller issues HRQ. The HLDA signal then informs the controller when access to the system buses is permitted. For stand-alone operation where the DMA controller always controls the buses, HRQ may be tied to HLDA. This will result in one S0 state before the transfer.
INTR	70	O	**Interrupt** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, and is usually connected to the CPU's interrupt pin.
AS	71	I	**Address strobe** Address strobe is a positive pulse whose falling edge latches the address from the XD bus.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
OSCI	72	I	**Oscillator input** The time base for the time functions is connected to this pin. External square waves of 32.768 KHz may be connected to this input.
HLDA	73	I	**Hold acknowledge** The active high hold acknowledge from the CPU indicates that it has relinquished control of the system buses.
V_{CC}	32, 75	–	**Power supply (+5 V)**
GND	12, 53, 74	–	**Ground (0 V)**

Functional Description

The SAB 82C206 is an LSI implementation of the standard peripherals required to implement an IBM PC/AT system board. This device contains the equivalent of two 8237A DMA controllers, a 74LS612 mapper, two 8259A interrupt controllers, an 8254 counter/timer, and a 146818 read time clock with RAM. The SAB 82C206 provides all of the standard peripherals required for a system board implementation except the keyboard interface controller. Figure 2 illustrates the subsystems contained within the SAB 82C206.

Two DMA controllers are connected in such a way as to provide the user with four DMA channels (DMA1) for 8-bit transfers and three DMA channels (DMA2) for 16-bit transfers (the first 16-bit DMA channel is used for cascading). Included as part of the DMA subsystem is the page register (DMAPAGE) device which is used to supplement the DMA and drive the upper address lines when required.

Sixteen interrupt channels are provided in the SAB 82C206. These channels are allocated to two cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user-definable interrupt channels. The three internally connected channels are as follows:

Channel 0 – counter/timer counter 0 interrupt
Channel 2 – cascade to slave interrupt controller (INTC2)
Channel 8 – real time clock interrupt

The remaining 13 channels may be defined and utilized as necessary to meet the user-specific system requirements.

A counter/timer (CTC) subsystem contains three independent counters. All three counters are driven from a clock input pin which is independent from the other clock inputs to the device. Counter 0 is connected to interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third channel (counter 2) is a full function counter/timer which has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

A real time clock (RTC) is included in the SAB 82C206 for maintaining the time and date. This subsystem also contains 114 bytes of RAM in addition to the clock/calendar. The clock/calendar information and RAM are kept active by connecting the device to an external battery when system power is turned off.

To interconnect and control all of these major subsystems a top level control section is employed which is divided into subsystems for purposes of discussion.

The first section is the clock and wait state control section. This subsystem controls the generation of DMA wait states and the negation of IOCHRDY (if programmed to do so) during CPU access of the device. The last subsystem is the top level decoder.

In order to accommodate over 200 registers in the SAB 82C206 and maintain I/O decode compatibility with the IBM PC/AT, a multilevel decode scheme is employed. The top level decoder subsystem performs the function of generating enables to the various subsystems. Control and direction of the XD0-XD7 data bus buffers are also handled by this subsystem.

Top Level Decoder

The SAB 82C206 top level decoder provides 8 separate enables to various subsystems of the device. Table 1 contains a truth table for the top level decoder. Enabling of the SAB 82C206 XD0-XD7 output buffers is also controlled by this section. The output buffers are enabled whenever an enable is generated to an internal subsystem and the $\overline{\text{XIOR}}$ signal is asserted.

Table 1
Top Level Decoder

$\overline{ACK}$	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	Address range (Hex)	Selected device
1	0	0	0	0	0	0	X	X	X	X	000-00F	DMA1
1	0	0	0	0	1	0	0	0	0	X	020-021	INTC1
1	0	0	0	0	1	0	0	0	1	X	022-023	CONFIG
1	0	0	0	1	0	0	0	0	X	X	040-043	CTC
1	0	0	0	1	1	1	0	0	0	X	070-071	RTC
1	0	0	1	0	0	0	X	X	X	X	080-08F	DMAPAGE
1	0	0	1	0	1	0	0	0	0	X	0A0-0A1	INTC2
1	0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA2
0	X	X	X	X	X	X	X	X	X	X	Disabled	
X	1	X	X	X	X	X	X	X	X	X	Disabled	
X	X	1	X	X	X	X	X	X	X	X	Disabled	

The decoder is enabled by three signals. These three signals are $\overline{ACK}$, XA9 and XA8. To enable any internal device $\overline{ACK}$ must be "1" and both XA9 and XA8 must be "0".

The decode scheme employed in the SAB 82C206 is designed to comply with the IBM PC/AT requirements and is more fully decoded. If the user wishes to take advantage of the areas which are unused by inserting additional peripherals in the I/O map, he may do so since the subsystems in the SAB 82C206 will not respond to the unused address spaces established by the top level decoder. The extra peripherals may be tied directly to the XD0-XD7 data lines since the SAB 82C206 output buffers are not enabled unless an internal subsystem is enabled.

Clock and Wait State Control

The clock and wait state control subsystem performs four functions, control of the DMA command width, control of the CPU read or write cycle length, and selection of the DMA clock rate. All of these functions are user selectable by writing to the configuration register located at address 023H.

Writing and reading this register is accomplished by first writing a 01H to location 022H to select the SAB 82C206 configuration register, and then performing either a read or write to location 023H.

Configuration register (023H):

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
RW1	RW0	16W1	16W0	8W1	8W0	EMR	CLK

RW1-RW0 – When the higher speed CPU's are accessing the SAB 82C206, the cycle can be extended by programming up to four wait states into the configuration register. This will cause the SAB 82C206 to assert a not ready condition on IOCHRDY (low) whenever a valid decode from the top level decoder is detected and either $\overline{XIOR}$ or $\overline{XIOW}$ is asserted. IOCHRDY will remain low for the number of wait states programmed into the configuration register bits 6 and 7.

RW1	RW0	Read/write cycle wait states
0	0	1
0	1	2
1	0	3
1	1	4

Wait states programmed by RW0 and RW1 are in increments of one SCLK cycle and are not affected by the DMA clock divider.

16W1-16W0 – Wait states can be independently controlled for both 8-bit and 16-bit DMA cycles. This allows the user to tailor the DMA cycle more closely to the application.

16W1	16W0	16-Bit DMA wait states
0	0	1
0	1	2
1	0	3
1	1	4

8W1-8W0 – Wait states may be inserted in 8-bit DMA cycles by programming these two bits in the configuration register.

8W1	8W0	8-Bit DMA wait states
0	0	1
0	1	2
1	0	3
1	1	4

Further control of the cycle length is available through the use of the IOCHRDY pin on the SAB 82C206. During DMA this pin is used as an input to the wait state generation logic to extend the cycle if necessary. This input is driven low by the peripheral to extend the cycle. The cycle can then be completed by releasing IOCHRDY and allowing it to return high.

EMR – This bit enables the extended $\overline{\text{DMAMEMR}}$ function. Normally the assertion of $\overline{\text{DMAMEMR}}$ is delayed one clock cycle later than $\overline{\text{XIOR}}$ in the IBM PC/AT implementation. This may not be desirable in some systems. A "1" programmed into this bit position will start $\overline{\text{DMAMEMR}}$ at the same time as $\overline{\text{XIOR}}$.

CLK – This bit allows the user to insert a divider between the DMA controller subsystems and the SCLK input in, or connect the two directly. When this bit position contains a "0", the SCLK input is divided by two and is used to drive both the 8-bit and 16-bit DMA subsystems. A "1" in this position bypasses the divider and uses the SCLK input directly. Whenever the state of this bit is changed, an internal synchronizer controls the actual switching of the clock to prevent a short clock pulse from causing a DMA malfunction.

DMA wait states are in increments of one DMA clock cycle, which is affected by the DMA clock divider.

The configuration register contents are preloaded by RESET to an initial value of 0C0H. This value establishes a default which is IBM PC/AT compatible and corresponds to:

Read/write cycles – 4 wait states
16-bit DMA transfers – 1 wait state
8-bit DMA transfers – 1 wait state

$\overline{\text{DMAMEMR}}$ is delayed 1 DMA clock cycle later than $\overline{\text{XIOR}}$.

DMA clock is equal to SCLK/2.

DMA Functional Description

The equivalent of two 8237A DMA controllers is implemented in the SAB 82C206. Each controller is a four channel DMA device which will generate the memory addresses and control signals necessary to transfer information between a peripheral device and memory directly. This allows high speed information transfers with less CPU intervention.

The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1), and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection of the two DMA devices, thereby maintaining IBM PC/AT compatibility.

DMA cycle length control is provided internally in the SAB 82C206 allowing independent control for both 8-bit and 16-bit cycles. This is done through the programmable registers which can extend command signals or insert wait states.

Each DMA channel has a pair of 16-bit counters and a reload register for each counter. The 16-bit counters allow the DMA channel to transfer blocks as large as 64 K words. The register associated with each counter allows the channel to reinitialize without reprogramming.

From this point on, the description of the DMA subsystem pertains to both DMA1 and DMA2 unless otherwise noted.

DMA Operation

During normal operation of the SAB 82C206, the DMA subsystem will be in either the idle condition, the program condition or the active condition. In the idle condition the DMA controller will be executing cycles consisting of only one state. The idle state SI is the default condition and the DMA will remain in this condition unless the device has been initialized and one of the DMA requests is active or the CPU attempts to access one of the internal registers.

When a DMA request becomes active the device enters the active condition and issues a hold request to the system. Once in the active condition the SAB 82C206 will generate the necessary memory addresses and command signals to accomplish a memory-to-I/O, I/O-to-memory, or a memory-to-memory transfer. Memory-to-I/O and I/O-to-memory transfers take place in one cycle while memory-to-memory transfers require two cycles. During transfers between memory and I/O, data is presented on the system bus by either memory or the requesting device and the transfer is completed in one cycle. Memory-to-memory transfers, however, require the DMA to store data from the read operation in an internal register. The contents of this register is then written to memory on the subsequent cycle.

During transfers between memory and I/O, two commands are activated during the same cycle. In the case of a memory-to-I/O transfer, the SAB 82C206 will assert both $\overline{\text{DMAMEMR}}$ and $\overline{\text{XIOW}}$ allowing data to be transferred directly to the requesting device from memory. Note that SAB 82C206 does not latch data from nor drive data out on this type of cycle.

The number of clock cycles required to transfer a word of data may be varied by programming the DMA or, optionally extended by the peripheral device. During an active cycle the DMA will sequence through a series of states. Each state will be one DMA clock cycle in length and the number of states in a cycle will vary depending on how the device is programmed and what type of cycle is being performed. The states are labeled S0-S4 and will be explained in detail in the section entitled active condition.

Idle Condition

When no device is requesting service the DMA is in an Idle condition which maintains the state machine in the SI state. During this time the SAB 82C206 will sample the DREQ input pins every clock cycle. The internal select from the top level decoder and HLDA are also sampled at the same time to determine if the CPU is attempting to access the internal registers. When either of the above two situations occurs, the DMA will exit the Idle condition. Note that the program condition has priority over the active condition since a CPU cycle has already started.

Program Condition

The program condition is entered whenever HLDA is inactive and an internal select is active. The internal select is derived from the top level decoder described previously. During this time address lines XA0-XA3 become inputs if DMA1 is selected, or XA1-XA4 become inputs if DMA2 is selected. Note, when DMA2 is selected XA0 is ignored. These address inputs are used to select the DMA controller registers which are to be read or written. Table 2 lists the register address assignment. Due to the large number of internal registers in the DMA subsystem, an internal flip-flop is used to supplement the addressing of the count and address registers. This bit is used to select between the high and low bytes of these registers. The flip-flop will toggle each time a read or write occurs to any of the word count or address registers in the DMA. This internal flip-flop will be cleared by hardware RESET or a master clear command and may be set or cleared by the CPU issuing the appropriate command.

Table 2
DMA Register Address Operations

DMA1	DMA2	$\overline{XIOR}$	$\overline{XIOW}$	Flip-Flop	Register Function
000H	0C0H	0	1	0	Read channel 0 current addres low byte
		0	1	1	Read channel 0 current address high byte
		1	0	0	Write channel 0 base and current address low byte
		1	0	1	Write channel 0 base and current address high byte
001H	0C2H	0	1	0	Read channel 0 current word count low byte
		0	1	1	Read channel 0 current word count high byte
		1	0	0	Write channel 0 base and current word count low byte
		1	0	1	Write channel 0 base and current word count high byte
002H	0C4H	0	1	0	Read channel 1 current address low byte
		0	1	1	Read channel 1 current address high byte
		1	0	0	Write channel 1 base and current address low byte
		1	0	1	Write channel 1 base and current address high byte
003H	0C6H	0	1	0	Read channel 1 current word count low byte
		0	1	1	Read channel 1 current word count high byte
		1	0	0	Write channel 1 base and current word count low byte
		1	0	1	Write channel 1 base and current word count high byte
004H	0C8H	0	1	0	Read channel 2 current address low byte
		0	1	1	Read channel 2 current address high byte
		1	0	0	Write channel 2 base and current address low byte
		1	0	1	Write channel 2 base and current address high byte
005H	0CAH	0	1	0	Read channel 2 current word count low byte
		0	1	1	Read channel 2 current word count high byte
		1	0	0	Write channel 2 base and current word count low byte
		1	0	1	Write channel 2 base and current word count high byte
006H	0CCH	0	1	0	Read channel 3 current address low byte
		0	1	1	Read channel 3 current address high byte
		1	0	0	Write channel 3 base and current address low byte
		1	0	1	Write channel 3 base and current address high byte
007H	0CEH	0	1	0	Read channel 3 current word count low byte
		0	1	1	Read channel 3 current word count high byte
		1	0	0	Write channel 3 base and current word count low byte
		1	0	1	Write channel 3 base and current word count high byte
008H	0D0H	0	1	X	Read status register
		1	0	X	Write command register
009H	0D2H	0	1	X	Read DMA request register
		1	0	X	Write DMA request register
00AH	0D4H	0	1	X	Read command register
		1	0	X	Write single bit DMA request mask register

Table 2
DMA Register Address Operations (cont'd)

DMA1	DMA2	$\overline{XIOR}$	$\overline{XIOW}$	Flip-flop	Register function
00BH	0D6H	0 1	1 0	X	Read mode register Write mode register
00CH	0D8H	0 1	1 0	X X	Set byte pointer flip-flop Clear byte pointer flip-flop
00DH	0DAH	0 1	1 0	X X	Read temporary register Master clear
00EH	0DCH	0 1	1 0	X X	Clear mode register counter Clear all DMA request mask register bits
00FH	0DEH	0 1	1 0	X X	Read all DMA request mask register bits Write all DMA request mask register bits

Special commands are supported by the DMA subsystem in the program condition to control the device. These commands do not make use of the data bus but are derived from a set of addresses, the internal select and $\overline{XIOW}$ or $\overline{XIOR}$. These commands are master clear, clear mask register, clear mode register counter, set and clear byte pointer flip-flop.

The SAB 82C206 will enable programming whenever HLDA has been inactive for one DMA clock cycle. It is the responsibility of the system to ensure that programming and HLDA are mutually exclusive. Erratic operation of the SAB 82C206 can occur if a request for service occurs on an unmasked channel which is being programmed. The channel should be masked or the DMA disabled to prevent the SAB 82C206 from attempting to service a device with a channel which is partially programmed.

Active Condition

The SAB 82C206 DMA subsystem enters the active condition whenever a software request or a DMA request on an unmasked channel occurs and the device is not in the program condition. The SAB 82C206 will then begin a DMA transfer cycle.

In a read cycle for example, after receiving a DREQ, the SAB 82C206 will issue a HRQ to the system. Until a HLDA is returned the DMA will remain in an idle condition. On the next clock cycle the DMA will exit idle and enter state S0. During S0 the device will resolve priority and issue DACK on the highest priority channel requesting service. The DMA will then proceed to state S1 where the multiplexed addresses are output and latched. State S2 is then entered, at which time the SAB 82C206 will assert $\overline{DMAMEMR}$. The device then transitions into S3 where the $\overline{XIOW}$ command is asserted. The SAB 82C206 DMA will then remain in S3 until the wait state counter has decremented to zero and IOCHRDY is true. Note that at least one additional S3 will occur unless compressed timing is selected. Once a ready condition is detected, the DMA will enter S4 where both command lines are deasserted. In burst mode and demand mode, subsequent cycles will begin in S2 unless the intermediate addresses require updating. In these subsequent cycles the lower addresses are changed in S2.

The DMA can be programmed on a channel by channel basis to operate in one of four modes. The four modes are listed in the following.

Single Transfer Mode – This mode directs the DMA to execute only one transfer cycle at a time. DREQ must be held active until DACK becomes active. If DREQ is held active throughout the cycle, the SAB 82C206 will deassert HRQ and release the bus once the transfer is complete. After HLDA has gone inactive the SAB 82C206 will again assert HRQ and execute another cycle on the same channel unless a request from a higher priority channel has been received. In this mode the CPU is ensured of being allowed to execute at least one bus cycle between transfers.

Following each transfer the word count is decremented and the address is incremented or decremented. When the word count decrements from 0000H to FFFFH the terminal count bit in the status register is set and a TC pulse is generated. If the autoinitialization option has been enabled, the channel will reinitialize itself. If autoinitialize is not selected the DMA will set the DMA request bit mask and suspend transferring on that channel.

Block Transfer Mode – When block transfer mode is selected, the SAB 82C206 will begin transfers in response to either a DREQ or a software request and will continue until a terminal count (FFFFH) is reached, at which time TC is pulsed and the status register terminal count bit is set. In this mode DREQ need only be held active until DACK is asserted. Autoinitialization is optional in this mode also.

Demand Transfer Mode – In demand transfer mode the DMA will start transfers in response to the assertion of DREQ and will continue until either terminal count is reached or DREQ becomes inactive. This mode is normally used for peripherals which have limited buffering capability. The peripheral can initiate a transfer and continue until its buffer capacity is exhausted. The peripheral may then re-establish service by again asserting DREQ. During idle periods between transfers the CPU is released to operate and can monitor the operation by reading intermediate values from the address and word count registers. Once DREQ has been deasserted, higher priority channels are allowed to intervene. Reaching terminal count will result in the generation of a TC pulse, the setting of the terminal count bit in the status register and autoinitialization (if enabled).

Cascade Mode – This mode is used to interconnect more than one DMA controller, to extend the number of DMA channels while preserving the priority chain. In cascade mode the master DMA controller does not generate address or control signals. The DREQ and DACK signals of the master are used to interface the HRQ and HLDA signals of the slave DMA devices. Once the master has received a HLDA from the CPU in response to a DREQ caused by the HRQ from a slave DMA controller, the master DMA controller will ignore all inputs except HLDA from the CPU and DREQ on the active channel. This prevents conflicts between the DMA devices.

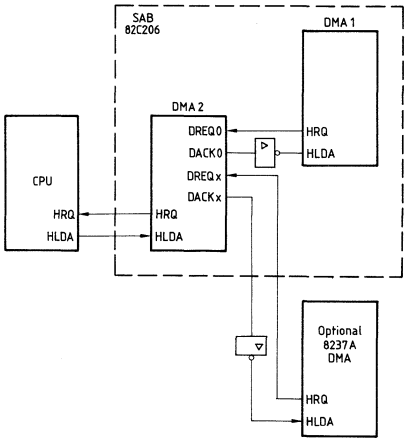
Figure 3 shows the cascade interconnection for two levels of DMA devices. Note that channel 0 of DMA2 is internally connected for cascade mode to DMA1. Additional devices can be cascaded to the available channels in either DMA1 or DMA2 since cascade is not limited to two levels of DMA controllers.

When programming cascaded controllers, begin with the device which is actually generating HRQ to the system (first level device) and then proceed to the second level devices. RESET causes the DACK outputs to become active low and are placed in the inactive state. To allow the internal cascade between DMA1 and DMA2 to function correctly, the active low state of DACK should not be modified. This is because the SAB 82C206 has an inverter between DACK0 of DMA2 and HLDA of DMA1. The first level device's DMA request mask bits will prevent second level cascaded devices from generating unwanted hold requests during the initialization process.

DMA Transfers

Four types of transfer modes are provided in the SAB 82C206 DMA subsystem. These transfer types are:

Figure 3
Cascade Mode Interconnections



Read Transfer – Read transfers move data from memory to an I/O device by generating the memory address and asserting $\overline{\text{DMAMEMR}}$ and $\overline{\text{XIOW}}$ during the same cycle.

Write Transfer – Write transfers move data from an I/O device to memory by generating the memory address and asserting $\overline{\text{XIOR}}$ and $\overline{\text{DMAMEMW}}$.

Memory-to-Memory Transfer – The memory-to-memory transfer is used to move a block of memory from one location in memory to another. DMA channels 0 and 1 may be programmed to operate as memory-to-memory channels by setting a bit in the command register. Once programmed to perform a memory-to-memory transfer the process can be started by generating either a software or an external request to channel 0. Once the transfer is initiated, channel 0 provides the address for the source block during the memory read portion of the cycle. Channel 1 generates the address for the memory write cycle. During the read cycle, a byte of data is latched in the internal temporary register of the SAB 82C206. The contents of this register are then output on the XD0-7 data lines during the write portion of the cycle and subsequently written to memory. Channel 0 may be programmed to maintain the same source address on every cycle. This allows the CPU to initialize large blocks of memory with the same value. The SAB 82C206 will continue performing transfer cycles until channel 1 reaches terminal count.

Verify Transfer – The verify transfer is a pseudo-transfer which is useful for diagnostics. In this type of transfer the DMA will operate as if it is performing a read or write transfer by generating HRQ, addresses and DACK but will do so without asserting a command signal. Since no transfer actually takes place IOCHRDY is ignored during verify transfer cycles.

Autoinitialization

Each of the four DMA channel mode registers contains a bit which will cause the channel to reinitialize after reaching terminal count. During this process, referred to an autoinitialization, the base address and base word count registers, which were originally written to by the CPU, are reloaded into the current address and current word count registers (both the base and current registers are loaded during a CPU write cycle). The base registers remain unchanged during DMA active cycles and can only be changed by the CPU. If the channel has been programmed to autoinitialize, the request mask bit will not be set upon reaching terminal count. This allows the DMA to continue operation without CPU intervention.

During memory-to-memory transfers the word count registers of both channel 0 and channel 1 must be programmed with the same starting value for full autoinitialization. If channel 0 reaches terminal count before channel 1, then channel 0 will reload the starting address and word count and continue transferring data from the beginning of the source block.

Should channel 1 reach terminal count first, it will reload the current registers and channel 0 will remain uninitialized.

DREQ Priority

The SAB 82C206 supports two schemes for establishing DREQ priority. The first is fixed priority which assigns priority based on channel position. In this method channel 0 is assigned the highest priority. Priority assignment then progresses downward through the channels in order with channel 3 receiving the lowest priority.

The second type of priority assignment is rotating priority. In this scheme the order of priority from channel 0 to channel 3 is maintained but the actual assignment of priority changes. The channel most recently serviced will be assigned the lowest priority and, since the order of priority assignment remains fixed, the remaining three channels rotate accordingly. The rotating priority assignment is illustrated in figure 4.

In instances where multiple requests occur at the same time the SAB 82C206 will issue a HRQ but will not freeze the priority logic until HLDA is returned. Once HDLA becomes active the priority logic is frozen and DACK is asserted on the highest requesting channel. Priority will not be re-evaluated until HLDA has been deactivated.

Address Generation

Eight intermediate bits of the address are multiplexed onto the data lines during active cycles of the DMA. This reduces the number of pins required by the DMA subsystem. During state S1, the intermediate addresses are output on data lines XD0-XD7. These addresses must be externally latched and used to drive the system address bus. Since DMA1 is used to transfer 8-bit data and DMA2 is used to transfer 16-bit data, a one-bit skew occurs in the intermediate address fields. DMA1 will therefore output addresses A8-A15 on the data bus at this time whereas DMA2 will output A9-A16. A separate set of latch and enable signals are provided for both DMA1 and DMA2 to accommodate the address skew.

Figure 4
Rotating Priority Scheme

First arbitration	Second arbitration	Third arbitration	Priority
Channel 0	Channel 2 — Cycle grant	Channel 3 — Cycle grant	Highest
Channel 1 — Cycle grant	Channel 3	Channel 0	
Channel 2	Channel 0	Channel 1	
Channel 3	Channel 1	Channel 2	Lowest

Channel X = Requested channel

During 8-bit DMA cycles, in which DMA1 is active, the SAB 82C206 will output the lower 8 bits of address on XA0-XA7. The intermediate 8 bits of address will be output on XD0-XD7 and ADSTB8 will be asserted for one DMA clock cycle. The falling edge of ADSTB8 is used to latch the intermediate addresses A8-A15. Enable signal $\overline{\text{AEN8}}$ is used to control the output drivers of the external latch. A16-A23 are also generated at this time from a DMA page register in the SAB 82C206. Note that A16 is output on the XA16 pin of the device.

16-bit DMA cycles from DMA2 require the SAB 82C206 to output the lower 8-bits of the address on XA1-XA8. The intermediate addresses A9-A16 are output on XD0-XD7. Control for a separate latch is provided by signals ADSTB16 and $\overline{\text{AEN16}}$. The DMA page register now generates A17-A23. During 16-bit DMA transfers XA0 and XA16 remain inactive.

The DMA page register is a set of 16 8-bit registers in the SAB 82C206 which are used to generate the high-order addresses during DMA cycles. Only 8 of the registers are actually used but all 16 were included to maintain IBM PC/AT compatibility. Each DMA channel has a register associated with it with the exception of channel 0 of DMA2 which is used for internal cascading to DMA1. Assignment of each of these registers is shown in table 3 along with its read/write address.

Table 3
DMA Address Extension Register Map

Address	Register function
080H	Unused
081H	8-bit DMA channel 2 (DACK2)
082H	8-bit DMA channel 3 (DACK3)
083H	8-bit DMA channel 1 (DACK1)
084H	Unused
085H	Unused
086H	Unused
087H	8-bit DMA channel 0 (DACK0)
088H	Unused
089H	16-bit DMA channel 2 (DACK6)
08AH	16-bit DMA channel 3 (DACK7)
08BH	16-bit DMA channel 1 (DACK5)
08CH	Unused
08DH	Unused
08EH	Unused
08FH	Refresh cycle

During demand and block transfers, the SAB 82C206 generates multiple sequential transfers. For most of these transfers the information in the external address latches will remain the same, eliminating the need to be relatched. Since the need to update the latches occurs only when a carry of borrow from the lower 8-bits of the address counter exists, the SAB 82C206 will only update the latch contents when necessary. The SAB 82C206 will therefore only execute S1 cycles when necessary, resulting in an overall throughput improvement.

Compressed Timing

The DMA subsystem in the SAB 82C206 can be programmed to transfer a word in as few as 3 DMA clock cycles. The normal DMA cycle consists of three states: S2, S3 and S4 (this assumes demand or block transfer mode). Normal transfers require 4 DMA clock cycles since S3 is executed twice due to the 1 wait state insertion. In systems capable of supporting higher throughput, the SAB 82C206 can be programmed to omit one S3 and assert both commands in S2. S2 begins the cycle by generating the address and asserting both commands. One S3 cycle is executed and the cycle terminates in S4. If compressed timing is selected, TC will be output in S2 and S1 cycles will be executed as necessary to update the address latch. Note that compressed timing is not allowed for memory-to-memory transfers.

Register Description
Current Address Register

Each DMA channel has a 16-bit current address register which holds the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes. If autoinitialization is selected, this register will be reloaded from the base address register upon reaching terminal count in the current word count register. Channel 0 can be prevented from incrementing or decrementing by setting the address hold bit in the command register.

Current Word Count Register

Each channel has a current word count register which determines the number of transfers to perform. The actual number of transfers performed will be one greater than the value programmed into the register. The register is decremented after each transfer until it goes from zero to FFFFH. When this roll-over occurs the SAB 82C206 will generate and either suspend operation on that channel and set the appropriate request mask bit or autoinitialize and continue.

Base Address Register

Associated with each current address register is a base address register. This is a write only register which is loaded by the CPU when writing to the current address register. The purpose of this register is to store the initial value of the current address register for autoinitialization. The contents of this register are loaded into the current address register whenever terminal count is reached and the autoinitialize bit is set.

Base Word Count Register

This register preserves the initial value of the current word count register. It is also a write only register which is loaded by writing to the current word count register. This register is loaded into the current word count register during autoinitialization.

Command Register

This register controls the overall operation of a DMA subsystem. The register can be read or written by the CPU and is cleared by either RESET or a master clear command.

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
DAK	DRQ	EW	RP	CT	CD	AH	M-M

DAK – DACK active level is determined by bit 7. Programming a 1 in this bit position makes DACK an active high signal.

DRQ – DREQ active level is determined by bit 6. Writing a 1 in this bit position causes DREQ to become active low.

EW – Extended write is enabled by writing a 1 to bit 5, causing the write commands to be asserted one DMA cycle earlier during a transfer. The read and write commands both begin in state S2 when enabled.

RP – Writing a 1 to bit 4 causes the SAB 82C206 to utilize a rotating priority scheme for honoring DMA requests. The default condition is fixed priority.

CT – Compressed timing is enabled by writing a 1 to bit 3 of this register. The default 0 condition causes the DMA to operate with normal timing.

CD – Bit 2 is the master disable for the DMA controller. Writing a 1 to this location disables the DMA subsystem (DMA1 or DMA2). This function is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles.

AH – Writing a 1 to bit 1 enables the address hold feature in channel 0 when performing memory-to-memory transfers.

M-M – A 1 in the bit 0 position enables channel 0 and channel 1 to be used for memory-to-memory transfers.

Mode Register

Each DMA channel has a mode register associated with it. All four mode registers reside at the same I/O address. Bits 0 and 1 of the write mode register command determine which channel's mode register will be written to. The remaining six bits control the mode of the selected channel. Each channel's mode register can be read by sequentially reading the mode register location. A clear mode register counter command is provided to allow the CPU to restart the mode read process at a known point. During mode read operations, bits 0 and 1 will both be undefined.

Msb **Lsb**

b7	b6	b5	b4	b3	b2	b1	b0
M1	M0	DEC	AI	TT1	TT0	CS1	CS0

(Read/write register)

M1-M0 – Mode selection for each channel is accomplished by bits 6 and 7.

M1	M0	MODE
0	0	Demand mode
0	1	Single cycle mode
1	0	Block mode
1	1	Cascade mode

DEC – Determines direction of the address counter. A one in bit 5 decrements the address after each transfer.

AI – The autoinitialization function is enabled by writing a 1 in bit 4 of the mode register.

TT1-TT0 – Bits 2 and 3 control the type of transfer which is to be performed.

TT1	TT0	TYPE
0	0	Verify transfer
0	1	Write transfer
1	0	Read transfer
1	1	Illegal

CS1-CS0 – Channel select bits 1 and 0 determine which channel's mode register will be written to. Read back of a mode register will result in bits 1 and 0 both being undefined.

CS1	CS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Request Register

This is a 4-bit register used to generate software requests (DMA service can be requested either externally or under software control). Request register bits can be set or reset independently by the CPU. The request mask has no effect on software-generated requests.

All four bits are read in one operation and appear in the lower four bits of the byte. Bits 4 through 7 are read as ones. All four request bits are cleared to zero by RESET.

Msb **Lsb**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	RB	RS1	RS0

(Write operation)

RB – The request bit is set by writing a 1 to bit 2. RS1-RS0 select which bit (channel) is to be manipulated.

RS1-RS0 – Channel select 0 and 1 determine which channel's request register will be written.

RS1	RS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

The format for the request register read operation is shown below.

Msb **Lsb**

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	RC3	RC2	RC1	RC0

(Read operation)

RC3-RC0 – During a request register read, the state of the request bit associated with each channel is returned in bits 0 through 3 of the byte. The bit position corresponds to the channel number.

Request Mask Register

The request mask register is a set of four bits which are used to inhibit external DMA requests from generating transfer cycles.

This register can be programmed in two ways. Each channel can be independently masked by writing to the write single mask bit location. The data format for this operation is shown below.

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	MB	MS1	MS0

(Set/reset operation)

MB – Bit 2 sets or resets the request mask bit for the channel selected by MS1 and MS0. Writing a 1 in this bit position sets the mask-bit, inhibiting external requests.

MS1-MS0 – These two bits select the specific mask bit which is to be set or reset.

MS1	MS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Alternatively all four mask bits can be programmed in one operation by writing to the write all mask bits address. Data format for this and the read all mask bits function is shown below.

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	MB3	MB2	MB1	MB0

(Read/write operation)

MB3-MB0 – Each bit position in the field represents the mask bit of a channel. The mask bit number corresponds to the channel number associated with the mask bit.

All four mask bits are set following a RESET or a master clear command. Individual channel mask bits will be set as a result of terminal count being reached, if autoinitialize is disabled. The entire register can be cleared, enabling all four channels, by performing a clear mask register operation.

Status Register

The status of all four channels can be determined by reading the status register. Information is available to determine if a channel has reached terminal count and whether an external service request is pending. Bits 0-3 of this register are cleared by RESET, master clear or each time a status read takes place. Bits 4-7 are cleared by RESET, master clear or the pending request being deasserted. Bits 4-7 are not affected by the state of the mask register bits. The channel number corresponds to the bit position.

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
DRQ3	DRQ2	DRQ1	DRQ0	TC3	TC2	TC1	TC0

(Read only register)

Temporary Register

The temporary register is used as a temporary holding register for data during memory-to-memory transfers. The register is loaded during the first cycle of a memory-to-memory transfer from XD0-XD7. During the second cycle of the transfer, the data in the temporary register is output on the XD0-XD7 pins. Data from the last memory-to-memory transfer will remain in the register unless a RESET or master clear occurs.

Special Commands

Five special commands are provided to make the task of programming the device easier. These commands are activated as a result of a specific address and assertion of either a $\overline{\text{XIOR}}$ or $\overline{\text{XIOW}}$. Information on the data lines is ignored by the SAB 82C206 whenever an $\overline{\text{XIOW}}$ activated command is issued, thus data returned on $\overline{\text{XIOR}}$ activated commands is invalid.

Clear Byte Pointer Flip-Flop – This command is normally executed prior to reading or writing to the address or word count registers. This initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write register bytes in correct sequence.

Set Byte Pointer Flip-Flop – Setting the byte pointer flip-flop allows the CPU to adjust the pointer to the high byte of an address or word count register.

Master Clear – This command has the same effect as a hardware RESET. The command register, status register, request register, temporary register, mode register counter and byte pointer flip-flop are cleared and the request mask register is set. Immediately following master clear or RESET, the DMA will be in the idle condition.

Clear Request Mask Register – This command enables all four DMA channels to accept requests by clearing the mask bits in the register.

Clear Mode Register Counter – In order to allow access to four mode registers while only using one address, an additional counter is used. After clearing the counter all four mode registers may be read by doing successive reads to the read mode register address. The order in which the registers will be read is channel 0 first, channel 3 last.

Interrupt Controller Functional Description

The programmable interrupt controllers in the SAB 82C206 function as a system wide interrupt manager. They accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector which is used as an index by the CPU to determine which interrupt service routine to execute.

A variety of priority assignment modes are provided, which can be reconfigured at any time during system operation, allowing the complete interrupt subsystem to be restructured based on the system environment.

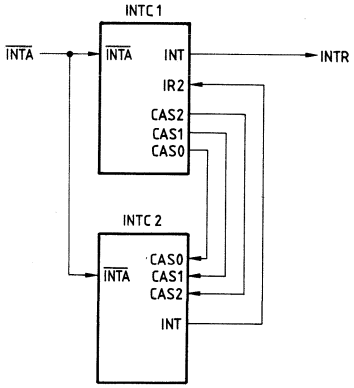
Overview

Two interrupt controllers, INTC1 and INTC2, are included in the SAB 82C206. Each of the interrupt controllers is equivalent to an 8259A device operating in the 86-Mode. The two controllers are interconnected and must be programmed to operate in cascade mode (see figure 5) for proper operation of all 16 interrupt channels. INTC1 is located at addresses 020H-021H and is configured for master operation (defined below) in cascade mode. INTC2 is a slave device (defined below) and is located at 0A0H-0A1H. The interrupt request output signal from INTC2 (INT) is internally connected to the interrupt request input channel 2 (IR2) of INTC1. The address decoding and cascade interconnection matches that of the IBM PC/AT.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of timer 0 in the counter/timer subsystem is connected to channel 0 (IR0) of INTC1. Interrupt request from the real time clock is connected to channel 0 (IR0) of INTC2. Figure 5 lists the 16 interrupt channels and their interrupt request source.

The description of the interrupt subsystem will pertain to both INTC1 and INTC2 unless otherwise noted. Wherever register addresses are used, the address for the INTC1 register will be listed first and the address for the INTC2 register will follow in parenthesis. Example: 020H (0A0H).

Figure 5
Internal Cascade Interconnections



Controller Operation

Figure 6 shows a block diagram of the major elements in the interrupt controller. The interrupt request register (IRR) is used to store requests from all of the channels which are requesting service. Interrupt request register bits are labeled using the channel name IR7-IR0. The in-service register (ISR) contains all the channels which are currently being serviced (more than one channel can be serviced at a time). In-service register bits are labeled IS7-IS0 and correspond to IR7-IR0. The interrupt mask register (IMR) allows the CPU to disable any or all of the interrupt channels. The priority resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the in-service register. During interrupt acknowledge cycles, a master controller outputs a code to the slave device which is compared in the cascade buffer/comparator with a 3-bit ID code previously written. If a match occurs in the slave controller, it will generate an interrupt vector. The contents of the vector register are used to provide the CPU with an interrupt vector during interrupt acknowledge ($\overline{\text{INTA}}$) cycles.

Interrupt Sequence

The SAB 82C206 allows the CPU to perform an indirect jump to a service routine in response to a request for service from a peripheral device. The indirect jump is based on a vector which is provided by the SAB 82C206 on the second of two CPU-generated $\overline{INTA}$ cycles (the first $\overline{INTA}$ cycle is used for resolving priority and the second cycle is for transferring the vector to the CPU). The events which occur during an interrupt sequence are as follows:

Table 4
Interrupt Request Sources

Controller number	Channel name	Interrupt request source
INTC1	IR0	Counter/timer out 0
INTC1	IR1	IRQ1 input pin
INTC1	IR2	INTC2 cascade interrupt
INTC1	IR3	IRQ3 input pin
INTC1	IR4	IRQ4 input pin
INTC1	IR5	IRQ5 input pin
INTC1	IR6	IRQ6 input pin
INTC1	IR7	IRQ7 input pin
INTC2	IR0	Real time clock IRQ
INTC2	IR1	IRQ9 input pin
INTC2	IR2	IRQ10 input pin
INTC2	IR3	IRQ11 input pin
INTC2	IR4	IRQ12 input pin
INTC2	IR5	IRQ13 input pin
INTC2	IR6	IRQ14 input pin
INTC2	IR7	IRQ15 input pin

1 – One or more of the interrupt requests (IR7-IR0) becomes active, setting the corresponding IRR bit(s).

2 – The interrupt controller resolves priority based on the state of the IRR, IMR and ISR and asserts the INTR output if appropriate.

3 – The CPU accepts the interrupt and responds with an $\overline{INTA}$ cycle.

4 – During the first $\overline{INTA}$ cycle, the highest priority ISR bit is set and the corresponding IRR bit is reset. The internal cascade address is generated and the XD7-XD0 outputs remain tristated.

5 – The CPU will excecute a second $\overline{INTA}$ cycle, during which the SAB 82C206 will drive an 8-bit vector onto the data pins XD7-XD0, which is in turn latched by the CPU. The format of this vector is shown in table 5. Note that V7-V3 in table 5 are programmable by writing to initialization control word 2 (see initialization command words section below).

6 – At the end of the second $\overline{INTA}$ cycle, the ISR bit will be cleared if the automatic end of interrupt mode is selected (see end of interrupt section). Otherwise, the ISR bit must be cleared by an end of interrupt (EOI) command from the CPU at the end of the interrupt service routine.

If no interrupt request is present at the beginning of the first $\overline{INTA}$ cycle (i.e. a spurious interrupt) INTC1 will issue an interrupt level 7 vector during the second $\overline{INTA}$ cycle.

End of Interrupt

EOI is defined as the condition which causes an ISR bit to be reset. Determination of which ISR bit is to be reset can be done by a CPU command (specific EOI) or, the priority resolver can be instructed to clear the highest priority ISR bit (non-specific EOI).

Figure 6
Interrupt Controller Block Diagram

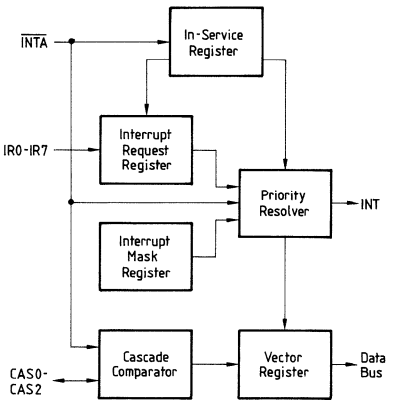
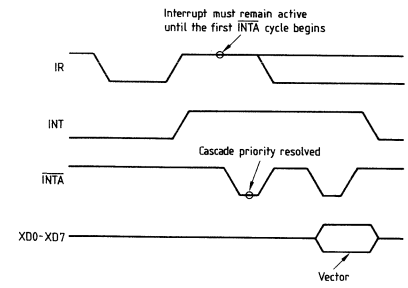


Figure 7
Interrupt Sequence



The SAB 82C206 can determine the correct ISR bit to reset when operated in modes which do not alter the fully nested structure, since the current highest priority ISR bit is necessarily the last level acknowledged and serviced. In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine. An ISR bit that is masked, in special mask mode by an IMR bit, will not be cleared by a non-specific EOI command. The interrupt controller can optionally generate an automatic end of interrupt (AEOI) on the trailing edge of the second $\overline{\text{INTA}}$ cycle.

Priority Assignment

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 has the lowest, and priority assignment is fixed (fixed priority mode). Priority assignment can be rotated either manually (specific rotation mode) or automatically (automatic rotation mode) by programming operational command word 2 (OCW2).

Fixed Priority Mode – This is the default condition which exists unless rotation (either manual or automatic) is enabled, or the controller is programmed for polled mode. In fixed priority mode, interrupts are fully nested with priority assigned as shown:

	Lowest						Highest
Priority status	7	6	5	4	3	2	1	0

Nesting allows interrupts of a higher priority to generate interrupt requests prior to the completion of the interrupt in service. When an interrupt is acknowledged, priority is resolved, the highest priority request's vector is placed on the bus and the ISR bit for that channel is set. This bit remains set until an EOI (automatic or CPU generated) is issued to that channel. While the ISR bit is set, all interrupts of equal or lower priority are inhibited. Note that a higher priority interrupt which occurs during an interrupt service routine, will only be acknowledged if the CPU has internally re-enabled interrupts.

Specific Rotation Mode – Specific rotation allows the system softare to reassign priority levels by issuing a command which redefines the lowest priority channel.

Before Rotation

	Lowest						Highest
Priority status	7	6	5	4	3	2	1	0

(Specific rotation command issued with channel 5 specified).

After Rotation

	Lowest					Highest		
Priority status	5	4	3	2	1	0	7	6

Automatic Rotation Mode – In applications where a number of equal priority peripherals are requesting interrupts, automatic rotation may be used to equalize the priority assignment. In this mode a peripheral, after being serviced, is assigned the lowest priority. All peripherals connected to the controller will be serviced at least once in 8 interrupt requests to the CPU from the controller. Automatic rotation will occur, if enabled, due to the occurrance of EOI (automatic or CPU-generated).

Before Rotation (IR4 highest priority request being serviced)

ISR status bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	1	0	0	0	0

	Lowest						Highest
Priority status	7	6	5	4	3	2	1	0

After Rotation (IR4 service completed)

ISR status bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	0	0	0	0	0

	Lowest					Highest		
Priority status	4	3	2	1	0	7	6	5

Programming the Interrupt Controller

Two types of commands are used to control the SAB 82C206 interrupt controllers, initialization command words (ICWs) and operational command words (OCWs).

Initialization Command Words

The initialization process consists of writing a sequence of 4 bytes to each interrupt controller. The initialization sequence is started by writing the first initialization command word (ICW1) to address 020H (0A0H) with a 1 on bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1 – The initialization command word counter is reset to zero.
2 – ICW1 is latched into the device
3 – Fixed priority mode is selected
4 – IR7 is assigned the highest priority
5 – The interrupt mask register is cleared
6 – The slave mode address is set to 7
7 – Special mask mode is disabled
8 – The IRR is selected for status read operations

The next three I/O writes to address 021H (0A1H) will load ICW2-ICW4. See figure 8 for a flow chart of the initialization sequence. The initialization sequence can be terminated at any point (all 4 bytes must be written for the controller to be properly initialized) by writing to address 020H (0A0H) with a 0 in data bit 4. Note, this will cause OCW2 or OCW3 to be written.

Figure 8
Initialization Sequence

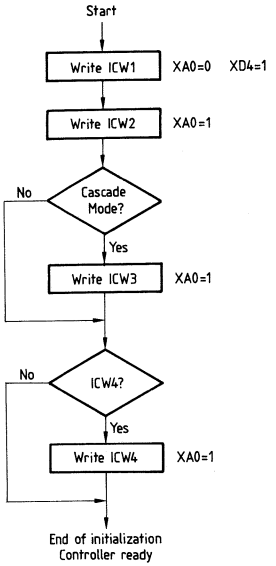


Table 5
Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	V7	V6	V5	V4	V3	1	1	1
IR6	V7	V6	V5	V4	V3	1	1	0
IR5	V7	V6	V5	V4	V3	1	0	1
IR4	V7	V6	V5	V4	V3	1	0	0
IR3	V7	V6	V5	V4	V3	0	1	1
IR2	V7	V6	V5	V4	V3	0	1	0
IR1	V7	V6	V5	V4	V3	0	0	1
IR0	V7	V6	V5	V4	V3	0	0	0

ICW1 – Address 020H (0A0H)

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	SI	LTM	X	SM	X

(Write only register)

SI – Bit 4 indicates to the interrupt controller that an initialization sequence is starting and must be a 1 to write ICW1.

LTM – Bit 3 selects level or edge triggered inputs to the IRR. If a 1 is written to LTM, a "high" level on the IRR input will generate an interrupt request. The IR must be active until the first $\overline{\text{INTA}}$ cycle is started to generate the proper interrupt vector (an IR7 vector will be generated if the IRR input is deasserted earlier) and the IR must be removed prior to EOI to prevent a second interrupt from occuring.

SM – Bit 1 selects between single mode and cascade mode. Single mode is used whenever only one interrupt controller (INTC1) is used and is not recommended for this device. Cascade mode allows the two interrupt controllers to be connected through IR2 of INTC1. INTC1 will allow INTC2 to generate its own interrupt vectors if cascade mode is selected and the highest priority IR pending is from an INTC2 input. INTC1 and INTC2 must be programmed for cascade mode for both devices to operate.

ICW2 – Address 021H (0A1H)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
V7	V6	V5	V4	V3	X	X	X

(Write only register)

V7-V3 – These bits are the upper 5 bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the priority resolver during $\overline{INTA}$ (see table 5). INTC1 and INTC2 need not be programmed with the same value in ICW2.

ICW3 Format for INTC1 – Address 021H

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
S7	S6	S5	S4	S3	S2	S1	S0

(Write only register)

S7-S0 – Select which IR inputs have slave mode controllers connected. ICW3 in INTC1 must be written with a 04H for INTC2 to function.

ICW3 Format for INTC2 – Address 0A1H

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	ID2	ID1	ID0

(Write only register)

ID2-ID0 – Determine the slave mode address the controller will respond to during the cascaded $\overline{INTA}$ sequence. ICW3 in INTC2 should be written with a 02H for cascade mode operation. Note, b7-b3 should be zero.

ICW4 – Address 021H (0A1H)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	EMI	X	X	AEOI	X

(Write only register)

EMI – Bit 4 will enable multiple interrupts from the same channel in fixed priority mode. This allows INTC2 to fully nested interrupts, when cascade mode with fixed priority mode are both selected, without being blocked by INTC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to INTC2 and check its in-service register for zero, when exciting an interrupt service routine. If zero, a non-specific EOI command should be sent to INTC1. If non-zero, no command is issued.

AEOI – Auto end of interrupt is enabled when ICW4 is written with a one in bit 1. The interrupt controller will perform a non-specific EOI on the trailing edge of the second $\overline{INTA}$ cycle. Note, this function should not be used in a device with fully nested interrupts unless the device is a cascade master.

Operational Command Words

Operational command words (OCWs) allow the SAB 82C206 interrupt controllers to be controlled or reconfigured at any time while operating. Each interrupt has 3 OCWs which can be programmed to effect the proper operating configuration and a status register to monitor controller operation.

Operational command word 1 (OCW1) is located at address 021H (0A1H) and may be written any time the controller is not in initialization mode. Operational command words 2 and 3 (OCW2, OCW3) are located at address 020H (0A0H). Writing to address 020H (0A0H) with a 0 in bit 4 will place the controller in operational mode and load OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

OCW1 – Address 021H (0A1H)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
M7	M6	M5	M4	M3	M2	M1	M0

(Read/write register)

M7-M0 – These bits control the state of the interrupt mask register. Each interrupt request can be masked by writing a 1 in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no affect on lower priority requests. All IMR bits are cleared by writing ICW1.

OCW2 – Address 020H (0A0H)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
R	SL	EOI	SI	2/3	L2	L1	L0

(Write only register)

R – This bit in conjunction with SL and EOI selects operational function. Writing a 1 in bit 7 causes one of the rotate functions to be selected.

R	SL	EOI	Function
0	0	0	Rotate on auto EOI disable
0	0	1	Non-specific EOI command
0	1	0	No operation
0	1	1	Specific EOI command
1	0	0	Rotate on auto EOI enable
1	0	1	Rotate on non-specific EOI
1	1	0	Specific rotate command
1	1	1	Rotate on specific EOI

SL – This bit in conjunction with R and EOI selects operational function. Writing a 1 in this bit position causes a specific or immediate function to occur. All specific commands require L2-L0 to be valid except no operation.

EOI – This bit in conjunction with R and SL selects operational function. Writing a 1 in this bit position causes a function related to EOI to occur.

SI – Writing a 0 in this bit position takes the interrupt controller out of initialize mode and writes OCW2 or OCW3.

2/3 – If the I/O write places a 0 in bit 4 (SI), then writing a 0 in bit 3 (2/3) selects OCW2 and writing a 1 will select OCW3.

L2-L0 – These three bits are internally decoded to select which interrupt channel is to be affected by the specific command. L2-L0 must be valid during three of the four specific cycles (see SL).

OCW3 – Address 020H (0A0H)

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
0	ESMM	SMM	SI	2/3	PM	RR	RIS

(Write only register)

ESMM – Writing a 1 in this bit position enables the set/reset special mask mode function controlled by bit 5 (SMM). ESMM allows the other functions in OCW3 to be accessed and manipulated without affecting the special mask mode state.

SMM – If ESMM and SMM both are written with a 1 the special mask mode is enabled. Writing a 1 to ESMM and a 0 to SMM disables special mask mode. During special mask mode, writing a 1 to any bit position inhibits interrupts and a 0 enables interrupts on the associated channel by causing the priority resolver to ignore the condition of the ISR.

SI – See SI on the left.

2/3 – See 2/3 on the left.

PM – Polled mode is enabled by writing a 1 to bit 2 of OCW3, causing the SAB 82C206 to perform the equivalent of an $\overline{\text{INTA}}$ cycle during the next I/O read operation to the controller. The byte read during this cycle will have bit 7 set if an interrupt is pending. If bit 7 of the byte is set, the level of the highest pending request will be encoded on bits 2-0. The IRR will remain frozen until the read cycle is completed at which time the PM bit is reset.

RR – When the RR bit (bit 1) is 1, reading the status port at address 020h (0A0h) will cause the contents of IRR or ISR (determined by RIS) to be placed on XD7-XD0. Asserting PM forces RR to be reset.

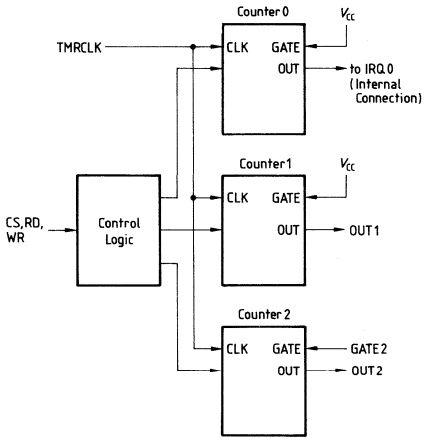
RIS – This bit selects between the IRR and the ISR during status read operations if RR = 1.

Counter/Timer

The counter/timer (CTC) in the SAB 82C206 is general purpose, and can be used to generate accurate time delays under software control. The CTC contains three 16-bit counters (counter 0-2) which can be programmed to count in binary or binary coded decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter.

All three of the counters shown in figure 9 are controlled from a common set of control logic. The control logic decodes control information written to the CTC and provides the controls necessary to load, read, configure and control each counter. Counter 0 and counter 1 can be programmed for all six modes, but mode 1 and mode 5 have limited usefulness due to the absence of an external hardware trigger signal. Counter 2 can be operated in any of the six modes listed in the following.

Figure 9
Counter/Timer Block Diagram



Mode 0 Interrupt on terminal count
Mode 1 Hardware retriggerable one-shot
Mode 2 Rate generator
Mode 3 Square wave generator
Mode 4 Software triggered strobe
Mode 5 Hardware retriggerable strobe

All three counters in the CTC are driven from a common clock input pin (TMRCLK) which is independent from other clock inputs to the SAB 82C206. Counter 0's output (OUT0) is connected to IR0 of INTC1 (see interrupt controller, functional description) and may be used as an interrupt to the system for time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third counter (counter 2) is a full function counter/timer. This channel can be used as an interval timer, a counter, or as a gated rate/pulse generator.

Counter Description

Each counter in the CTC contains a control register, a status register, a 16-bit counting element (CE), a pair of 8-bit counter input latches (CIL, CIH), and a pair of 8-bit counter output latches (COL, COH). Each counter also has a clock input for loading and decrementing the CE, a mode defined GATE input for controlling the counter (only GATE2 is externally accessible), and an OUT signal (OUT0 is not externally accessible). The OUT signal's state and function are controlled by the counter mode and condition of the CE (see mode definitions).

The control register stores the mode and command information used to control the counter. The control register may be loaded by writing a byte, containing a pointer to the desired counter, to the write control word address (043H). The remaining bits in the byte contain the mode, the type of command, and count format information.

The status register allows the software to monitor counter condition and read back the contents of the control register.

The counting element is a loadable 16-bit synchronous down counter. The CE is loaded or decremented on the falling edge of TMRCLK. The CE contains the maximum count when a 0 is loaded, which is equivalent to 65536 in binary operation or 10000 in BCD. The CE does not stop when it reaches 0. In modes 2 and 3 the CE will be reloaded and in all other modes it will wrap around to FFFF in binary operation or to 9999 in BCD operation.

The CE is indirectly loaded by writing one or two bytes (optional) to the counter input latches, which are in turn loaded into the CE. This allows the CE to be loaded or reloaded in one TMRCLK cycle.

The CE is also read indirectly by reading the contents of the counter output latches. COL and COH are transparent latches which can be read while transparent or latched (see latch counter command).

Programming the CTC

After power-up the condition of CTC control registers, counter registers, CE, and the output of all counters is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a control word and then read/write an initial count. The control register of a counter is written by writing to the control word address (see table 10). The control register is a write only location.

Control Word – (043H)

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
F3	F2	F1	F0	M2	M1	M0	BCD

(Write only register)

F3-F0 – Bits 7-4 determine the command to be performed.

M2-M0 – Bits 3-1 determine the counter's mode during read/write counter commands (see read/write counter command) or select the counter during a read-back command (see read back command). Bits 3-1 become "don't cares" during latch counter commands.

BCD – Bit 0 selects binary coded decimal counting format during read/write counter commands. Note, during read back command this bit must be 0.

Table 10
Counter/Timer Address Map

Address	Function
040H	Counter 0 read/write
041H	Counter 1 read/write
042H	Counter 2 read/write
043H	Control register write only

Read/Write Counter Command

When writing to a counter, two conventions must be observed:

1 – Each counter's control word must be written before the initial count is written.

2 – Writing the initial count must follow the format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count can be written into the counter at any time after programming without rewriting the control word providing the programmed format is observed.

During read/write counter commands M3-M0 are defined as follows:

M2	M1	M0	Function
0	0	0	Select mode 0
0	0	1	Select mode 1
X	1	0	Select mode 2
X	1	1	Select mode 3
1	0	0	Select mode 4
1	0	1	Select mode 5

Latch Counter Command

When a latch counter command is issued, the counter's output latches (COL, COH) latch the current state of the CE. COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition the latches are enabled and the contents of the CE may be read directly.

F3	F2	F1	F0	Command
0	0	0	0	Latch counter 0 (see counter latch command)
0	0	0	1	Read/write counter 0 Lsb only
0	0	1	0	Read/write counter 0 Msb only
0	0	1	1	Read/write counter 0 Lsb then Msb
0	1	0	0	Latch counter 1 (see counter latch command)
0	1	0	1	Read/write counter 1 Lsb only
0	1	1	0	Read/write counter 1 Msb only
0	1	1	1	Read/write counter 1 Lsb then Msb
1	0	0	0	Latch counter 2 (see counter latch command) 2
1	0	0	1	Read/write counter 2 Lsb only
1	0	1	0	Read/write counter 2 Msb only
1	0	1	1	Read/write counter 2 Lsb then Msb
1	1	X	X	Read back command (see counter read back command)

Latch counter commands may be issued to more than one counter before reading the first counter to which the command was issued. Also, multiple latch counter commands issued to the same counter without reading the counter will cause all but the first command to be ignored.

Read Back Command

The read back command allows the user to check the count value, mode, and state of the OUT signal and null count flag of the selected counter(s).

The format of the read-back command is:

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
1	1	LC	LS	C2	C1	C0	0

LC – Writing a 0 in bit 5 causes the selected counter(s) to latch the state of the CE in COL and COH.

LS – Writing a 0 in bit 4 causes the selected counter(s) to latch the current condition of its control register, null count and output into the status register. The next read of the counter will result in the contents of the status register being read (see status read).

C2-C0 – Writing a 1 in bit 3 causes counter 3 to latch one or both of the registers specified by LC and LS. The same is true for bits 2 and 1 except that they enable counters 1 and 0 respectively.

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed.

If LS=LC=0, status will be returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter result in the count being returned.

Status Byte

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
OUT	NC	F1	F0	M2	M1	M0	BCD

OUT – Bit 7 contains the state of the OUT signal of the counter.

NC – Bit 6 contains the condition of the null count flag. This flag is used to indicate that the contents of the CE are valid. NC will be set to a 1 during a write to the control register or the counter. NC is cleared to a 0 whenever the counter is loaded from the counter input registers.

F1-F0 – Bits 5-4 contain the F1 and F0 command bits which were written to the command register of the counter during initialization. This information is useful in determining whether the high byte, the low byte or both must be transferred during counter read/write operations.

M2-M0 – These bits reflect the mode of the counter and are interpreted in the same manner as in write command operations.

BCD – Bit 0 indicates that the CE is operating in BCD format.

Counter Operation

Due to the previously stated restrictions in counter 0 and counter 1, counter 2 will be used as in the example describing counter operation, but the description of mode 0, 2, 3 and 4 is relevant to all counters.

The following terms are defined for describing CTC operation.

TMRCLK pulse – A rising edge followed by a falling edge of the SAB 82C206 TMRCLK input.

Trigger – The rising edge of the GATE2 input.

Counter load – The transfer of the 16-bit value in CIL and CIH to the CE.

Initialized – A control word written and the counter input latches loaded.

Counter 2 operates in one of the following modes.

Mode 0 – Interrupt on terminal count

Writing the control word causes OUT2 to go low and remain low until the CE reaches 0, at which time it goes back high and remains high until a new count or control word is written. Counting is enabled when GATE2=1. Disabling the count has no effect on OUT2.

The CE is loaded with the first TMRCLK pulse after the control word and initial count are loaded. When both CIL and CIH are written, the CE is loaded after CIH is written (see write operations). This TMRCLK pulse does not decrement the count, so for an initial count of N, OUT2 does not go high until N+1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the CE on the next TMRCLK pulse and counting continues from the new count.

If an initial count is written with GATE2=0, it will still be loaded on the next TMRCLK pulse but counting does not begin until GATE2=1. OUT2, therefore, goes high N TMRCLK pulses after GATE2=1.

Mode 1 – Hardware retriggerable one-shot

Writing the control word causes OUT2 to go high initially. Once initialized the counter is armed and a trigger causes OUT2 to go low on the next TMRCLK pulse. OUT2 then remains low until the counter reaches 0. An initial count of N results in a one-shot pulse N TMRCLK cycles long.

Any subsequent triggers while OUT2 is low cause the CE to be reloaded, extending the length of the pulse. Writing a new count to CIL and CIH will not affect the current one-shot unless the counter is retriggered.

Mode 2 – Rate generator

Mode 2 functions as a divide-by-N counter, with OUT2 as the carry. Writing the control word during initialization sets OUT2 high.

When the initial count is decremented to 1, OUT2 goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high, reloads the CE and the process is repeated. In mode 2 the counter continues counting (if GATE2=1) and will generate an OUT2 pulse every N TMRCLK cycles. Note that a count of 1 is illegal in mode 2.

GATE2=0 disables counting and forces OUT2 high immediately. A trigger reloads the CE on the next TMRCLK pulse. Thus GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not affect the current operation unless a trigger is received. Otherwise, the new count will be loaded at the end of the current counting cycle.

Mode 3 – Square wave generator

Mode 3 is similar to mode 2 in every respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an even count, the duty cycle of OUT2 will be 50% (high=low=N/2). For odd count values. OUT2 is high one TMRCLK cycle longer than it is low. Therefore, high = (N+1)/2 and low=(N-1)/2.

Mode 4 – Software triggered strobe

Writing the control word causes OUT2 to go high initially. Expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2=0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. The CE begins decrementing one TMRCLK pulse later. OUT2 will go low for one TMRCLK cycle, (N+1) cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be "retriggerable" by software.

Mode 5 – Hardware triggered strobe

Writing the control word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting.

The CE is loaded on the TMRCLK pulse after a trigger. Since loading the CE inhibits decrementing, OUT2 will go low for one TMRCLK cycle (N+1) TMRCLK cycles after the trigger.

If a new count is loaded during counting, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter "retriggerable".

GATE2

In modes 0, 2, 3 and 4 GATE2 is level sensitive and is sampled on the rising edge of TMRCLK. In modes 1, 2, 3 and 5 the GATE2 input is rising-edge sensitive. This rising edge sets an internal flip-flop whose output is sampled on the next rising edge of TMRCLK. The flip-flop resets immediately after being sampled. Note that in modes 2 and 3 the GATE2 input is both edge and level sensitive.

Table 11
Gate Pin Functions

Mode	Condition		
	Low	Rising	High
0	Disables counting	–	Enables counting
1	–	a) Initiates counting b) Resets out pin	–
2	a) Disables counting b) Forces out pin high	Initiates counting	Enables counting
3	a) Disables counting b) Forces out pin high	Initiates counting	Enables counting
4	Disables counting	–	Enables counting
5	–	Initiates counting	–

Real Time Clock

Functional Description

This section of the SAB 82C206 combines a complete time-of-day clock with alarm facility, one-hundred-year calendar, a programmable periodic interrupt, and 114 bytes of low-power static RAM. Provisions are made to enable the device to operate in a low power (battery-powered) mode and protect the contents of both the RAM and clock during system power-up and power-down.

Register Access

Reading and writing to the 128 locations in the real time clock is accomplished by first placing the index address of the location you wish to access on the data input pins XD0-XD6 and then strobing the AS input pin. The address will then be latched into the index address register on the falling edge of AS. The index address register is then used as a pointer to the specific byte in the real time clock, which may be read or written to by asserting $\overline{\text{XIOR}}$ or $\overline{\text{XIOW}}$ with an address on the XA9-XA0 inputs of 071H.

Since AS will most likely be generated by an I/O operation which will result in the assertion of $\overline{\text{XIOW}}$, it is recommended that an address of 070H be applied to the XA9-XA0 inputs during this time. This will prevent the modification of other registers in the SAB 82C206.

Address Map

Table 12 illustrates the internal register RAM organization of the real time clock portion of the SAB 82C206. The 128 addressable locations in the real time clock are divided into 10 bytes which normally contain the time, calendar, and alarm data, four control and status bytes and 114 general purpose RAM bytes. All 128 bytes are readable by the CPU. The CPU may also write to all locations except registers C, D, bit 7 of register A and bit 7 of the seconds byte which is always 0.

Table 12
Address Map for Real Time Clock

Index	Function
00	Seconds
01	Seconds alarm
02	Minutes
03	Minutes alarm
04	Hours
05	Hours alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Register A
0B	Register B
0C	Register C
0D	Register D
0E	User RAM
0F . . . 7E	User RAM User RAM
7F	User RAM

Time Calendar and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the real time clock. Initialization of the time, calendar and alarm information is accomplished by writing to these locations. Information is stored in these locations in binary-coded decimal (BCD) format.

Before initialization of the internal registers can be performed, the SET bit in register B should be set to a "1" to prevent real time clock updates from occuring. The CPU then initializes the first 10 locations in BCD format. The SET bit should then be cleared to allow updates. Once initialized and enabled, the real time clock will perform clock/calendar updates at a 1 Hz rate.

Table 13
Time, Calendar, Alarm Data Format

Index register address	Function	BCD range
0	Seconds	00-59
1	Seconds alarm	00-59
2	Minutes	00-59
3	Minutes alarm	00-59
4	Hours (12-hour mode) Hours (24-hour mode)	01-12 (AM) 81-92 (PM) 00-23
5	Hours alarm (12-hour mode) Hours alarm (24-hour-mode)	01-12 (AM) 81-92 (PM) 00-23
6	Day of week	01-07
7	Day of month	01-31
8	Month	01-12
9	Year	00-99

Table 13 shows the format for the ten clock, calendar and alarm locations. The 24/12 bit in register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initialization the 24/12 bit cannot be changed without reinitializing the hour locations. In 12-hour format the high-order bit of the hours byte in both the time and alarm bytes will indicate PM when it is a "1".

During updates, which occur once per second, the 10 bytes of time, calendar and alarm information are unavailable to be read or written by the CPU for a period of 2 ms. These 10 locations cannot be written during this time. Information read while the real time clock is performing an update will be undefined. The update cycle section shows how to avoid update cycle/CPU contention problems.

The alarm bytes can be programmed to generate an interrupt at a specific time or a periodic interrupt. To generate an interrupt at a specific time, the user only needs to program the time at which the interrupt is to occur into the 3 alarm bytes. Alternatively, a periodic interrupt can be generated by setting the two high-order bits in an alarm register to a "1", which turns that byte into a "don't care". For instance, an interrupt can be generated every hour by programming a C0H into register 5, or an interrupt can be generated once a second by programming the same value into all three alarm registers.

Static RAM

The 114 bytes of RAM from index address 0EH to 7FH are not affected by the real time clock. These bytes are accessable during the update cycle and may be used for whatever the designer wishes. Typical applications will use this as nonvolatile storage for configuration and calibration parameters since this device is normally battery-powered when the system is turned off.

Control and Status Registers

The SAB 82C206 contains four registers used to control the operation and monitor the status of the real time clock. These registers are located at index address 0AH-0DH and are accessable by the CPU at all times.

Register A (0AH)

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

(Read/write register except UIP)

UIP – Update in progress flag is a status bit used to indicate when an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP will go active (High) 224 µs prior to the start of an update cycle and will remain active for an additional 2 ms while the update is taking place. The UIP bit is read only and is not affected by reset. Writing a "1" to the SET bit in register B will clear the UIP status bit.

DV2-DV0 – These three bits are used to control the divider/prescaler on the real time clock. While the SAB 82C206 can operate at frequencies higher than 32.768 kHz, this is not recommended for battery powered operation due to the increased power consumption at these higher frequencies.

Divider Options

DV2	DV1	DV0	Osc. freq.	Mode
0	0	0	4.194304 MHz	Operate
0	0	1	1.048576 MHz	Operate
0	1	0	32.768 KHz	Operate
1	1	X	Reset divider	

RS3-RS0 – These four bits control the periodic interrupt rate. The periodic interrupt is derived from the divider/prescaler in the real time clock and is separate from the alarm interrupt. Both the alarm and periodic interrupts do, however, use the same interrupt channel in the interrupt controller. Use of the periodic interrupt allows the generation of interrupts at rates higher than once per second. On the next page there are the interrupt rates for which the real time clock can be programmed.

Periodic Interrupt Rate

Rate selection				Time base	
RS3	RS2	RS1	RS0	4.194304 MHz 1.048576 MHz	32.768 KHz
0	0	0	0	None	None
0	0	0	1	30.517 µs	3.90526 ms
0	0	1	0	61.035 µs	7.8125 ms
0	0	1	1	122.070 µs	122.070 µs
0	1	0	0	244.141 µs	244.141 µs
0	1	0	1	488.281 µs	488.281 µs
0	1	1	0	976.562 µs	976.562 µs
0	1	1	1	1.953125 ms	1.953125 ms
1	0	0	0	3.90625 ms	3.90625 ms
1	0	0	1	7.8125 ms	7.8125 ms
1	0	1	0	15.625 ms	15.625 ms
1	0	1	1	31.25 ms	31.25 ms
1	1	0	0	62.5 ms	62.5 ms
1	1	0	1	125 ms	125 ms
1	1	1	0	250 ms	250 ms
1	1	1	1	500 ms	500 ms

Register B (0BH)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	0	0	24/12	DSE

(Read/write register)

SET – Writing a "0" to this bit enables the update cycle and allows the real time clock to function normally. When set to a "1" the update cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by the RESET input pin.

PIE – The periodic interrupt enable bit controls the generation of interrupts based on the value programmed into the RS3-RS0 bits of register A. This allows the user to disable this function without affecting the programmed rate. Writing a "1" to this bit enables the generation of periodic interrupts. This bit is cleared to a "0" by RESET.

AIE – The generation of alarm interrupts is enabled by setting this bit to a "1". Once this bit is enabled the real time clock will generate an alarm whenever a match occurs between the programmed alarm and clock information. If the don't care condition is programmed into one or more of the alarm registers, this will enable the generation of periodic interrupts at rates of one second or greater. This bit is cleared by RESET.

UIE – The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-ended interrupt flag (UF) bit in register C to assert an interrupt. This bit is cleared by SET = 1 or RESET.

24/12 – The 24/12 control bit is used to establish the format of both the hours and hours alarm bytes. If this bit is a "1", the real time clock will interpret and update the information in these two bytes using the 24 hour mode. This bit can be read or written by the CPU and is not affected by RESET.

DSE – The real time clock can be instructed to handle daylight saving time changes by setting this bit to a "1". This enables two exceptions to the normal time keeping sequence to occur on the last Sunday in April a.m. Setting this bit to a "0" disables the execution of these two exceptions. $\overline{\text{PSRSTB}}$ has no effect on this bit.

Register C (0CH)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

(Read only register)

IRQF – The interrupt request flag bit is set to a "1" when any of the conditions which can cause an interrupt is true and the interrupt enable for that condition is true. The condition which causes this bit to be set, also generates an interrupt. The logic expression for this flag is:

IRQF = PF & PIE
+ AF & AIE
+ UF & UIE

This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB input pin. Writing to this register has no effect on the contents.

PF – The periodic interrupt flag is set to a "1" when a transition, which is selected by RS3-RS0, occurs in the divider chain. This bit will become active, independent of the condition of the PIE control bit. The PF bit will then generate an interrupt and set IRQF if PIE is a "1".

AF – A "1" appears in the AF bit whenever a match has occurred between the time registers and alarm registers during an update cycle. This flag is also independent of its enable (AIE) and will generate an interrupt if AIE is true.

UF – The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is set to "1" the "1" in UF causes the IRQF bit to be a "1", generating an interrupt. UF is cleared by a register C read or a RESET.

Register D (0DH)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

(Read only register)

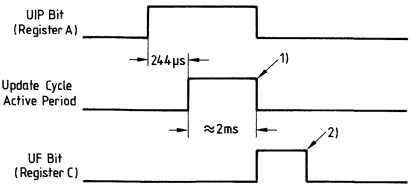
VRT – The valid RAM and time bit indicates the condition of the contents of the real time clock. This bit is cleared to a "0" whenever the $\overline{\text{PSRSTB}}$ input pin is low. This pin is normally derived from the power supply which supplies V_{CC} to the device and will allow the user to determine whether the registers have been initialized since power was applied to the device. VRT has no effect on this bit and it can only be set by reading register D. All unused register bits will be "0" when read and are not writable.

Update Cycle

During normal operation the real time clock will perform an update cycle once every second. The performance of an update cycle is contingent upon the divider bits DV2-DV0 not being cleared, and the SET bit in register B cleared. The function of the update cycle is to increment the clock/calendar registers and compare them to the alarm registers. If a match occurs between the two sets of registers, an alarm is generated and an interrupt will be issued if the alarm and interrupt control bits are enabled.

During the time that an update is taking place, the lower 10 registers are unavailable to the CPU. This is done to prevent the possible corruption of data in the registers or the reading of incorrect data. To avoid contention problems between the real time clock and the CPU, a flag is provided in register A to alert the user of an impending update cycle. This update in process bit (UIP) is asserted 244 µs before the actual start of the cycle and is maintained until the cycle is complete. Once the cycle is complete the UIP bit will be cleared and the update-ended interrupt flag (UF) in register C will be set. Figure 10 illustrates the update cycle. CPU access is always allowed to registers A through D during update cycles.

Figure 10
Update Cycle



Note:
1. Register 0-9 are unavailable to be read or written during this time.
2. If bit cleared by CPU read of register C.

Two methods for reading and writing to the real time clock are recommended. Both of these methods will allow the user to avoid contention between the CPU and the real time clock for access to the time and date information.

The first method is to read register A, determine the state of the UIP bit and if it is "0", perform the read or write operation. For this method to work successfully the entire read or write operation (including any interrupt service routines which might occur) must not require more than 244 µs to complete from the beginning of the read of register A to the completion of the last read or write operation to the clock calendar registers.

The second method of accessing the lower 10 registers is to read register C once and disregard the contents. Then subsequently continue reading this register until the UF bit is a "1". This bit will become true immediately after an update has been completed. The user then has to complete a read or write operation until the start of the next update cycle.

Power-Up/Down

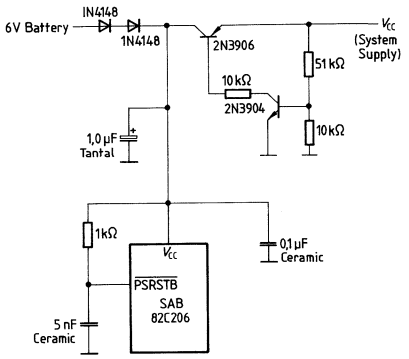
Most applications will require the real time clock to remain active whenever the system power is turned off. To accomplish this the user must provide an alternative source of power to the SAB 82C206. This alternative source of power is normally provided by connecting a battery to the V_{CC} supply pin of the device. A means should be provided to switch from the system power supply to the battery. A circuit such as the one shown in Figure 11 may be used to eliminate power drain on the battery when the entire SAB 82C206 is active. The circuit shown here will allow for reliable transitions between system and battery power without undue battery power drain.

The user should also ensure that the V_{IN} maximum specification is never exceeded when powering the system up or down. Failure to observe this specification may result in damage to the device.

A pin is provided on the device to protect the contents of the real time clock and reduce power consumption whenever the system is powered down. This pin (PWRGD) should be low whenever the system power supply is not within specifications for proper operation of the system. This signal may be generated by circuitry in either the power supply or on the system board. The PWRGD input will disable all unnecessary inputs during the time the system is powered down to prevent noise on the inactive pins from causing increased I_{CC}. This pin must therefore be inactive for the remainder of the device to operate properly when system power is applied.

One pin is provided to initialize the device whenever power is applied to the SAB 82C206. This pin ($\overline{PSRSTB}$) will not alter the RAM or clock/calendar contents but it will initialize the necessary control register bits. (See pin description for a list of the control register bits affected by $\overline{PSRSTB}$). Assertion of $\overline{PSRSTB}$ disables the generation of interrupts and sets a flag indicating that the contents of the device may not be valid. A recommended circuit for controlling the $\overline{PSRSTB}$ input is also shown in figure 11.

Figure 11
Power Conversion and Reset Circuitry



Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Supply voltage	−0.5 V to + 7.0 V
Voltage on any pin with respect to ground	−0.5 V to V_{CC} + 0.5 V
Power dissipation	1 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ±5%; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage	V_{IL}	−0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC}+0.5	V	–
Output low voltage	V_{OL}	–	0.4	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = −2.0 mA
Input leakage current	I_{IL}	−10	10	µA	V_{IN} = V_{CC} to 0 V
Output leakage current	I_{OL}	−10	10	µA	V_{OUT} = V_{CC} to 0.45
V_{CC} supply current	I_{CC}	–	30	mA	SCLK freq. = 8 MHz
V_{CC} standard supply current	I_{CCSB}	–	10	µA	SCLK freq. = DC

Capacitance [1)]

T_A = 25°C, V_{CC} = GND = 0 V

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input capacitance	C_{IN}	–	10	pF	f_C = 1 MHz Unmeasured pins returned to GND
I/O capacitance	C_{IO}	–	20	pF	
Output capacitance	C_{OUT}	–	20	pF	

[1)] This parameter is periodically sampled and not 100% tested.

AC Characteristics

T_A = 0°C to 70°C; V_{CC} = +5V ±5%; GND = 0V

Parameter	Symbol	Limit values		Unit
		min.	max.	
Address setup to command active	t_1	25	–	ns
Command active period	t_2	200	–	ns
Address hold time from command inactive	t_3	0	–	ns
Data valid delay	t_4	160	–	ns
Data hold time from $\overline{\text{XIOR}}$/$\overline{\text{INTA}}$ inactive	t_5	10	–	ns
XD0-XD7 active from $\overline{\text{XIOR}}$/$\overline{\text{INTA}}$	t_6	5	40	ns
Data setup to $\overline{\text{XIOW}}$ inactive	t_7	160	–	ns
Data hold time from $\overline{\text{XIOW}}$ inactive	t_8	0	–	ns
Command recovery time	t_9	120	–	ns
Interrupt request width (low)	t_{10}	100	–	ns
Interrupt request width (high)	t_{11}	200	–	ns
INT output delay	t_{12}	–	300	ns
IOCHRDY delay from $\overline{\text{XIOR}}$/$\overline{\text{XIOW}}$ active	t_{13}	–	TBD	ns
IOCHRDY delay from SCLK	t_{14}	–	TBD	ns
Real time clock cycle time	t_{20}	–	500	ns
AS pulse width	t_{21}	160	–	ns
Data valid setup to AS inactive	t_{22}	160	–	ns
Data hold time from AS inactive	t_{23}	0	–	ns
OSCI period	t_{24}	500	–	ns
OSCI high time	t_{25}	200	–	ns
OSCI low time	t_{26}	200	–	ns
$\overline{\text{PSRSTB}}$ high delay from V_{CC}	t_{27}	5	–	µs
$\overline{\text{PSRSTB}}$ low pulse width	t_{28}	5	–	µs
VRT bit valid delay	t_{29}	–	2	µs
TMRCLK period	t_{40}	125	DC	ns
TMRCLK low time	t_{41}	50	–	ns
TMRCLK high time	t_{42}	50	–	ns
GATE2 setup to TMRCLK	t_{43}	50	–	ns
GATE2 hold time from TMRCLK	t_{44}	50	–	ns

AC Characteristics (cont'd)

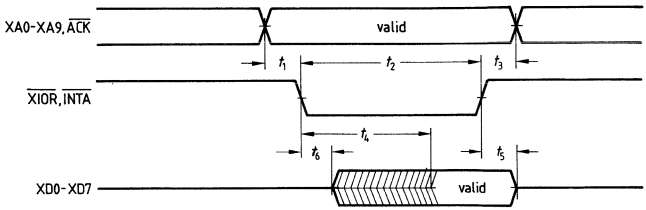
Parameter	Symbol	Limit values		Unit
		min.	max.	
GATE2 low time	t_{45}	50	–	ns
GATE2 high time	t_{46}	50	–	ns
OUT2 delay from TMRCLK	t_{47}	–	120	ns
OUT2 delay from GATE2	t_{48}	–	120	ns
SCLK period (DMA clock = SCLK)	t_{50}	125	–	ns
SCLK period (DMA clock = SCLK/2	t_{50A}	62	–	ns
SCLK low time (DMA clock = SCLK)	t_{51}	43	–	ns
SCLK low time (DMA clock = SCLK/2)	t_{51A}	22	–	ns
SCLK high time (DMA clock = SCLK)	t_{52}	55	–	ns
SCLK high time (DMA clock = SCLK/2)	t_{52A}	27	–	ns
DREQx setup to SCLK	t_{53}	0	–	ns
HRQ valid from SCLK	t_{54}	–	75	ns
HLDA setup to SCLK	t_{55}	45	–	ns
$\overline{\text{AENx}}$ valid delay from SCLK	t_{56}	–	105	ns
$\overline{\text{AENx}}$ invalid delay from SCLK	t_{57}	TBD	80	ns
ADSTBx valid delay from SCLK	t_{58}	–	70	ns
ADSTBx invalid delay from SCLK	t_{59}	–	70	ns
XD0-XD7 active delay from SCLK	t_{60}	–	60	ns
XD0-XD7 valid setup to ADSTBx low	t_{61}	65	–	ns
XD0-XD7 hold time from ADSTBx low	t_{62}	25	–	ns
XD0-XD7 tristate delay from SCLK	t_{63}	–	135	ns
Address valid delay from SCLK	t_{64}	–	60	ns
Address hold time from $\overline{\text{DMAMEMR}}$ high	t_{65}	50	–	ns
Address tristate delay from SCLK	t_{66}	–	55	ns
DACKx delay from SCLK	t_{67}	–	105	ns
Command enable delay from SCLK	t_{68}	–	90	ns
Command active delay from SCLK	t_{69}	–	120	ns
Write command inactive delay from SCLK	t_{70}	–	80	ns
Address hold time from write high	t_{71}	75	–	ns
Command tristate delay from SCLK	t_{72}	–	75	ns

AC Characteristics (cont'd)

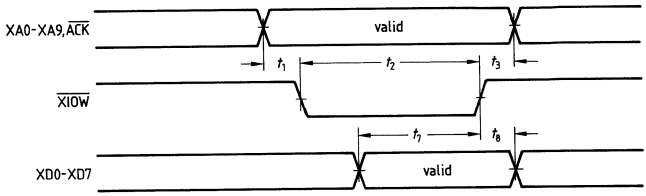
Parameter	Symbol	Limit values		Unit
		min.	max.	
Read command inactive delay from SCLK	t_{73}	–	115	ns
TC delay from SCLK	t_{74}	–	60	ns
XD0-XD7	t_{75}	90	–	ns
XD0-XD7 hold from read command inactive	t_{76}	0	–	ns
XD0-XD7 valid delay from SCLK	t_{77}	–	120	ns
XD0-XD7 hold from write inactive	t_{78}	15	–	ns
IOCHRDY input setup to SCLK	t_{79}	35	–	ns
IOCHRDY input hold time from SCLK	t_{80}	20	–	ns
RESET pulse width	t_{81}	TBD	–	ns
First $\overline{\text{XIOR}}/\overline{\text{XIOW}}$ active after RESET	t_{82}	TBD	–	ns

Waveforms

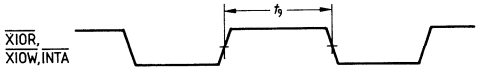
Peripheral Read/$\overline{\text{INTA}}$ Cycle



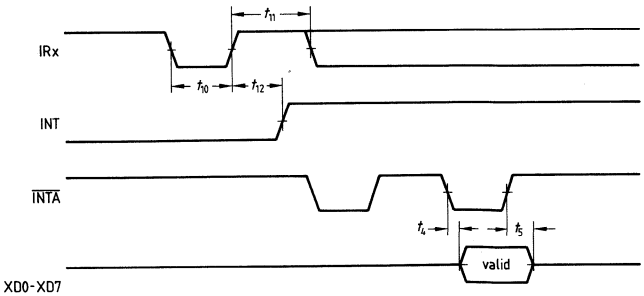
Peripheral Write Cycle



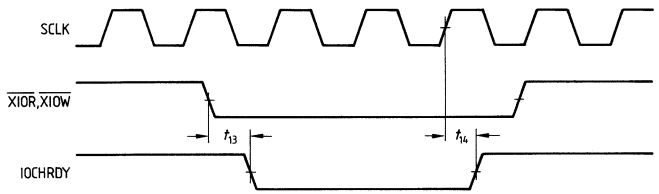
Command Recovery



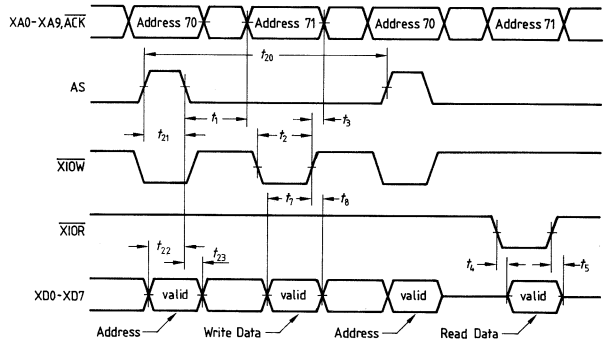
$\overline{\text{INTA}}$ Sequence



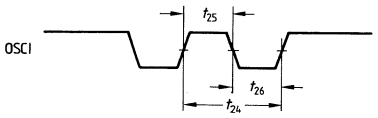
IOCHRDY OUTPUT



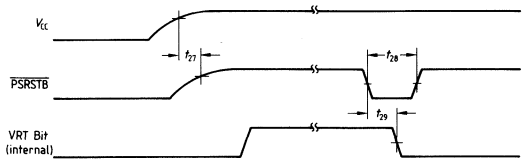
Real Time Clock Access Cycle



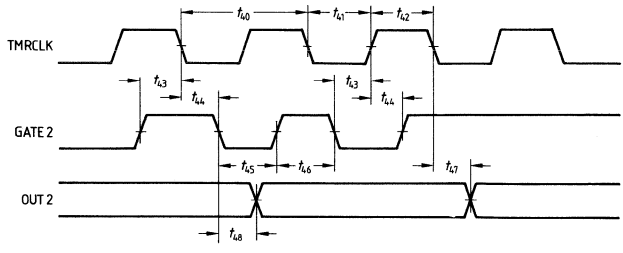
Real Time Clock Input



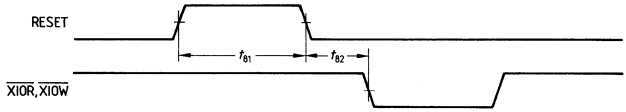
Real Time Clock Power-up Sequence



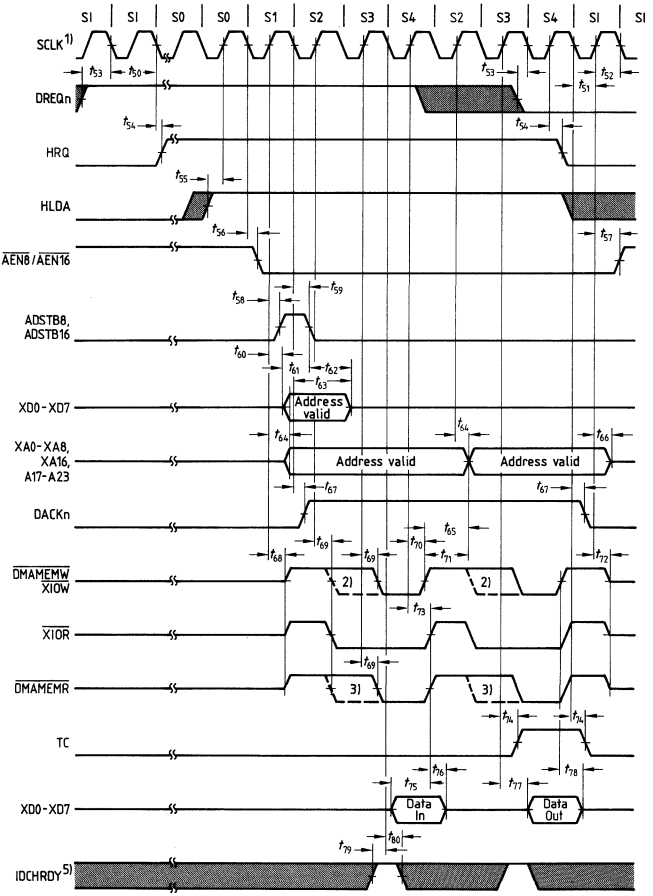
Counter/Timer Parameters



DMA Reset

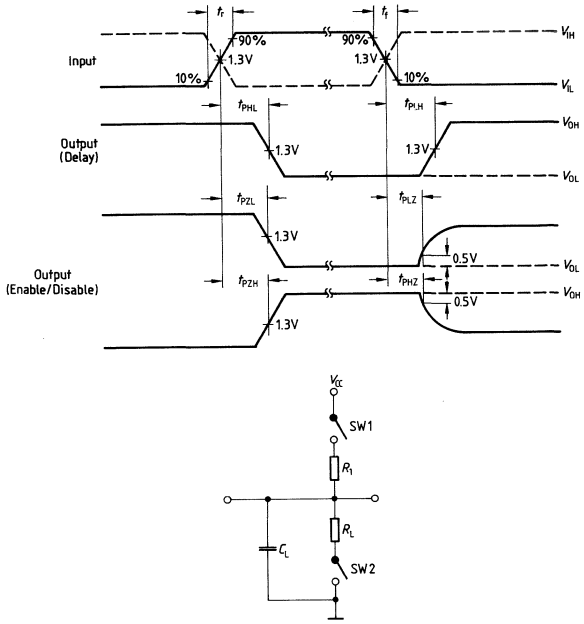


DMA Transfer Timing



1) All timings referenced to SCLK are independent of the state of the clock select bit in the configuration register. SCLK shown in this diagram is the undivided clock directly from the input.
2) Extended write mode selected
3) Extended read mode selected
4) Data bus during memory to memory transfer
5) IOCHRDY input timing

Load Circuit and AC Characteristics Measurement Waveform



Load Circuit Measurement Conditions

Parameter	Output type	Symbol	C_L (pF)	R_1 (kΩ)	R_L (kΩ)	SW_1	SW_2
Propagation delay time	Totem pole tristate Bidirectional	 t_{PLH} t_{PHL}	 50 50	 – –	 1.0 1.0	OFF	ON
Propagation delay time	Open drain or open collector	t_{PLH} t_{PHL}	50 50	0.5 0.5	– –	ON	OFF
Disable time	Tristate Bidirectional	t_{PLZ} t_{PHZ}	5 5	0.5 0.5	1.0 1.0	ON OFF	 ON
Enable time	Tristate Bidirectional	t_{PZL} t_{PZH}	50 50	0.5 0.5	1.0 1.0	ON OFF	ON ON

Ordering Information

Type	Ordering code	Description
SAB 82C206-N	Q67120-P286	Integrated peripheral controller (PL-CC-84)

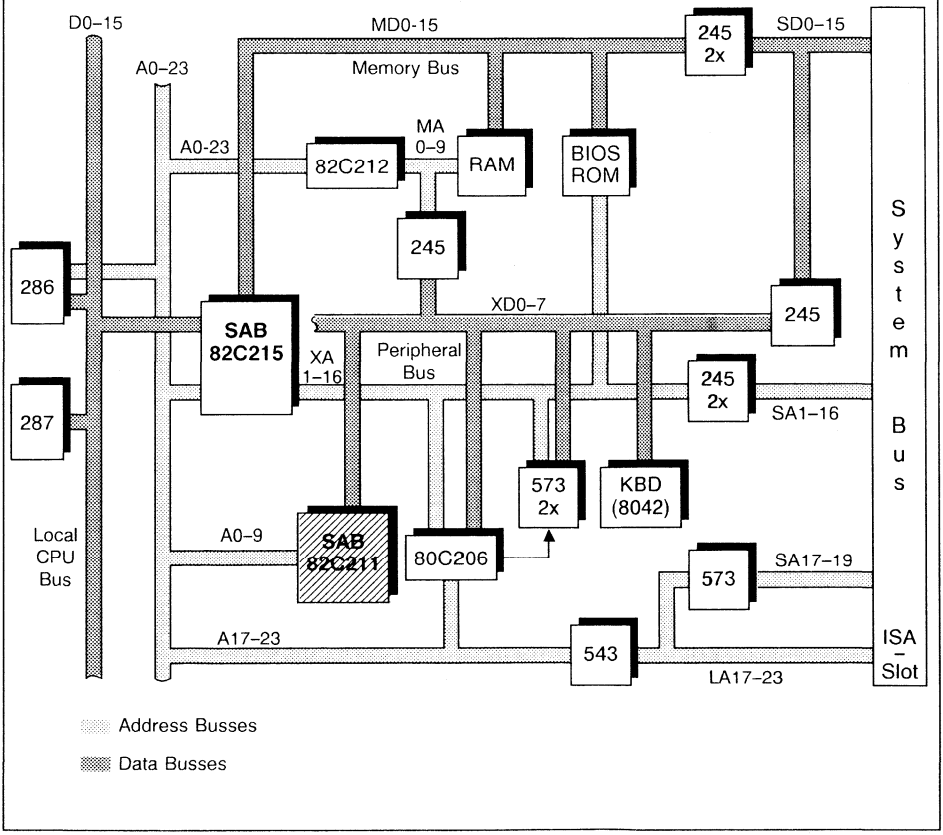
SIEMENS

SAB 82C211

CPU/Bus Controller of Siemens PC-AT™ Chipset

Advance Information

Siemens PC-AT Chipset



- SAB 80286 bus interface and bus control
- CPU/AT bus state machine and bus arbitration logic
- Clock generator with software speed selection logic (optional independent AT bus clock)
- Programmable command delays and wait state generation
- Reset and shut down control logic
- DMA and refresh control logic
- 80287 interface logic
- Action code generation logic for SAB 82C215
- Port B register and NMI logic
- Internal configuration registers
- CMOS implementation for high speed and low power requirements
- 84-pin plastic leaded chip carrier package (PL-CC-84)

As a member of the Siemens PC-AT Chipset the SAB 82C211 CPU/Bus Controller provides synchronization and control signals for the PC-AT busses.

The SAB 82C211 CPU/Bus controller, the SAB 82C212 memory controller, the SAB 82C215 data/address buffer and the SAB 82C206 integrated peripheral controller provide a highly integrated high performance system solution for PC-AT compatible systems.

The SAB 82C211 is fabricated in Siemens ACMOS technology and packaged in an 84-pin plastic leaded chip carrier package (PL-CC-84).

Ordering Information

Type	Ordering code	Package	Function
SAB 82C211-12-N	Q67120-P291	PL-CC-84 (SMD)	CPU/Bus Controller for Siemens PC-AT Chipset (12 MHz)
SAB 82C211-16-N	Q67120-P292	PL-CC-84 (SMD)	CPU/Bus Controller for Siemens PC-AT Chipset (16 MHz)

Figure 1
Logic Symbol

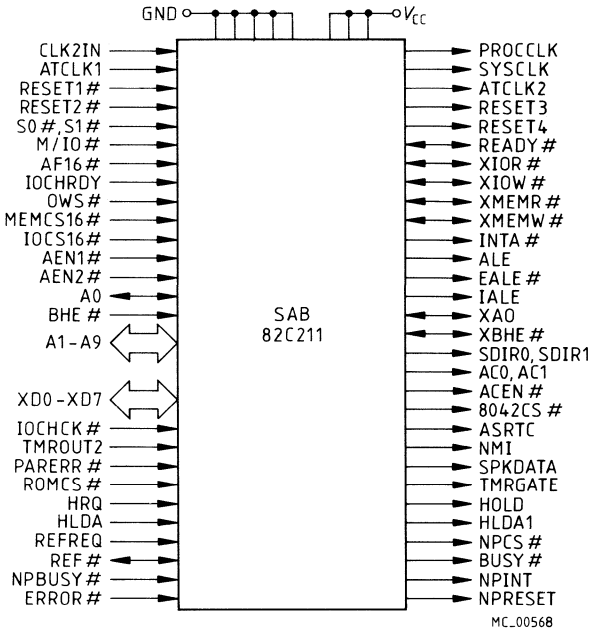
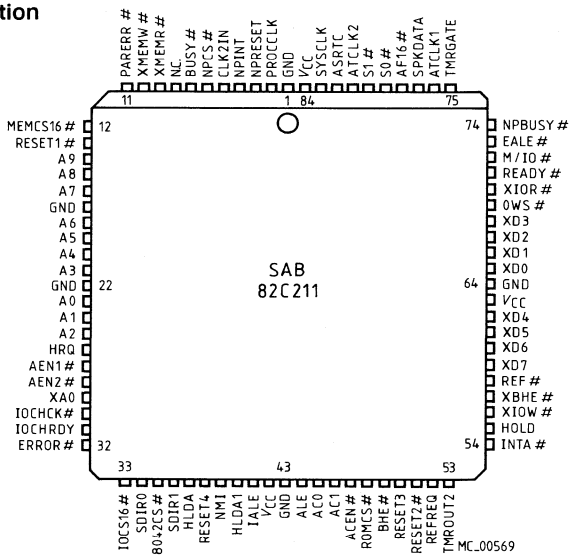


Figure 2
Pin Configuration



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
Clock Generator			
CLK2IN	5	I	**Clock 2 Input** CLK2IN is driven by a TTL crystal oscillator which has a maximum of twice the rated frequency of the SAB 80286 processor clock.
PROCCLK	2	O	**Processor Clock** This is the clock output for the SAB 80286 CPU and the SAB 82C212. It is derived from CLK2IN. It can also be programmed to be derived from ATCLK.
ATCLK1	76	I	**AT BUS Clock 1** ATCLK1 is the clock oscillator input for crystal operation or an external clock source. This clock input is used for the AT bus operation and is only required if the AT bus state machine clock, BLCK (internal) will not be derived from CLK2IN. This clock input should be tied low if not used. Its frequency should be lower than CLK2IN. BCLK is the AT bus state machine clock and can be programmed to be equal to ATCLK.
ATCLK2	81	O	**AT Bus Clock 2** ATCLK2 is the output of the SAB 82C211 crystal oscillator (if a crystal is used to generate AT bus clock). A series damping resistor of 10 Ω should be used to reduce amplitude of the resonant circuit. It should be left open if a TTL oscillator is used.
SYSCLK	83	O	**System Clock** AT System Clock output is buffered to drive the SYSCLK line on the AT bus I/O channel. It is half the frequency of BLCK and should be between 6 and 8 MHz for maintaining correct AT I/O bus timing compatibility with the IBM PC-AT.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
Reset Control			
RESET1#	13	I	**Reset Line1#** RESET1# is an active low input generated by the power good signal of the power supply. When low, it activates RESET3 and RESET4. RESET1# is latched internally.
RESET2#	51	I	**Reset Line 2#** RESET2# is an active low input generated from the keyboard controller (8042/8742) for a "warm reset" not requiring the system power to be shut off. It forces a CPU reset by activating RESET3.
RESET4	38	O	**Reset Line 4** RESET4 is an active high output used to reset the AT-bus, the SAB 82C206, the 8042 keyboard controller, and the SAB 82C212 memory controller. It is synchronized with the processor clock.
RESET3	50	O	**Reset Line 3** RESET3 is an active high output to the SAB 80286 CPU when RESET1# or RESET2# is active. It is also activated when shut-down condition in the CPU is deleted. RESET3 will stay active for at least 16 PROCLK cycles.
CPU Interface			
READY#	71	I/O	**Ready#** READY# as an output is driven low to terminate the current CPU cycle after IOCHDRY is high and OWS# is high, or if "time out" condition is detected. During all other cycles, it is an input from the SAB 82C212. It is an open collector output, requiring an external pull-up resistor of 1 KΩ and is connected to the SAB 80286 READY# pin.
S0# S1#	79 80	I I	**Status Inputs 0, 1#** The status signals S0# and S1# are used by the SAB 82C211 to determine the state of the CPU cycles. Pull-up resistors of 10 kΩ each should be provided.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CPU Interface (cont'd)			
M/IO#	72	I	**Memory/IO# Control** M/IO# is a signal from the SAB 80286 CPU. When high it indicates a memory access, when low it indicates an I/O access. It is used to generate memory and I/O control signals for the system. A 10 kΩ pull-up resistor is recommended.
HOLD	55	O	**Hold Request** HOLD is an active high output to the CPU. It is activated during DMA, Master or refresh cycles.
HLDA	37	I	**Hold Acknowledge** HLDA is an active high input generated by the CPU to indicate to the requesting master that it has relinquished the bus. When activated, all command lines (IOR#, IOW#, MEMR#, MEMW#, INTA#) are tristated.
BHE#	49	I/O	**Bus High Enable#** BHE# is an active low signal which indicates the transfer of data on the upper byte of the data bus. In conjunction with A0, it is input during CPU cycles and in conjunction with XA0, it is output during DMA/MASTER cycles. A pull-up resistor of 10 kΩ is required.
NMI	39	O	**Non Maskable Interrupt** NMI is an active high output to the NMI pin of the CPU and is generated by the SAB 82C211 to invoke a non-maskable interrupt.
IALE	41	O	**Internal Address Latch Enable** IALE is an active high output synchronized with PROCCLK and controls address latches used to hold addresses during bus cycles. It is not issued for halt bus cycles.
IOCHRDY	31	I	**I/O Channel Ready** IOCHRDY is an active high input from the AT bus. When low it indicates a not ready condition and inserts wait states in AT-I/O or AT-memory cycles. When high it allows termination of the current AT-bus cycle. A series damping resistor of 53 Ω at the AT bus connector is recommended to limit the negative under shoot. A 1 kΩ pull-up resistor is required for this open collector line.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CPU Interface (cont'd)			
IOCHCK#	30	I	**I/O Channel Check#** IOCHCK# is an active low input from the AT bus causing an NMI to be generated if enabled. It is used to signal an I/O error condition from a device residing on the AT bus. A 10 kΩ pull-up resistor is required.
PARERR#	11	I	**Parity Error#** PARERR# is an active low input from the SAB 82C215 which causes an NMI if enabled. It indicates a parity error in local system memory.
ALE	44	O	**Address Latch Enable** ALE is an active high output to the AT bus and is synchronized with the AT state machine clock. It controls the address latches used to hold the addresses during bus cycles. This signal should be buffered to drive the AT bus.
EALE#	73	O	**External/Address Latch Enable#** EALE# is an active low output used to latch the CPU A17–A23 address lines to the LA17–LA23 lines on the AT bus.
DMA Interface			
HLDA1	40	O	**Hold Acknowledge 1** HLDA1 is an active high output. It is activated when a bus cycle is granted in response to HRQ.
HRQ	26	I	**Hold Request** HRQ is an active high input. It is activated when DMA/Master is requesting a bus cycle. For an AT compatible architecture, it should be connected to the hold request signal from DMA1 and DMA2.
AEN1#	27	I	**Address Enable 1#** AEN1# is an active low input from one of the two DMA controllers enabling the address latches for 8-bit DMA transfers.
AEN2#	28	I	**Address Enable 2#** AEN2# is an active low input from one of the two DMA controllers enabling the address latches for 16-bit DMA transfers.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
DMA Interface (cont'd)			
ROMCS#	48	I	**ROM Chip Select#** ROMCS# is an active low input from the SAB 82C212. It is used to disable parity checks for local ROM cycles.
MEMCS16#	12	I	**Memory Chip Select 16#** MEMCS16# is an active low input from the AT bus indicating a 16-bit memory transfer. If high it implies an 8-bit memory transfer. A pull-up resistor of 330 Ω is required.
IOCS16#	33	I	**I/O Channel Select 16#** IOCS16# is an active low input from the AT bus indicating a 16-bit I/O transfer. If high it implies an 8-bit I/O transfer. A pull-up resistor of 330 Ω is required.
0WS#	69	I	**Zero Wait States#** 0WS# is an active low input from the AT bus causing immediate termination of the current AT bus cycle. Memories requiring zero wait states use this line to speed up memory cycles. It requires a 330 Ω pull-up resistor.
Device Decoder			
8042CS#	35	O	**8042 Chip Select#** 8042 Chip Select# is an active low signal for the keyboard controller chip select.
ASRTC	82	O	**Address Strobe to Real Time Clock** ASRTC is an active high signal used for the Real Time Clock at the SAB 82C206.
Refresh Control			
REFREQ	52	I	**Refresh Request** REFREQ is an active high input initiating a DRAM refresh sequence. It is generated by the 8254 compatible timer controller of the SAB 82C206 IPC in a PC-AT implementation.
REF#	58	I/O	**Refresh#** REF# is an active low signal. As an open drain output, it initiates a refresh cycle for the DRAMs. As an input, it can be used to force a refresh cycle from an I/O device. An external pull-up of 620 Ω is required.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
Peripheral Bus (X-Bus) Interface			
XMEMR#	9	I/O	**X-Bus Memory Read#** XMEMR# is an active low control strobe directing memory to place data on the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus.
XMEMW#	10	I/O	**X-Bus Memory Write#** XMEMW# is an active low control strobe directing memory to accept data from the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus.
XIOR#	70	I/O	**X-Bus I/O Read#** XIOR# is an active low strobe directing an I/O port to place data on the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus.
XIOW#	56	I/O	**X-Bus I/O Write#** XIOW# is an active low strobe directing an I/O port to accept data from the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus.
XBHE#	57	I/O	**X-Bus Byte High Enable#** XBHE# is an active low signal indicating the high byte has valid data on the bus. It is an output when the CPU is in control of the bus and is an input when a DMA controller is in control of the bus. A 4.7 kΩ pull-up resistor is required on this line.
XD0–3 XD4–7	65 – 68 62 – 59	I/O I/O	**X-Bus Data Lines 0–7** XD0-7 are the data bus lines of the peripheral data bus.
TMRGATE	75	O	**Timer Gate** TMRGATE is an active high output that enables the timer on the 8254 compatible counter/timer in the SAB 82C206 to enable the tone signal for the speaker.
TMROUT2	53	I	**Timer Out 2** TMROUT2 is an active high input from the 8254 compatible counter/timer in the SAB 82C206 that can be read from port B.

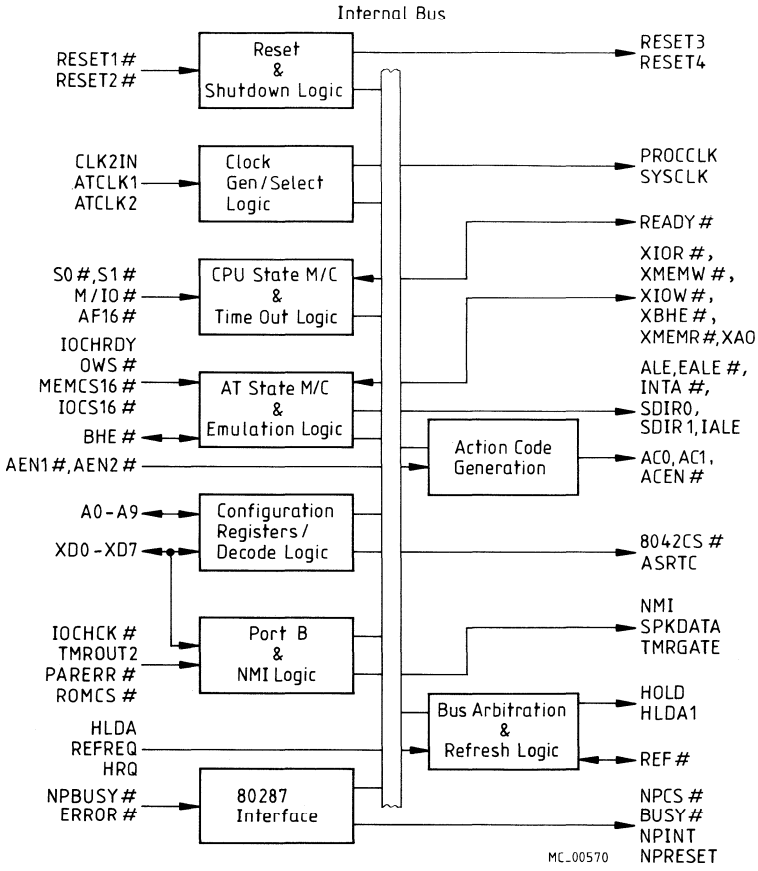
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
Peripheral Bus (X-Bus) Interface (cont'd)			
SPKDATA	77	O	**Speaker Data** SPKDATA is an active high output used to gate the 8254 compatible tone signal of the SAB 82C206 to the speaker.
INTA#	54	O	**Interrupt Acknowledge#** INTA# is an active low output to the SAB 82C206 interrupt controller. It is also used to direct data from the X-to S-bus during an interrupt acknowledge cycle.
Buffer Control			
SDIR0 SDIR1	34 36	O O	**System Bus Direction 0, 1** A low sets the data path from the S-Bus to the M-Bus. A high sets the data path from the M-Bus to the S-Bus. SDIR0 controls the low byte of the 16-bit data bus and SDIR1 controls the high byte.
ACEN#	47	O	**Action Code Enable#** ACEN# is an active low output that validates the action code signals AC0,1 that are used by the SAB 82C215 address/data buffer.
AC0 AC1	45 46	O O	**Action Code Lines 0,1** AC0,1 are 2-bit encoded outputs that control bus size and byte assembly operations performed in the SAB 82C215.
Memory Control			
AF16#	78	I	**AF16#** AF16# is an active low input indicating that the current cycle is a local bus cycle. A high indicates an AT bus cycle. A 10 kΩ pull-up resistor is required.
A0-2 A3-6 A7-9	23 – 25 21 – 18 16 – 14	I/O I/O I/O	**Address Lines 0-9** A0-A9 are input from the CPU. These lines are output during refresh. A1 is used to detect shut down condition of the CPU. A0 is used to generate the enable signal for the data bus transceivers.
XA0	29	I/O	**X-Bus Address Line 0** XA0 is an output during CPU accesses on the X-Bus and is an input for 8-bit DMA cycles.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
Coprocessor Interface			
NPCS#	6	O	**Numeric Coprocessor Chip Select#** NPCS# is an active low output signal used to select the internal registers of the 80287 NPX.
BUSY#	7	O	**Busy#** BUSY# is an active output to the CPU initiated by the 80287 NPX, indicating that it is busy. A 4.7 kΩ pull-up resistor is required.
NPBUSY#	74	I	**Numeric Coprocessor Busy#** NPBUSY# is an active low input from the NPX, indicating that it is currently executing a command. It is used to generate the BUSY signal to the CPU. A 4.7 kΩ pull-up resistor is required.
ERROR#	32	I	**Error#** ERROR# is an active low input from the NPX indicating that an unmasked error condition exists. A 4.7 kΩ pull-up resistor is required.
NPINT	4	O	**Numeric Coprocessor Interrupt** NPINT is an active high output. It is an interrupt request from the 80287 and is connected to the IRQ13 line of the SAB 82C206 IPC in a PC-AT environment. A 10 kΩ pull up resistor is required.
NPRESET	3	O	**Numeric Coprocessor Reset** NPRESET is an active high reset to the 80287. It is active when RESET4 is active or when a write operation is made to Port 0F1H. In the later case, it is active for the period of the command.
Miscellaneous			
NC	8	–	**Not connected**
V_{CC}	42, 63, 84	–	**Power Supply** (+ 5 V)
GND	1,17,22, 43,64	–	**Ground** (0 V)

Figure 3
Block Diagram



Functional Description

The SAB 82C211 CPU/Bus Controller of the Siemens PC-AT Chipset provides the following functional units:

- Reset and shut-down logic
- Clock generation and selection logic
- CPU state machine, AT bus state machine and bus arbitration logic
- Action codes generation logic
- Port B register and NMI logic
- DMA and refresh logic
- Numeric coprocessor interface logic
- Configuration registers

Reset and Shut-down Logic

Two reset inputs (RESET1# and RESET2#) are provided on the SAB 82C211 bus controller. RESET1# is the Power Good signal from the power supply. When RESET1# is active, the SAB 82C211 asserts RESET3 and RESET4 for a system reset. RESET2# is generated from the 8042 (or 8742) keyboard controller when a "warm reset" is required. The warm reset activates RESET3 to reset the 80286 CPU.

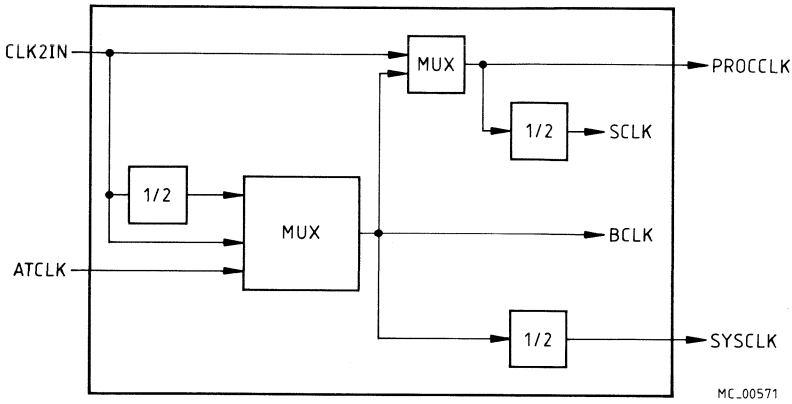
RESET3 is also activated by the SAB 82C211 when a shut-down condition is detected in the CPU. Additionally, a low to high transition in REG60.5 causes RESET3 to be active after the current I/O command goes inactive. RESET3 is asserted for at least 16 PROCCLK cycles and then deasserted. RESET4 is used to reset the AT bus, SAB 82C206 IPC, 8042 keyboard controller and the SAB 82C212 memory controller. It is synchronized with respect to PROCCLK and is asserted as long as the Power Good signal is held low.

After a shut-down condition is detected, RESET3 is asserted and held high for at least 16 PROCCLK cycles and then deasserted. RESET3 resulting from a shut-down condition is synchronous with PROCCLK, ensuring proper CPU operation. Both RESET3 and RESET4 meet the setup and hold timing requirements of the 80286 CPU.

Clock Generation and Selection Logic

The SAB 82C211 provides a flexible clock selection scheme as shown in figure 4. It has two input clocks; CLK2IN and ATCLK. CLK2IN is driven from TTL crystal oscillator, running at a maximum of twice the processor clock (PROCCLK) frequency. ATCLK is derived from a crystal. Typically, it should be of a lower frequency than CLK2IN. ATCLK and CLK2IN can be selected under program control.

Figure 4
Clock Selection Block Diagram



The SAB 82C211 generates processor clock, PROCCLK, for driving the CPU state machine and interface. SCLK (internal) is PROCCLK/2 and is in phase with the internal states or the 80286. BCLK (internal) is the AT bus state machine clock and is used for the AT bus interface. SYSCLK is the AT bus system clock and is always BCLK/2.

PROCCLK can be derived from CLK2IN or from ATCLK. In the synchronous mode, both PROCCLK and BCLK are derived from CLK2IN, so that the processor state machine and the AT bus state machine run synchronous. In the synchronous mode, BCLK is generated from the ATCLK and PROCCLK is generated from CLK2IN or the ATCLK. In this case, the processor and the AT bus state machines run asynchronous to each other. The following clock selections are possible:

Synchronous mode

1. PROCCLK = BCLK = CLK2IN
   SYSCLK = BCLK/2 = CLK2IN/2
2. PROCCLK = CLK2IN
   BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4
3. PROCCLK = BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4

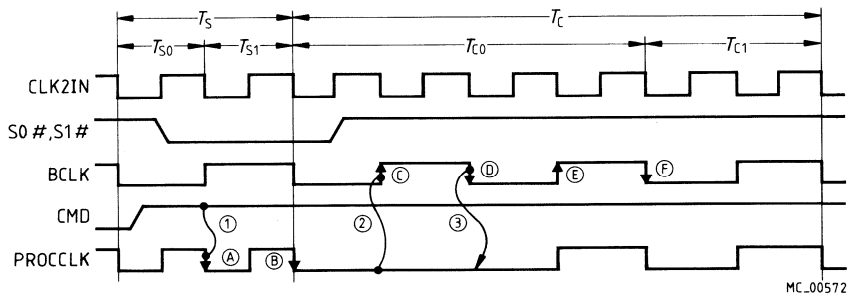
Asynchronous mode

1. PROCCLK = CLK2IN
   BCLK = ATCLK
   SYSCLK = BCLK/2 = ATCLK/2
2. PROCCLK = ATCLK
   BCLK = ATCLK
   SYSCLK = BCLK/2 = ATCLK/2.

Under normal operation, CLK2IN should be selected as the processor clock (PROCCLK) to allow the processor to run at full speed. BCLK can either be a sub-division of CLK2IN or the ATCLK. ATCLK may be selected to generate PROCCLK only when it is desired to slow down the processor for timing dependent code execution. Once the options for clock switching are set, the switching occurs with clean transition in the asynchronous or synchronous mode. During clock switching, no phases of PROCCLK are less than the minimum value or greater than the maximum value specified for the 80286 CPU. The clock source selection is made by writing to REG62H.1-0 first and then to REG60H.4, which default to: PROCCLK = CLK2IN, SYSCLK = CLK2IN/4.

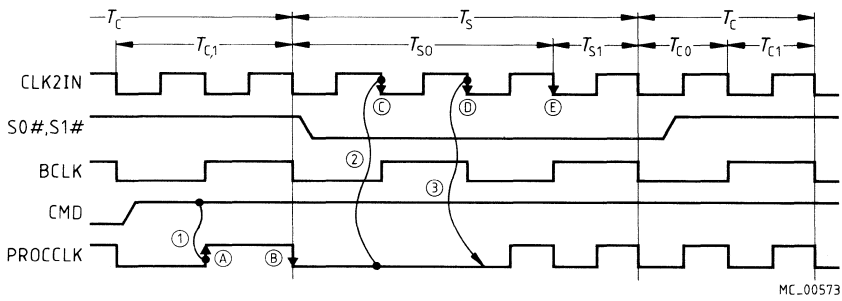
Figures 5 and 6 illustrate the sequence of events that switch PROCCLK from high to low speed and from low to high speed, upon receiving a request from the configuration register. In figure 5, the falling edge (A) of PROCCLK is used to latch the command inactive condition (1). On the falling edge (B), CLK2IN is disabled on the PROCCLK line. This ensures that clock switching will occur when PROCCLK is low. Once CLK2IN has been disabled, the first rising edge (C) of BLCK latches this condition as denoted by sequence (2). BLCK then enables itself on the PROCCLK line on the falling edge (D) as denoted by sequence (3). This ensures a glitch free transition between the two clocks. It also does not violate the min. and max. 80286 CPU clock specifications. If BLCK is asynchronous with respect to CLK2IN, it is possible that sequence (2) could violate setup time requirements with respect to edge (C). In this case, edge (D) will register the state of PROCCLK as still being high in sequence (3). Hence, edge (E) samples PROCCLK to be low and edge (F) enables BLCK on the PROCCLK line. This case does not violate the min. and max. 80286 CPU clock specifications.

Figure 5
Sequence Diagram for High to Low Frequency Transition



In figure 6, the rising edge (A) of PROCCLK latches command inactive as denoted by sequence (1). Edge (B) disables BLCK on the PROCCLK line. In sequence (2), edge (C) of CLK2IN latches PROCCLK low. Edge (D) then enables CLK2IN on the PROCCLK line as denoted by sequence (3). If sequence (2) does not meet setup time requirements of edge (C), then the state of PROCCLK is sampled being high in sequence (2). In this case, edge (D) samples PROCCLK low and edge (E) enables CLK2IN on the PROCCLK line. In this case also, PROCCLK does not violate the min. and max. 80286 CPU clock specifications.

Figure 6
Sequence Diagram for Low to High Frequency Transition



CPU State Machine, Bus State Machine and Bus Arbitration

In order to extract maximum performance out of the SAB 80286 on the system board, it is desirable to run the system board at the rated maximum CPU frequency. This frequency may be too fast for the slow AT bus. In order to overcome this problem, the SAB 82C211 has two state machines: the CPU state machine which typically runs off CLK2IN, and the AT bus state machine which runs off BLCK. The two state machines maintain an asynchronous protocol under external mode operation.

CPU State Machine

Interface to the SAB 80286 requires interpretation of the status lines S0#, S1#, M/IO# during T_{S0} and the synchonization and generation of READY# to the CPU upon completion of the requested operation. IALE# is issued in response to the beginning of a new cycle in T_{S1} by the SAB 82C211. If AF16# is detected as being inactive at the end of the processor T_S state, control is handed over the AT bus state machine. The CPU state machine then waits for READY# to be active to terminate the current cycle. All local memory cycles are 16-bit cycles. If AF16# is asserted in response to a new CPU cycle and READY is not returned to the SAB 82C211 within 128 clocks, and REG60H.2 is enabled, then an NMI is generated to signal bus time-out, if NMI has been enabled.

AT Bus State Machine

The AT bus state machine gains control when AF16# is detected inactive by the CPU state machine. It uses BLCK which is twice the frequency of AT system clock SYSCLK. When ATCLK is selected as the source for BLCK, it also performs the necessary synchronization of control and status signals between AT bus and the processor. The SAB 82C211 supports 8- and 16-bit transfers between the processor and 8- or 16-bit memory or I/O devices located on the AT bus. The action codes AC0, AC1 qualified by ACEN# are used for bus sizing and 8-, 16-bit bus conversions by the SAB 82C215.

The AT bus cycle is initiated by asserting ALE in AT-T_{S1}. On the falling edge of ALE, MEMCS16# is sampled for a memory cycle to determine the bus size. It then enters the command cycle AT-T_C and provides the sequencing and timing signals for the AT bus cycle. For an I/O cycle, IOCS16# is sampled in the middle of the processor T_C state. These control signals emulate the lower speed AT bus signals. The command cycle is terminated when IOCHDRY is active on the AT bus and all programmed wait states have been executed.

It is possible to provide software selectable wait states and command delays to the AT state machine. Providing command delays causes the commands (XMEMR#, XMEMW#, XIOR# or XIOW#) to be delayed from going active in BCLK steps. Providing wait states causes READY# to be delayed to the CPU in steps of the AT command cycles (AT-T_C).

Bus Arbitration

The SAB 82C211 controls all bus activity and provides arbitration between the CPU, DMA/Master devices, and DRAM refresh logic. It handles HRQ and REFREQ by generating HOLD request to the CPU and arbitrating among these requests in a non-preemptive manner. The CPU relinquishes the bus by issuing HLDA. The SAB 82C211 responds by issuing REF# or HLDA1 depending on the requesting device. During a refresh cycle, the refresh logic has control of the bus until REF# goes inactive. XMEMR# is asserted low during a refresh cycle and the refresh address is provided on the A0-A9 address lines by the SAB 82C211 to be used by the SAB 82C212 memory controller. During a DMA cycle, the DMA controller has control of the bus until HRQ goes inactive. The SAB 82C211 outputs the action codes for bus sizing. ALE, EALE# and ACEN# are active during DMA cycle.

Figure 7
Refresh/DMA Sequence

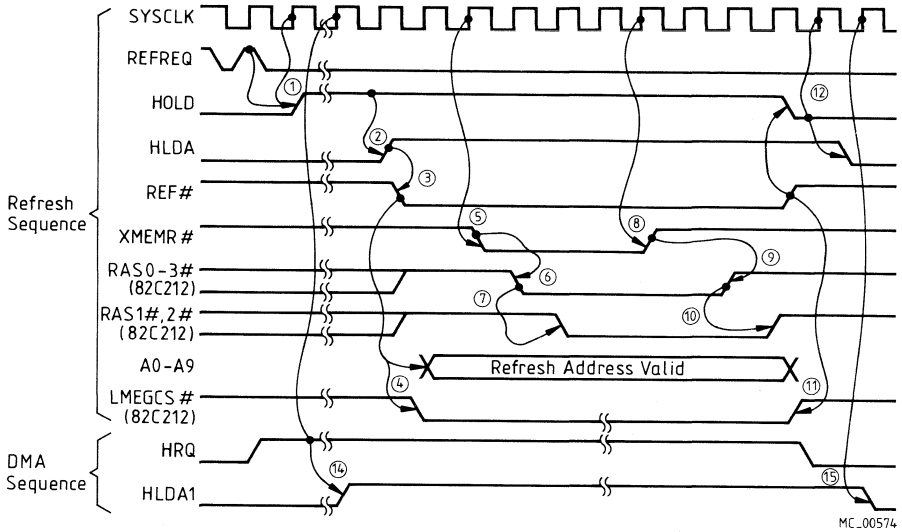


Figure 7 shows a sequence diagram for Refresh/DMA cycles. Upon receiving a refresh request (REFREQ) it is internally latched by the SAB 82C211. On the first rising edge of SYSCLK, HOLD is output to the processor in sequence 1. Depending on the current activity of the processor, a hold acknowlege (HLDA) is issued by the processor in sequence 2, after a DMA latency time. The SAB 82C211 responds with REF# active in sequence 3. LMEGCS# from the SAB 82C212 goes active in sequence 4. XMEMR# is asserted low on the second rising edge of SYSCLK after REF# is low in sequence 4. XMEMR# is asserted low on the second rising edge of SYSCLK after REF# is low in sequence 5.
The SAB 82C212 pulls all its RAS# lines (RAS0-RAS3#) high when REF# goes low. The RAS# lines go active in sequences 6 and 7 when the refresh address is active on the A0-A9 lines of the SAB 82C211. The SAB 82C212 uses the A0-A9 lines to generate the refresh address on the MA0-MA9 address lines. XMEMR# goes inactive in sequence 8 followed by the RAS# lines going inactive in sequences 9, 10. REF#, LMEGCS# and HOLD go inactive in sequence 11. Control is transferred to the CPU after HLDA goes inactive in sequence 12.

If a DMA device requests control of the bus, the SAB 82C211 receives HRQ active. After a DMA latency time, the CPU relinquishes the bus to the requesting device by issuing HLDA1 in sequence 14. HLDA1 is active as long as HRQ is active. Once the DMA device deasserts HRQ, HLDA1 is deasserted by the SAB 82C211 in sequence 15, to return control to the processor.

The AT state machine performs data conversion for CPU accesses to devices not on the CPU of Memory Bus. The AT bus conversions are performed for 16- to 8-bit read or write operations. Sixteen bit transfers to/from the CPU are broken into smaller 8-bit AT bus or peripheral bus reads or writes. The action codes are generated as shown in table 1 to control the buffers in the SAB 82C215. The action codes are in response to signals MEMCS16#, IOCS16#.

Table 1
Action Code Enable (ACEN#) Generation

Operation	ACEN#
DMA/MASTER	0
CPU (local)	1
CPU (AT bus)	0 for write 0 qualified by command for read and interrupt acknowledge cycles
REFRESH	1 qualified by REF#

Table 2
Definition of the Action Code Lines AC1, 0

AT-Bus CPU Cycles (HLDA1 = 0)

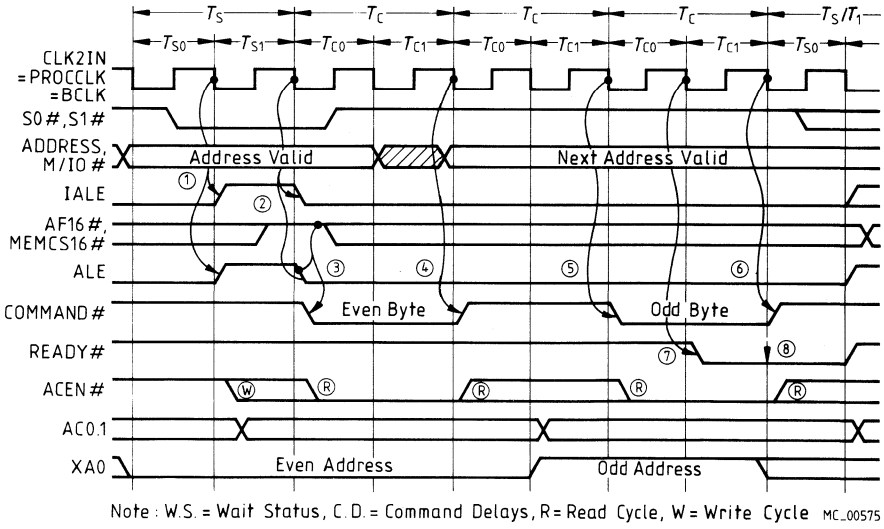
AC1, 0	Operation
00	16-bit write and 8-bit write (low byte)
01	16-bit read and 8-bit read (low byte)
10	8-bit write (high byte)
11	8-bit read (high byte)

DMA/MASTER Cycles (HLDA = 1)

AC1, 0	Operation
00	MD bus tri-stated from the SAB 82C215 for 16-bit and 8- (low byte) read/write operations
01	Reserved
10	High memory write MD0-7 to MD8-15
11	High memory read MD8-15 to MD0-7

Figure 8 shows a sequence diagram for a data conversion cycle in Quick mode with zero wait states (0 W.S.) and zero command delays (0 C.D.). In Quick mode ALE is issued on the AT bus as shown in sequences 1 and 2. MEMCS16# from an external device is sampled high by the SAB 82C211 in sequence 3, initiating a bus conversion cycle. The first command also goes active in sequence 3 for the first byte operation and is terminated in sequence 4. In order to provide sufficient back to back time between the two 8-bit cycles, the second byte command is issued two PROCCLKs later in sequence 5 and is terminated in sequence 6. No second ALE is issued for the second byte operation since only address line XA0 changes from zero to one. READY# is asserted low in sequence 7 and is sampled low by the processor in sequence 8, to terminate the current cycle. ACEN# and AC0, AC1 are issued by the SAB 82C211 for bus conversion as shown.

Figure 8
Quick Mode Bus Conversion Cycle (0 WS, 0 CD)



Port B and NMI Generation Logic

The SAB 82C211 provides access to Port B register defined for the PC/AT as shown in table 3.

Table 3
Port B Register Definition

IO ADDR	7	6	5	4	3	2	1	0	
61H	PCK	CHK	T20	RFD	EIC	EPR	SPK	T2G	PORT B

Bits	Read/Write	Function
7	R	PCK-System memory parity check
6	R	CHK-I/O channel check
5	R	T20-Timer 2 Out
4	R	RFD-Refresh Detect
3	R/W	EIC-Enable I/O channel check
2	R/W	EPR-Enable system memory parity check
1	R/W	SPK-Speaker Data
0	R/W	T2G-Timer 2 Gate (Speaker)

The NMI sub-module performs the latching and enabling of I/O and parity error conditions, which will generate a non-maskable interrupt to the CPU if NMI is enabled. Reading Port B will indicate the source of the error condition (CHK and PCK). Enabling and disabling of NMI is accomplished by writing to I/O address 070H. On the rising edge of XIOW#, NMI will be enabled if data bit 7 (XD7) is equal to 0 and will be disabled if XD7 is equal to 1.

Numeric Coprocessor Interface

Incorporated in the SAB 82C211 is the circuitry to interface an 80287 Numeric Coprocessor to the SAB 80286. The circuitry handles the decoding required for selecting and resetting the Numeric Coprocessor, handling NPBUSY# and ERROR# signals from the 80287 to the CPU, and generating interrupt signals for error handling.

The NPCS# signal is active for I/O addresses 0F8H-0FFH, used to access the internal registers of the 80287. It is also active for I/O addresses 070H-NMI mask register, 0F0H-Clear Numeric Coprocessor BUSY signal, and 0F1H-Clear the Numerical Coprocessor and Numerical Coprocessor BUSY signal. While executing a task, the 80287 issues an NPBUSY# signal to the SAB 82C211. Under normal operation, it is passed out to the CPU as BUSY#. If during this busy period, a numeric coprocessor error occurs, ERROR# input to the SAB 82C211 becomes active, resulting in latching of the BUSY# output and assertion of NPINT. Both signals stay active until cleared by an I/O write cycle to address 0F0H or 0F1H. A system reset clears both NPINT and BUSY# latches in the SAB 82C211. The 80287 is reset through the NPRESET output, which can be activated by a system reset or by performing a write operation to I/O port 0F1H.

Modes of Operation of the SAB 82C211

The SAB 82C211 has 4 modes of operation for different CPU and AT bus clock selections:

- Normal Mode
- Quick Mode
- Delayed Mode
- External Mode

Each mode is described in the following sections.

Normal Mode

This mode is enabled by default (without writing to the internal registers of the SAB 82C211). Under Normal Mode:

PROCCLK = CLK2IN
BCLK = CLK2IN/2
SYSCLK = CLK2IN/4

Since the CPU state machine clock and the AT bus state machine clock are derived from CLK2IN, this is a synchronous mode. ALE and commands (XMEMR#, XMEMW#, XIOR#, XIOW#) are issued only for AT bus cycles and not for local cycles. If activated by default, I/O cycles will have one command delay, 8-bit AT memory cycles will have 4 wait states, 16-bit AT memory cycles will have 1 wait state.

Figure 9
Normal Mode Local Cycle Followed by AT Bus Cycle (0 WS, 0 CD)

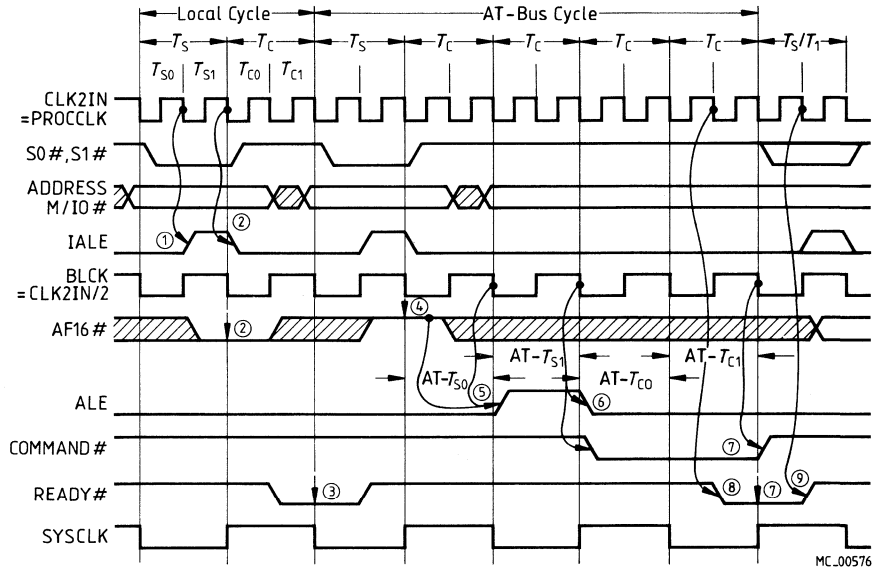
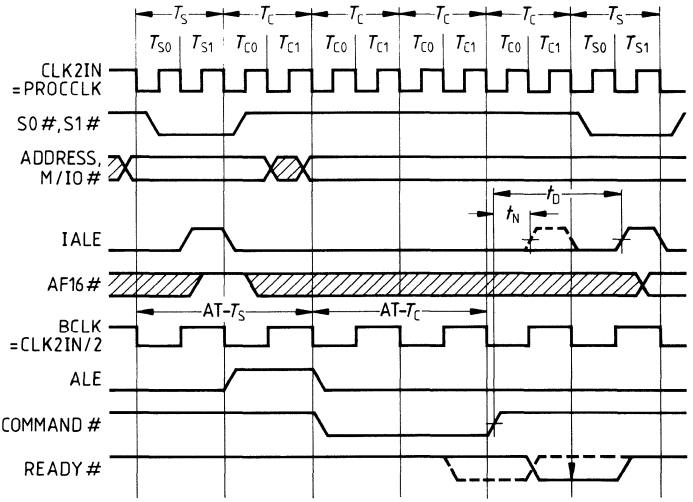


Figure 9 shows the sequence diagram of a Normal Mode local cycle with zero wait states (0 W.S.) and zero command delays (0 C.D.). In sequences 1 and 2, IALE is generated from CLK2IN. AF16# is sampled to be low in sequence 2. ALE and AT bus commands (XIOR#, XIOW#, XMEMR#, XMEMW#) are not generated since it is a local cycle. For a zero wait cycle, ready is sampled low by the 80286 CPU in sequence 3 and the cycle is terminated. For the AT bus cycle, AF16# is sampled high in sequence 4. Control is transferred to the AT bus state machine. BCLK then generates the AT bus states. ALE is generated in sequences 5 and 6. The AT bus command is generated in sequences 6 and 7, for zero command delays programmed in the SAB 82C211. For a zero wait state cycle, ready is asserted low as shown in sequences 8 and 9, to be sampled by the CPU in sequence 7. This terminates the AT bus cycle.

On the AT bus, certain slow peripherals require between 50 to 60 nanoseconds between commands going inactive to the next ALE going active, to provide sufficient data recovery time. The sequence diagram in figure 10 shows a Normal Mode AT bus cycle with additional hold time. The dotted IALE signal would have been valid, if the additional hold time register had not been enabled in RA1.7. Instead, IALE is delayed by one T_C state of the processor by asserting READY# one T_C cycle later. The SAB 82C212 provides an extended DLE to the SAB 82C215 in this mode, so that data is available to the CPU

during write cycles. If this mode was not invoked, then READY# would have been asserted earlier as shown by the dotted line. In Delayed Mode, the SAB 82C211 provides an extended data hold time. This additional hold time can only be programmed in the Normal Mode.

Figure 10
Normal Mode AT Bus Cycle with Additional Hold Time (0 WS, 0 CD)



Quick Mode

This mode is also a synchronous mode and is enabled by writing a zero to REG61.6 and the following clock selections have been made:

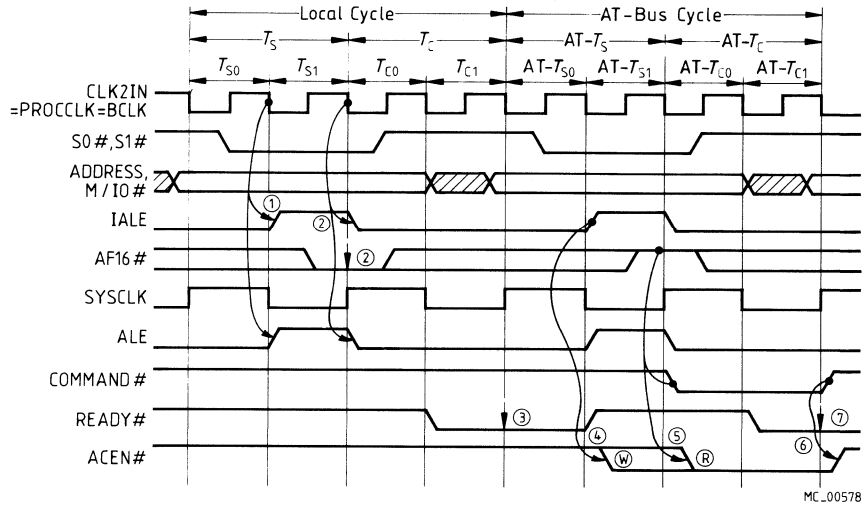
PROCCLK = BCLK = CLK2IN
SYSCLK = CLK2IN/2

In Quick Mode, an ALE signal is generated on the AT bus for both AT bus and local bus cycles. However, the commands (XMEMR#, XMEMW#, XIOR#, XIOW#) are not issued for local bus cycles.

The sequence diagram for a Quick Mode local cycle followed by an AT bus cycle is shown in figure 11. In this mode, both IALE and ALE are generated in sequences 1 and 2 for the local cycle. Hence, an ALE is issued on the AT bus for AT or non-AT bus cycles.

The local cycle is terminated when READY# is sampled low by the 80286 in sequence 3. For the AT bus cycle, the command is issued after AF16# is sampled high in sequence 5. For write cycles, ACEN# is activated in sequence 4. For read cycles, ACEN# is activated in sequence 5. If the next cycle is not an AT bus write cycle, then ACEN# is negated in sequence 6. READY# is sampled low by the 80286 in sequence 6, to terminate the cycle. As seen in figure 11 the AT bus states coincide with the CPU states for AT bus cycles. Hence, Quick Mode is performance efficient when switching local and AT bus cycles. This mode is useful for high speed add-on cards such as Laser Printer interface cards.

Figure 11
Quick Mode Local Cycle Followed by AT Bus Cycle (0 WS, 0 CD)



Delayed Mode

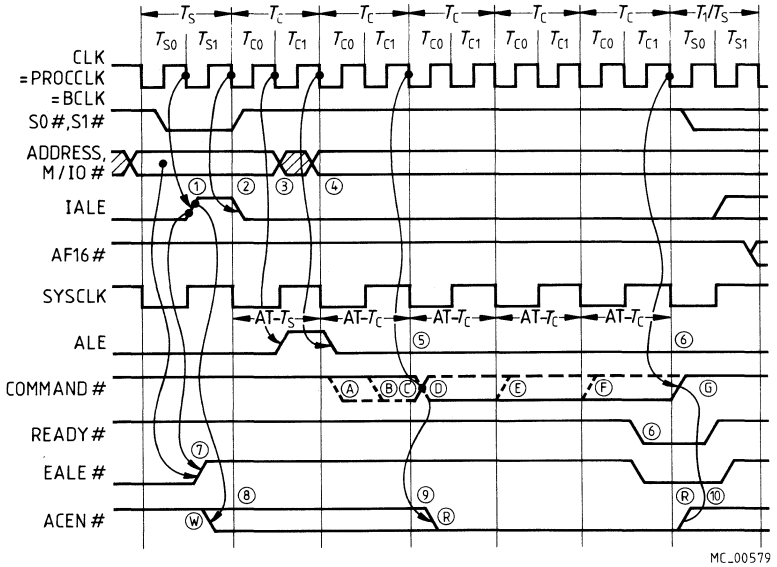
This mode is another synchronous mode and is enabled when Quick Mode is disabled and the following clock selections have been chosen made:

PROCCLK = CLK2IN
BCLK = CLK2IN
SYSCLK = CLK2IN/2

In Delayed Mode, ALE and commands are issued only for AT bus cycles like in the Normal Mode, except that BCLK = CLK2IN. ALE and commands are not issued for local cycles. Figure 12 shows a Delayed Mode AT bus cycle. IALE is generated in sequences 1 and 2.

ALE is asserted in sequences 3 after sampling AF16# high and it is deasserted in sequence 4. Hence the AT bus states, though synchronous, are delayed with respect to the processor states. Figure 12 is an example with two command delays and three wait states. The dotted lines A and B show command going active for 0 and 1 command delays. Sequence 5 shows command going active for programmed 2 command delays. Dotted lines D, E, F show command going inactive for 0, 1, 2 wait states. Sequence 6 shows command going inactive for programmed 3 wait states. READY# is sampled by the 80286 in sequence 6 to terminate the current cycle. Since the AT bus states are delayed with respect to the processor states, the local address lines LA17-LA23 (typically unlatched) are not valid when ALE is active. In order to have the LA17-LA23 lines valid when ALE is active, they are latched by EALE# as shown in sequence 7. Sequences 8, 9 show when ACEN# is asserted for AT bus write (W) and read (R) cycles. ACEN# is deasserted in sequence 10. This mode is useful for slow peripheral AT add-on cards.

Figure 12
Dealyed Mode AT Bus Cycle (3 WS, 2 CD)



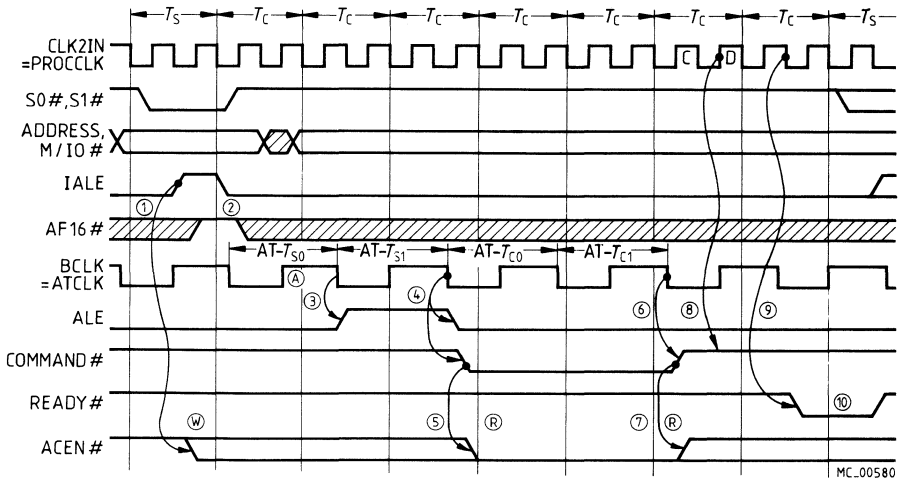
External Mode

This is an asynchronous mode and is enabled when ATCLK is selected as the source for BLCK. The following clock selections are required in this mode:

PROCCLK = CLK2IN
BCLK = ATCLK
SYSCLK = ATCLK/2

Since ATCLK is asynchronous to CLK2IN, the CPU state machine runs asynchronous to the AT bus state machine. ALE and commands (XMEMR#, XMEMW#, XIOR#, XIOW#) are issued only for AT bus cycles. These signals are inactive for local cycles. Figure 13 shows a sequence diagram for an External Mode AT bus cycle. AF16# is sampled high in sequence 2 and is latched internally, using CLK2IN. The asynchronous BLCK samples this latched state on the next rising edge of the BCLK. In the example shown, edge A samples the latched AF16# signal (internal) high. This causes the AT state machine to issue an ALE in sequences 3 and 4. For a zero command delay, zero wait states cycle, the command is issued on the AT bus in sequences 4 and 6, synchronized with BCLK. For write cycles, ACEN# is asserted in sequence 1 and for read cycles, it is asserted in sequence 5. ACEN# is deasserted in sequence 7. The command inactive state is sampled by CLK2IN on every rising edge. In this case, edge D of CLK2IN samples command high (sequence 8). It is followed by the assertion of READY# in sequence 9, synchronized with CLK2IN. The CPU samples READY# low in sequence 10 and terminates the current cycle.

Figure 13
External Mode AT Bus Cycle (0 WS, 0 CD)



Configuration Registers

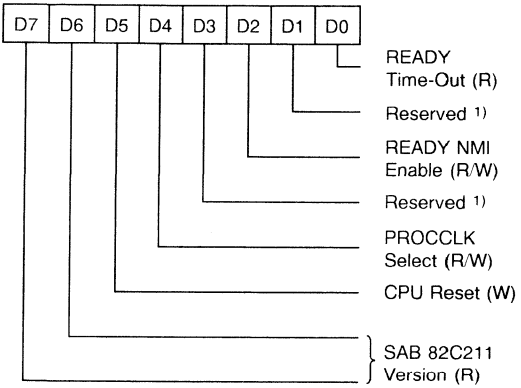
There are three bytes of configuration registers in the SAB 82C211; RA0, RA1 and RA2. An indexing scheme is used to reduce the I/O ports required to access all the registers required for the Siemens PC-AT Chipset. Port 22 H is used as an indexing register and Port 23 H is used as the data register. The index value is placed in port 22 H to access a particular register and the data to be read from or written to that register is located in port 23 H. Every access to port 23 H must be preceded by a write of the index value to port 22 H even if the same register data is being accessed again. All reserved bits are set to zero by default and when written to, must be set to zero.
Table 4 to 7 list up the three registers:

Table 4
SAB 82C211 Configuration Registers

Register Number	Register Name	Index
RA0	PROCCLK Selector	60 H
RA1	Command Delay	61 H
RA2	Wait State/BCLK Selector	62 H

Table 5
Description of RA0 (PROCCLK Register)

Index register port: 22 H
Data register port: 23 H
Index: 60 H

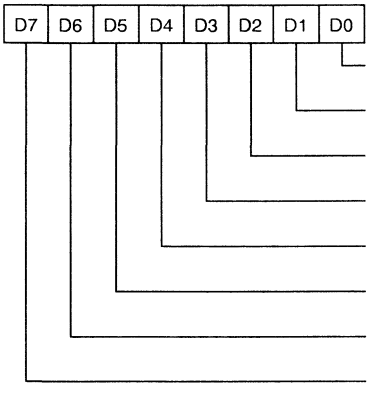


Bits	Function
0	Local bus READY timeout. A one indicates that READY timeout has occurred 128 PROCCLK cycles after AF16# has been asserted. A zero indicates that READY time out has not occurred.
1	Reserved 1)
2	Local bus READY timeout NMI enable. A one enables the NMI and a zero disables it. Default is 0
3	Reserved 1)
4	Processor clock select is by default set to zero and selects PROCCLK = CLK2IN. If high, it selects PROCCLK = BCLK.
5	Alternate CPU reset. A low to high transition in this bit activates a CPU reset. Once active, it remains active for 16 PROCCLK cycles and then goes low.
7, 6	SAB 82C211 revision number. 00 is the initial number.

1) The reserved bits are recommanded to be initialized to 1.

Table 6
Description of RA1 (Command Delay Register)

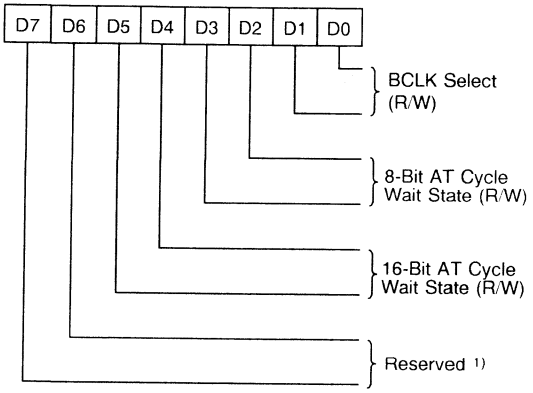
Index register port: 22 H
Data register port: 23 H
Index: 61 H



Bits	Function
1, 0	At Bus I/O cycle command delay. Specifies between 0 to 3 BCLK cycle command delays for AT I/O cycles. Default is 1.
3, 2	AT Bus 8-bit memory command delay. Specifies between 0 to 3 BCLK cycle command delays for 8-bit AT memory cycles. Default is 1.
5, 4	AT Bus 16-bit memory command delay. Specifies between 0 and 3 BCLK cycle command delays for 16-bit AT memory cycles. Default is 0.
6	Quick Mode enable. A zero enables Quick Mode and a one disables it. Default is 1.
7	Address hold time delay. A one enables extra address bus hold time and a zero disables it. Default is 0.

Table 7
Description of RA2 (Wait States Register)

Index register port: 22 H
Data register port: 23 H
Index: 62 H



Bits	Function
1, 0	Bus clock (BCLK) source select. Default is 00.
00	BCLK = CLK2IN/2
01	BCLK = CLK2IN
10	BCLK = ATCLK
11	Reserved
3, 2	8-bit AT cycle wait state generation. Default is 5.
00	2 wait states
01	3 wait states
10	4 wait states
11	5 wait states
5, 4	16-bit AT cycle wait state generation. Default is 3.
00	0 wait states
01	1 wait state
10	2 wait states
11	3 wait states
7, 6	Reserved 1)

1) The reserved bits are recommanded to be initialized to 1.

Absolute Maximum Ratings

Ambient temperature under bias ..... 0 to 70 °C
Storage temperature ..... – 65 to + 150 °C
Supply voltage ..... – 0.5 to + 7.0 V
Voltage on any pin with respect to ground ..... – 0.5 to V_{CC} + 0.5 V
Power dissipation ..... 1 W

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	–	0.8	V	–
Input high voltage	V_{IH}	2.0	–	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 4 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = –4 mA
Input leakage current	I_{IL}	–	± 10	µA	0 V < V_{IN} < V_{CC}
Power supply current	I_{CC}	–	50	mA	@16 MHz
Output tristate leakage current	I_{OZ1}	–	± 10	µA	0.45 V < V_{OUT} < V_{CC}
PROCCLK output low voltage	V_{OLC}	–	0.45	V	I_{OL} = 5 mA
PROCCLK output high voltage	V_{OHC}	4.0	–	V	I_{OH} = –1 mA
Standby power supply current	I_{CCSB}	–	1.5	mA	–

AC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ±5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
ALE active delay from SYSCLK ↓	t_1	– 1	10	ns	SAB 82C211-12
		– 1	6	ns	SAB 82C211-16
ALE inactive delay from SYSCLK ↑	t_2	– 1	10	ns	SAB 82C211-12
		– 1	6	ns	SAB 82C211-16
Command active delay from SYSCLK ↓	t_3	0	8	ns	–
Command inactive delay from SYSCLK ↑	t_4	0	6	ns	–
EALE# active delay from SYSCLK ↓	t_5	0	10	ns	–
MEMCS16# setup time to SYSCLK ↑	t_6	10	–	ns	–
MEMCS16# hold time to SYSCLK ↑	t_7	4	–	ns	–
IOCS16# setup time to SYSCLK ↓	t_8	10	–	ns	–
IOCS16# hold time to SYSCLK ↓	t_9	10	–	ns	–
OWS# setup time to SYSCLK ↑	t_{10}	9	–	ns	–
OWS# hold time to SYSCLK ↑	t_{11}	4	–	ns	–
IOCHRDY setup time to SYSCLK ↑	t_{12}	11	–	ns	–
IOCHRDY hold time to SYSCLK ↑	t_{13}	4	–	ns	–
IALE active delay from PROCCLK ↓	t_{14}	1	10	ns	–
IALE inactive delay from PROCCLK ↓	t_{15}	1	16	ns	SAB 82C211-12
		1	11	ns	SAB 82C211-16
AF16# setup time to PROCCLK ↓	t_{16}	19	–	ns	SAB 82C211-12
		15	–	ns	SAB 82C211-16
AF16# hold time to PROCCLK ↓	t_{17}	13	–	ns	SAB 82C211-12
		11	–	ns	SAB 82C211-16
READY# input setup time to PROCCLK ↓	t_{18}	11	–	ns	–
READY# input hold time to PROCCLK ↓	t_{19}	8	–	ns	–
RESET3 active delay from PROCCLK ↓	t_{20}	2	12	ns	–
RESET3 inactive delay from PROCCLK ↓	t_{21}	2	16	ns	–
RESET4 active delay from PROCCLK ↓	t_{22}	0	8	ns	–
RESET4 inactive delay from PROCCLK ↓	t_{23}	1	16	ns	–
SDIR0,1 active delay from SYSCLK ↓	t_{24}	3	11	ns	–
SDIR0,1 inactive delay from SYSCLK ↑	t_{25}	1	10	ns	–
ACEN# active delay from SYSCLK ↓	t_{26}	0	7	ns	–
ACEN# inactive delay from SYSCLK ↑	t_{27}	0	6	ns	–

AC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
AC0 active delay from PROCCLK ↓	t_{32}	6	17	ns	–
AC0 inactive delay from PROCCLK ↓	t_{33}	6	18	ns	–
AC1 active delay from PROCCLK ↓	t_{34}	7	18	ns	–
AC1 inactive delay from PROCCLK ↓	t_{35}	7	18	ns	–
HOLD active delay from SYSCLK ↓	t_{38}	0	6	ns	–
HOLD inactive delay from SYSCLK ↑	t_{39}	0	6	ns	–
REF# delay from HLDA	t_{40}	3	14	ns	–
REF# inactive delay from SYSCLK ↑	t_{43}	0	6	ns	–
XMEMR# active delay from SYSCLK ↑	t_{44}	1	9	ns	–
XMEMR# inactive delay from SYSCLK ↑	t_{45}	0	5	ns	–
HRQ setup to SYSCLK ↑	t_{46}	10	–	ns	–
HRQ hold time to SYSCLK ↑	t_{47}	4	–	ns	–
HLDA1 active delay from HLDA ↑	t_{49}	8	17	ns	–
HLDA1 inactive delay from HLDA ↓	t_{51}	12	20	ns	–
NPCS# active delay from PROCCLK ↓	t_{52}	11	21	ns	–
Overlap of NPBUSY#&ERROR# (both low)	t_{53}	8	–	ns	–
NPINT active delay from NPBUSY#, ERROR# low	t_{54}	7	16	ns	–
NPINT inactive delay from ERROR# ↑	t_{55}	3	11	ns	–
NPBUSY# active pulse width	t_{56}	13	–	ns	–
ERROR# hold time with respect to NPBUSY# ↑	t_{57}	0	–	ns	–
ERROR# setup time to NPBUSY# ↑	t_{58}	3	–	ns	–
ERROR# min. low time	t_{59}	8	–	ns	–
BUSY# active delay from NPBUSY# ↓	t_{60}	8	18	ns	–
BUSY# inactive delay from NPBUSY# ↑	t_{61}	8	15	ns	–
BUSY# delay from IOW# ↓	t_{62}	2	12	ns	–
NPRST active delay from IOW# ↓	t_{63}	9	19	ns	–
NPRST inactive delay from IOW# ↑	t_{64}	4	15	ns	–

Figure 14
Bus Cycle Timing

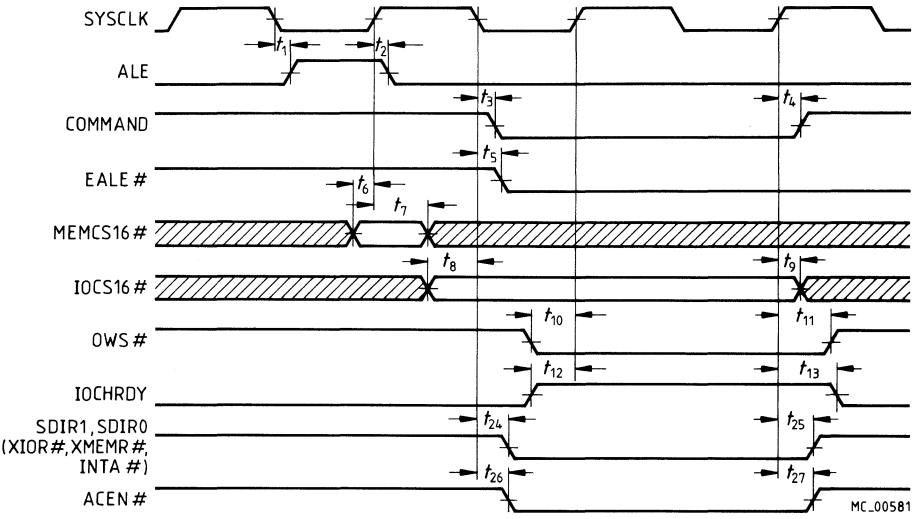


Figure 15
Local Bus/Coprocessor Timing

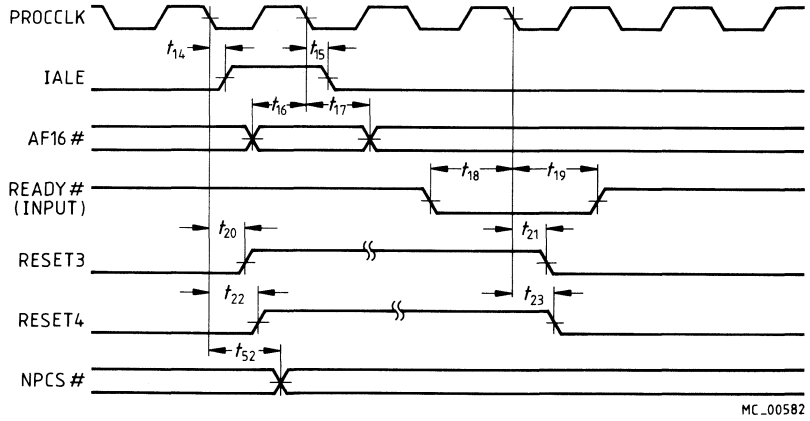


Figure 16
Action Code Timing

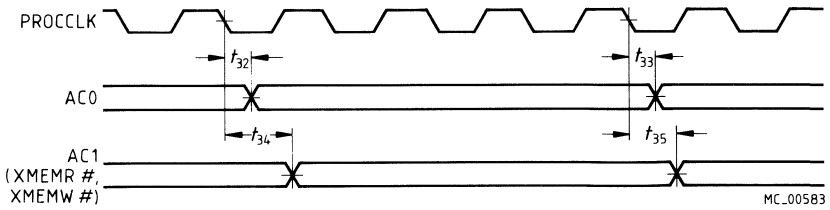


Figure 17
Refresh/DMA Timing

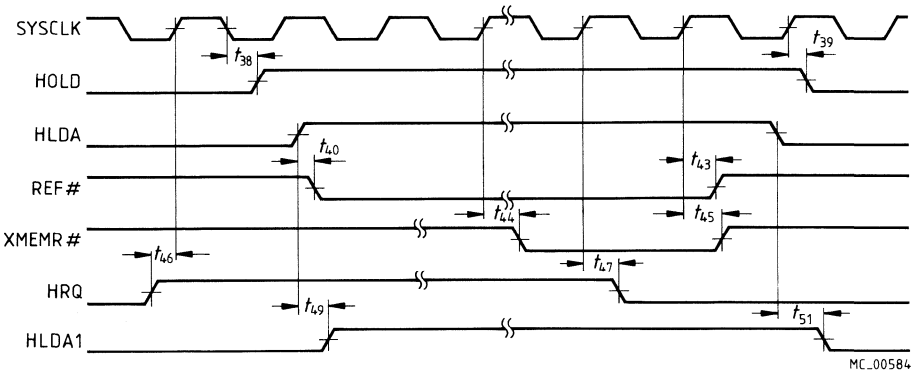


Figure 18
Coprocessor Timing

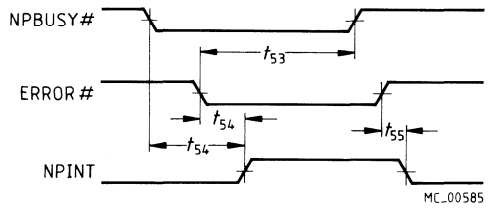


Figure 19
Coprocessor Timing

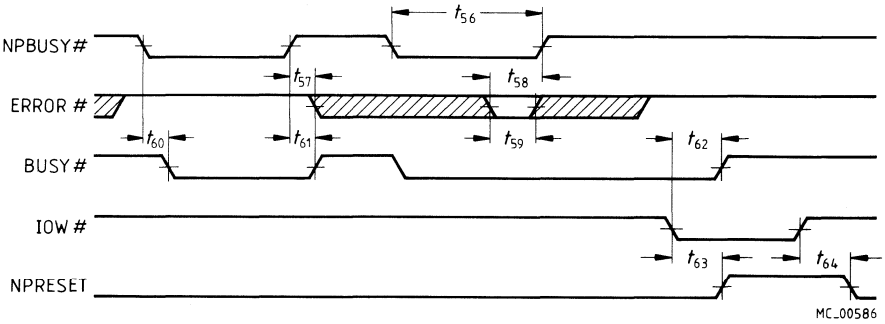
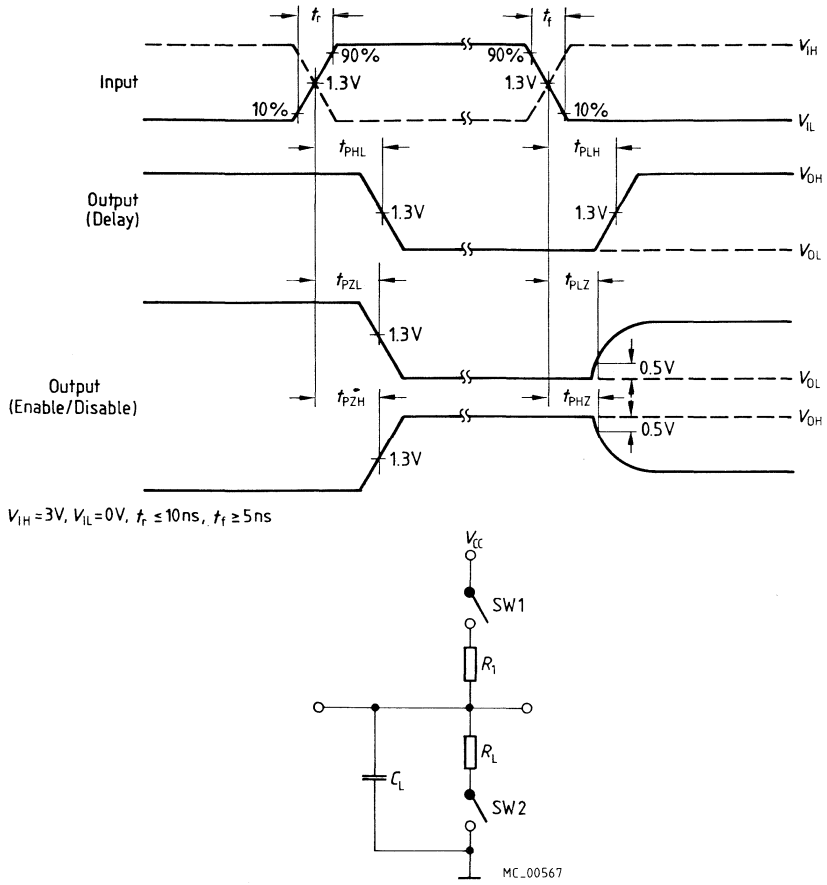


Figure 20
Load Circuit and AC Characteristics Measurement Waveform



V_{IH} = 3V, V_{IL} = 0V, $t_r \leq 10$ns, $t_f \geq 5$ns

Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L (pF)	R_1 (kΩ)	R_L (kΩ)	SW_1	SW_2
Propagation	Totem Pole						
Delay Time	Tristate	t_{PLH}	50	–	1.0	OFF	ON
	Bidirectional	t_{PHL}	50	–	1.0	OFF	ON
Propagation	Open Drain or	t_{PLH}	50	0.5	–	ON	OFF
Delay Time	Open Collector	t_{PHL}	50	0.5	–	ON	OFF
Disable Time	Tristate	t_{PLZ}	5	0.5	1.0	ON	
	Bidirectional	t_{PHZ}	5	0.5	1.0	OFF	ON
Enable Time	Tristate	t_{PZL}	50	0.5	1.0	ON	ON
	Bidirectional	t_{PZH}	50	0.5	1.0	OFF	ON

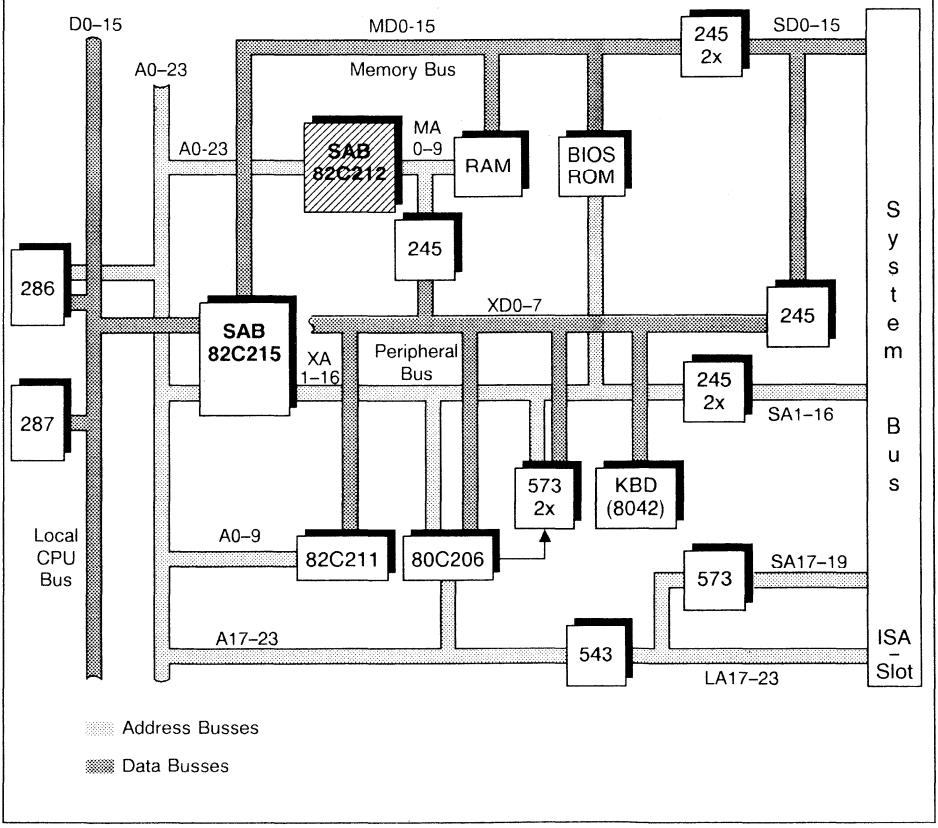
SIEMENS

SAB 82C212

Page/Interleave Memory Controller of Siemens PC-AT™ Chipset

Advance Information

Siemens PC-AT Chipset



- Higher performance of DRAM accesses using page mode access together with a interleaved memory accessing scheme
- Page interleaved operation with 16 MHz CPU and 100 ns DRAMs.
- Remapping of DRAM resident in 640 K to 1 MByte area as extended memory
- Supports Expanded Memory System (LIM-EMS 4.0) address translation logic
- Shadow RAM feature for fast BIOS code execution.
- Supports up to 8 MByte on-board DRAM (1 M/256 K DRAM's)
- Optimized fast switching between SAB 80286 protected and real mode for OS/2
- Staggered DRAM refresh for power supply noise reduction
- CMOS implementation for high speed and low power requirements
- 84-pin plastic leaded chip carrier package (PL-CC-84)

As a member of the Siemens PC-AT Chipset the SAB 82C212 memory controller provides an interleaved memory subsystem design with page mode operation. Also EMS address translation and shadow RAM for BIOS execution are supported.
The SAB 82C211 CPU/Bus controller, the SAB 82C212 memory controller, the SAB 82C215 data/address buffer and the SAB 82C206 integrated peripheral controller provide a highly integrated high performance system solution for PC-AT compatible systems.
The SAB 82C212 is fabricated in Siemens ACMOS technology and packaged in a 84-pin plastic leaded chip carrier package (PL-CC-84).

Ordering Information

Type	Ordering code	Package	Function
SAB 82C212-12-N	Q67120-P294	PL-CC-84 (SMD)	Page/Interleaved Memory Controller for Siemens PC-AT Chipset (12 MHz)
SAB 82C212-16-N	Q67120-P295	PL-CC-84 (SMD)	Page/Interleaved Memory Controller for Siemens PC-AT Chipset (16 MHz)

Figure 1
Logic Symbol

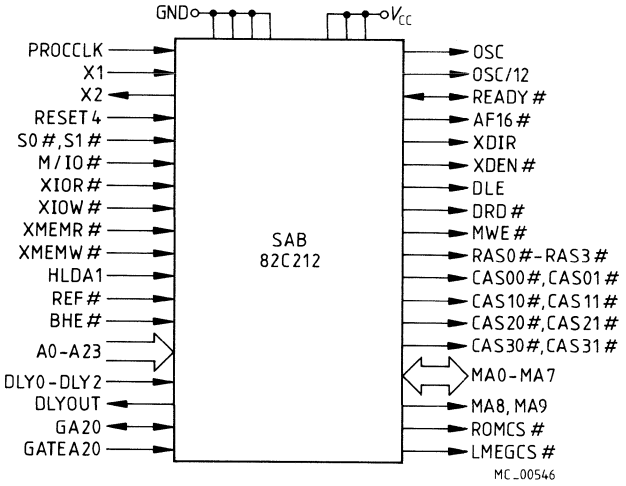
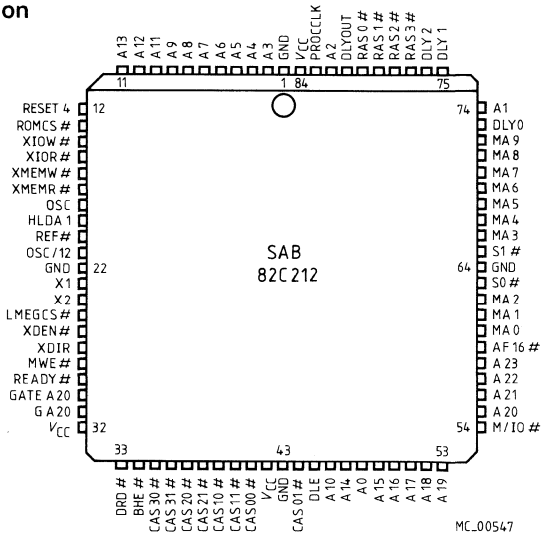


Figure 2
Pin Configuration



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
Clocks and Control			
PROCCLK	83	I	**Processor Clock** PROCCLK is the clock input line from the SAB 82C211.
X1	23	I	**Crystal 1** X1 is the input of the crystal oscillator circuit. Typically a 14.31818 MHz crystal is connected to X1.
X2	24	O	**Crystal 2** X2 is the output of the crystal oscillator circuit. Typically a 14.31818 MHz crystal is connected to X2.
OSC	18	O	**Oscillator Output** OSC is the oscillator output for the system clock at 14.31818 MHz and has a drive capability of 24 mA.
OSC/12	21	O	**Oscillator/12 Output** OSC/12 is an output with a clock frequency equal to 1/12 of the crystal frequency across the X1, X2 pins.
RESET4	12	I	**Reset Line 4** RESET 4 is the active high reset input from the SAB 82C211. It resets the configuration registers to their default values. When active, RAS0-3# and CAS00-31# remain high, OSC and OSC/12 remain inactive.
REF#	20	I	**Refresh#** REF# is an active low input for DRAM refresh control from the SAB 82C211. It initiates a refresh cycle for the DRAMs.
S1# S0#	65 63	I I	**Status Inputs 0, 1#** S0#, S1# are the status lines from the 80286 CPU. These lines are monitored to detect the start of a cycle.
M/IO#	54	I	**Memory/IO Control#** M/IO# is a signal from the 80286 CPU. If high it indicates a memory cycle. If low, it indicates an I/O cycle.
XIOR#	15	I	**X-Bus I/O Read#** XIOR# is the active low I/O read command line.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
Clocks and Control (cont'd)			
XIOW#	14	I	**X-Bus I/O Write#** XIOW# is the active low I/O write command line.
XMEMR#	17	I	**X-Bus Memory Read#** XMEMR# is the active low memory ready command line.
XMEMW#	16	I	**X-Bus Memory Write#** XMEMW# is the active low memory write command line.
HLDA1	19	I	**Hold Acknowledge 1** HLDA1 is an active high input from the SAB 82C211. It is used to generate RAS# and CAS# signals for DMA cycles, in response to a hold request.
ROMCS#	13	O	**ROM Chip Select#** ROMCS# is an active low chip select output to the BIOS EPROM. It can be connected to the output enable pin of the EPROM.
A0-A23	1)	I	**Address Inputs 0-23** A0-23 are the address input lines from the local CPU bus.
BHE#	34	I	**Byte High Enable#** BHE# is an active low input from the CPU for transfer of data on the upper byte.
READY#	29	I/O	**Ready#** READY# is the system ready signal to the CPU. It is an active low output after requested memory or I/O data transfer is completed. It is an input when the current bus cycle is an AT bus cycle and is an output for local memory and I/O cycles.
AF16#	59	O	**AF16#** AF16# is an active low output asserted on local memory (EPROM or DRAM) cycles. It is high for all other cycles. This signal is sampled by the SAB 82C211.

1) For detailed pin numbers see figure 2 (Pin configuration).

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
DRAM Interface			
RAS0-3#	80-77	O	**Row Address Strobe 0-3#** RAS0-3# are active low outputs used as RAS# signals to the DRAMs for selecting different banks. RAS3# selects the highest bank and RAS0# selects the lowest bank. These signals should be buffered and line terminated with 75 Ω resistors to reduce ringing before driving the DRAM RAS# lines.
CAS00#	41	O	**Column Address Strobe 00#** CAS00# is an active low output used to select the low byte DRAMs of bank 0. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS01#	44	O	**Column Address Strobe 01#** CAS01# is an active low output used to select the high byte DRAMs of bank 0. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS10#	39	O	**Column Address Strobe 10#** CAS10# is an active low output used to select the low byte DRAMs of bank 1. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS11#	40	O	**Column Address Strobe 11#** CAS11# is an active low output used to select the high byte DRAMs of bank 1. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS20#	37	O	**Column Address Strobe 20#** CAS20# is an active low output used to select the low byte DRAMs of bank 2. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS21#	38	O	**Column Address Strobe 21#** CAS21# is an active low output used to select the high byte DRAMs of bank 2. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.

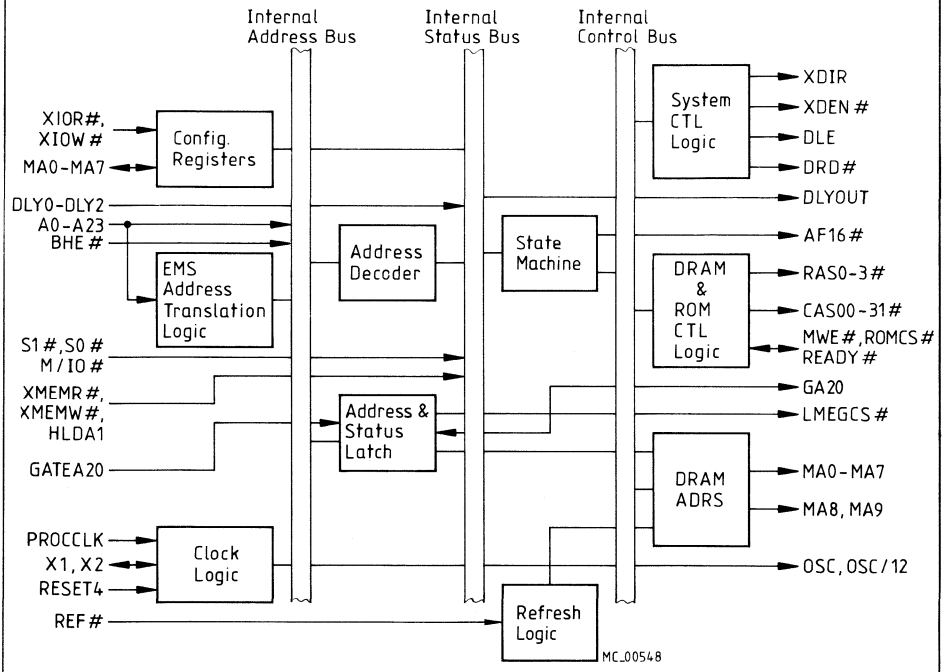
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
DRAM Interface (cont'd)			
CAS30#	35	O	**Column Address Strobe 30#** CAS30# is an active low output used to select the low byte DRAMs of bank 3. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
CAS31#	36	O	**Column Address Strobe 31#** CAS31# is an active low output used to select the high byte DRAMs of bank 3. This signal should be line terminated with a 75 Ω resistor to reduce ringing before driving the DRAM CAS# line.
MWE#	28	O	**Memory Write Enable#** MWE# is an active low output for DRAM write enable.
DLE	45	O	**Data Latch Enable** DLE is an active high output used to enable the local memory data buffer latch in the SAB 82C215.
DRD#	33	O	**Data Read#** DRD# is an active low output used to transfer data from the memory bus to the local CPU bus in the SAB 82C215. If high it sets the data path from the local CPU bus to the memory bus.
DLYOUT	81	O	**Delay Line Out** DLYOUT is an active high output to the delay line for generating the DRAM control signals.
DLY0 DLY1 DLY2	73 75 76	I I I	**Delay Input 0-2** DLY0-2 are active high inputs from the first to third taps of the delay line used to generate DRAM control signals.
XDEN#	26	O	**X-Data Buffer Enable#** XDEN# is an active low output asserted during I/O accesses to locations 22 H and 23 H. These locations contain the index and data registers for the Siemens PC-AT Chipset. It is used to enable the buffers between the XD and MA buses for accessing the SAB 82C212 internal registers.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
DRAM Interface (cont'd)			
XDIR	27	O	**X-Bus Direction** XDIR is used to control the drivers between the X and S busses. The driver should be used such that data flow is from the S to X bus when XDIR is high and in the other direction when XDIR is low.
MA8 MA9	71 72	O O	**Multiplexed DRAM Address 8, 9** The MA8, 9 address lines should be buffered and line terminated with 75 Ω resistors before driving the DRAM address lines.
MA0-2 MA3-7	60-62 66-70	I/O I/O	**Multiplexed DRAM Address 0-7** MA0-MA7 are used as bi-directional lines to read/write to the internal registers of the SAB 82C212. An external 74ALS245 buffer is required to isolate this path during normal DRAM operation. These lines should be buffered and line terminated with 75 Ω resistors before driving the DRAM address lines.
Miscellaneous			
GA20	31	I/O	**Gated Address Line A20** GA20 is the gated A20 address bit which is controlled by GATEA20.
GATEA20	30	I	**Gate Address 20** GATEA20 is an input used to force GA20 low when GATEA20 is low. When high it propagates A20 onto the GA20 line. It is used to keep address under 1 Mbyte during DOS operation.
LMEGCS#	25	O	**Low Meg Memory Chip Select** LMEGCS# is an unlatched active low output asserted when the low Meg memory address space (0 to 1024 Kbytes) is accessed or during refresh cycles. It is used to disable SMEMR# and SMEMW# signals on the AT bus if access are made beyond the 1 Mbyte address space to maintain PC and PC/XT compatibility.
V_{CC}	32, 42, 84	–	Power Supply (+ 5 V)
GND	1, 22, 43, 64	–	Ground (0 V)

Figure 3
Block Diagram



Functional Description

The SAB 82C212 Page/Interleave memory controller of the Siemens PC-AT Chipset provides the following functional submodules:

- EPROM and DRAM control logic
- System control logic
- Memory mapping and refresh logic
- Oscillator clock generation logic
- Configuration registers

Prior to the description of these functional submodules the following section describes some principles of the SAB 82C212 integrated features.

Overview

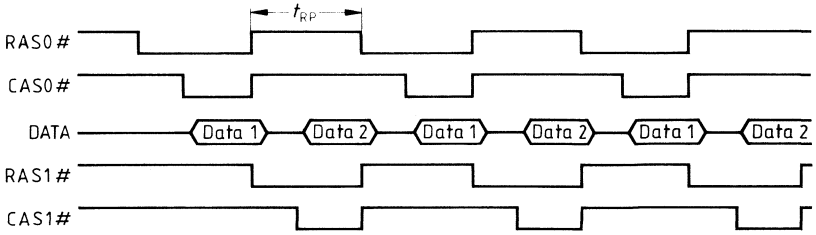
The SAB 82C212 performs the memory control functions in the Siemens PC-AT Chipset system, utilizing page mode access DRAMs. The various possible memory array configurations and page/interleaved mode operation are discussed in this section.

Memory Array Configuration

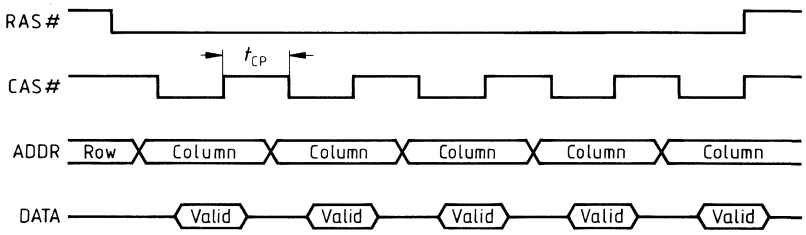
The SAB 82C212 organizes memory as banks of 18-bit modules, consisting of 16-bits of data and 2-bits of parity information. The 16-bits of data are split into high and low order bytes, with one parity bit for each byte. This configuration can be implemented by using eighteen 1-bit wide DRAMs or by using four 4-bit wide DRAMs for data with two 1-bit wide DRAMs for parity. The minimum configuration can be a single bank operating in non-interleaved mode or can be a pair of DRAM banks operating in two way interleaved mode. If the SAB 82C212 uses a two way interleaving scheme, the DRAMs within a pair of banks must be identical. However, each bank of DRAM pairs can be different from other pairs. For example, banks 0, 1 may have 256 K by 1-bit DRAMs and banks 2 and 3 could have 1 M by 1-bit DRAMs. A typical system may be shipped with one or two banks of smaller DRAM types (e.g. 256 K by 1-bit DRAMs) and later upgraded with additional pairs of banks of larger DRAMs (e.g. 1 M by 1-bit DRAMs).

Figure 4
DRAM Access Schemes

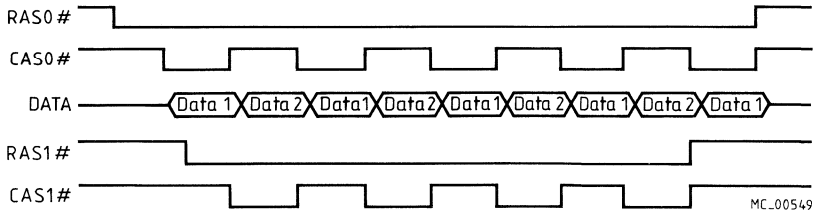
a) 2-Way DRAM Interleaved Operation



b) DRAM Page Mode Operation



c) 2-Way DRAM Page/Interleave Operation



Page/Interleaved Operation

The SAB 82C212 uses a page/interleaved design that is different from most interleaved memory designs. Typical two way interleaving schemes use two banks of DRAMs with even word addresses on one bank and odd word addresses on the other bank. If memory accesses are sequential, the RAS# precharge time of one bank overlaps the access time of the other bank. Typically, programs consist of instruction fetches interspersed with operand accesses. The instruction fetches tend to be sequential and the operand accesses tend to be random.

Figure 4a is a sequence diagram for a memory interleaved scheme using two banks 0 and 1. The RAS# signals of the two banks are interleaved so that the RAS# precharge time (t_{RP}) of one bank is used for the RAS# active time in the other bank. This requires sequential accesses to be alternating between the two banks. For non-sequential accesses, it is possible to get wait states due to a 'miss'. Typically, this results in a 50 % hit ratio (possible zero wait state accesses).

Figure 4b is a sequence diagram of a paged mode DRAM operation. In paged mode DRAMs, once a row access has been made, it is possible to access subsequent column addresses within that row, without the RAS# precharge penalty. However, after a RAS# active timeout, there is a RAS# precharge period which typically occurs every 10 micro-seconds. Since the CAS# precharge time t_{CP} is small, it is possible to make fast random accesses within a selected row. Typically, page mode access times are half the normal DRAM access times. For 256 K × 1 DRAMs, each row has 512-bits. If eighteen 256 K × 1-bit DRAMs are used to implement a bank, a page would have 512 × 2 Bytes (excluding 2-bits for parity) = 1 Kbytes. Thus paged mode DRAMs could be interleaved at 1 Kbyte boundaries rather than 2 Byte boundaries as in the regular interleaved mode operation. Any access to the currently active RAS# page would occur in a short page access time and any subsequent access could be anywhere in the same 1 Kbyte boundary, without incurring any penalty due to RAS# precharge. If memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving because:

1. Page mode access time is shorter than normal DRAM access time. This allows more time in the DRAM critical paths, to achieve penalty free accesses or 'hits'.
2. The possibility of the next access being fast is significantly higher than in a regular interleaving scheme. This is because instructions and data tend to cluster together by principle of locality of reference.

Figure 4c is a sequence diagram of a two way page/interleaved scheme using page mode DRAMs. As seen, it is possible to make zero wait state accesses between the two banks 0 and 1, by overlapping CAS# precharge time of the other bank. The DRAM RAS# lines for both banks can be held active till the RAS# active time out period, at which time a RAS# precharge for that bank is required. Typical hit ratios higher then 80 % are possible using this scheme. With the SAB 82C212 memory controller, using the page/interleaved scheme, 150 ns access time DRAMs can be used at 12 MHz and 100 ns access time DRAMs at 16 MHz.

The SAB 82C212 supports both two and four way interleaved mode. If four way interleaved mode is used, the DRAMs used in the four banks must be identical. Table 1 shows the 0 wait state hit space for possible banks configurations.

Table 1
Average 0 Wait State Hit Space

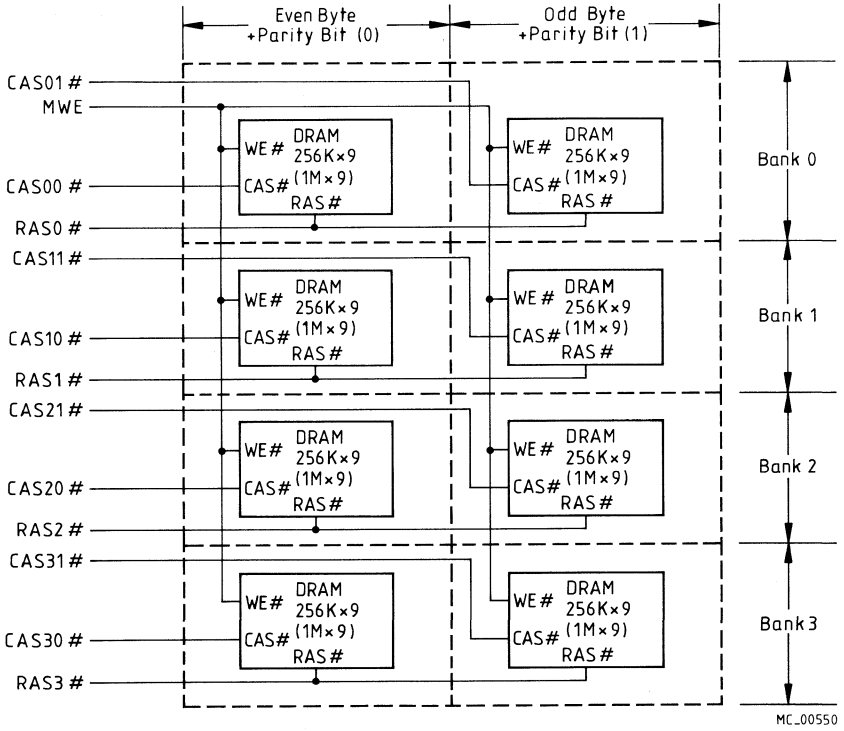
DRAM Type				Two Way Interleaved	Four Way Interleaved
Bank 0	Bank 1	Bank 2	Bank 3		
256 K	256 K	0	0	2 K	NA
256 K	256 K	256 K	256 K	2 K	4 K
256 K	256 K	1 M	1 M	3 K	NA
1 M	1 M	0	0	4 K	NA
1 M	1 M	1 M	1 M	4 K	8 K

OS/2 Optimization

The Siemens PC-AT Chipset architecture features OS/2 optimization using REG6F.1 of the SAB 82C212 in conjunction with REG60.5 of the SAB 82C211. OS/2 makes frequent DOS calls while operating in protected mode of the SAB 80286 CPU. In order to service these DOS calls, the SAB 80286 CPU has to switch from protected to real mode quickly. Typcial PC/AT architectures require the processor to issue two commands to the 8042 (or 8742) keyboard controller in order to reset the processor (to switch it into protected mode) and to activate GATEA20.

REG60.5 of the SAB 82C211 is to used to invoke a software reset to the SAB 80286 processor and REG6F.1 is used to activate GATEA20. Since this involves two I/O writes, it is possible to execute a "Fast GATEA20". In an OS/2 environment, where frequent DOS calls are made, this feature provides significant performance improvement.

Figure 5
DRAM Organization



EPROM and DRAM Control Logic

The EPROM and DRAM control logic in the SAB 82C212 is responsible for the generation of the RAS#, CAS# and MWE# signals for DRAM accesses and the generation of ROMCS# for EPROM accesses. This sub-module also generates READY# to the CPU upon completion of the desired local memory operation. The appropriate number of wait states are inserted, as programmed by software (or by default) in the wait state register of the SAB 82C212. Figure 5 is a block diagram of the DRAM organization for the Siemens PC-AT Chipset architecture. As seen, each RAS# line drives each 256 K × 18-bit bank (or 1 M × 18-bit bank). The CAS# lines are used to drive individual bytes within each bank. MWE# is connected to each DRAM bank write enable input.

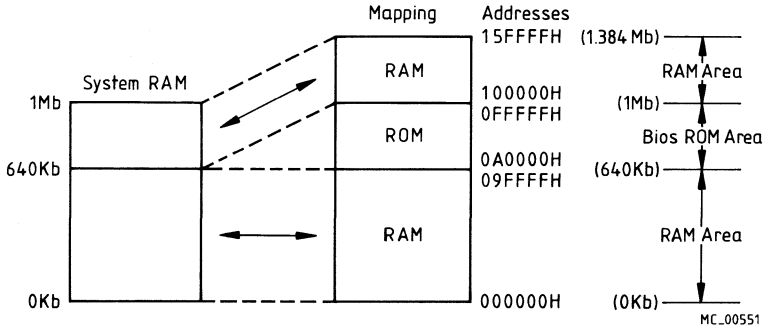
System Control Logic

This sub-module of the SAB 82C212 generates XDEN#, DLE, DRD#, AF16# for system control. XDEN# is issued for I/O accesses to the internal registers of the SAB 82C212. It is used to enable the XD0-7 lines onto the MA0-7 lines from an external buffer, for accessing the internal registers of the SAB 82C212. The DLE and DRD# signals are generated for enabling and controlling the direction of data between the CPU data bus and the memory data bus (MD bus). AF16# is issued by the SAB 82C212 state machine. It is active for local memory accesses and meets the set up and hold times with respect to PROCCLK for the SAB 82C211.

Memory Mapping and Refresh Logic

The SAB 82C212 has an extensive set of memory mapping registers for various memory organizations. Through the memory mapping logic, for up to 1 Mbyte of system RAM, it is possible to map RAM that overlaps the EPROM area (640 Kbyte - 1 Mbyte) above the 1 Mbyte area, as shown in figure 6. Hence, for 1 Mbyte of on board RAM, the software can address it from 0 to 640 Kbytes and from 1 Mbyte to 1.384 Mbytes. The EPROM can be addressed from the 640 Kbyte area to the 1 Mbyte area. For normal mode of operation, only one bank of DRAMs may be used. However, for the page/interleaved mode of operation, RAM bank pairs must be used.

Figure 6
System RAM/ROM Mapping for 1 Mbyte System RAM



Shadow RAM Feature

For efficient execution of BIOS, it is preferable to execute BIOS code through RAM rather than through slower EPROMs. The SAB 82C212 provides the shadow RAM feature which if enabled allows the BIOS code to be executed from system RAM resident at the same physical address as the BIOS EPROM. The software should transfer code stored in the BIOS EPROMs to the system RAM, before enabling the shadow RAM feature. This feature significantly improves the performance in BIOS-call intensive applications. Performance improvements as high as 300 to 400 % have been observed in benckmark tests on the shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping register.

If more than 1 Mbyte of system RAM exists, it is mapped as shown in figure 7a, if the shadow RAM feature is not invoked. This means that RAM in the 640 Kbyte to 1 Mbyte area cannot be accessed. If the shadow RAM feature is used, then the RAM is mapped as shown in figure 7b, overlapping or shadowing the EPROM area. In both cases, for accesses beyond the 1 Mbyte address range, the processor is switched from real to protected mode from BIOS.

Figure 7
RAM/ROM Mapping

a) RAM/ROM Mapping without Shadow RAM (More Than 1 Mbyte of RAM)

b) RAM Mapping with Shadow RAM (More Than 1 Mbyte of RAM)

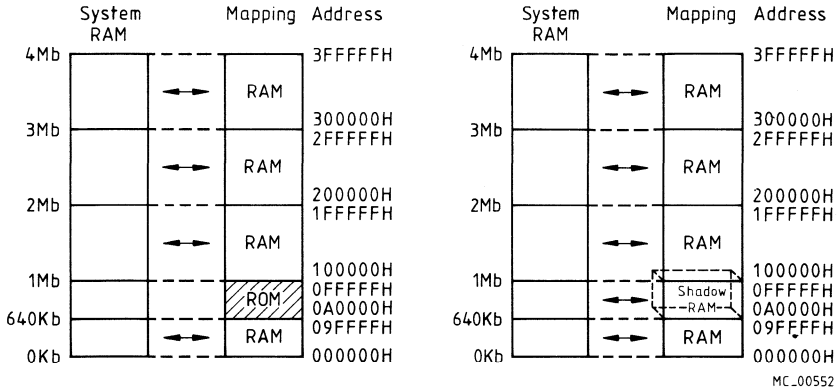
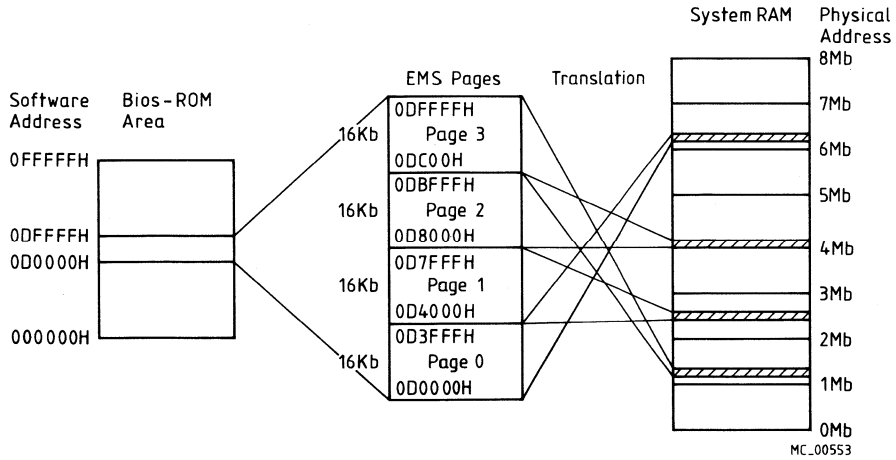


Figure 8
EMS Mapping



EMS Address Translation Logic

Expanded Memory System or EMS is a memory mapping scheme used to map a 64 Kbyte block of memory in the EPROM area D0000H-DFFFFH to anywhere in the 1 Mbyte - 8 Mbyte area. This 64 Kbyte memory block is segmented into four 16 Kbyte pages. Through a translation table, each 16 Kbyte segment can be mapped anywhere in the 1 Mbyte to 8 Mbyte area. Since the SAB 82C212 uses the translation table in the EMS mode, address lines A14 to A22 are translated by the appropriate EMS mapping register. Hence, this scheme does not require switching between user and protected mode. Figure 8 shows the EMS organization with a possible translation scheme. It is possible for the SAB 82C212 to map this 64 Kbyte block to anywhere in the 0 to 8 Mbyte area. However, it is desirable to map this block above the 1 Mbyte area in order to not use the RAM space in the 0 to 640 Kbyte area. Although the EMS scheme translates the 64 Kbyte block in the D0000H-DFFFFH area, it is possible to select a 64 Kbyte block from any other area.

Refresh Logic

During a refresh cycle, the SAB 82C211 outputs the refresh address on the A0-A9 address lines and asserts the REF# signal low to the SAB 82C212. The SAB 82C212 uses these signals to generate the refresh address on the MA0-MA9 address lines, the RAS# signals and LMEGCS#. The SAB 82C212 performs a staggered mode refresh to reduce the power supply noise generated during RAS# switching. Prior to a refresh, all RAS# lines are pulled high to ensure RAS# precharge. Following this RAS0# and RAS3# are asserted low. RAS1# and RAS2# are staggered by one delay unit using an external delay line, with respect to RAS0# and RAS3#. The RAS0#-RAS3#, RAS1#-RAS2# bundling is provided so that staggering is effective for a minimal 2 bank or a full 4 bank configuration.

Memory Configurations

It is possible to use 1-Mbit or 256-Kbit (and, in one case, 64-Kbit) DRAMs for system memory in the Siemens PC-AT Chipset. Each memory bank can be implemented with eighteen 1-bit wide DRAMs, or with four 4-bits wide plus two 1-bit wide DRAMs. Possible configurations for on-board memory are listed in table 2. Each bank is 16 bits wide plus two bits for parity. Page/interleaving is possible only for those combinations with similar pairs of DRAMs. In table 2, page/interleaving is possible with combinations 5, 6, 11, 13 and 14.

Table 2
Onboard Memory Configurations

	DRAM Type				Total	EMS
	Bank 0	Bank 1	Bank 2	Bank 3	Memory	Range
1	0	0	0	0	disable	0
2	256 K	0	0	0	512 Kbyte	0
3	1 M	0	0	0	2 Mbyte	1 Mbyte to 2 Mbyte
4	256 K	64 K	0	0	640 Kbyte	0
5	256 K	256 K	0	0	1 Mbyte	1 Mbyte to 1.384 Mbyte
6	1 M	1 M	0	0	4 Mbyte	1 Mbyte to 4 Mbyte
7	256 K	256 K	256 K	0	1.5 Mbyte	1 Mbyte to 1.5 Mbyte
8	256 K	256 K	1 M	0	3 Mbyte	1 Mbyte to 3 Mbyte
9	1 M	1 M	1 M	0	6 Mbyte	1 Mbyte to 6 Mbyte
10	256 K	64 K	256 K	256 K	1.64 Mbyte	1 Mbyte to 1.64 Mbyte
11	256 K	256 K	256 K	256 K	2 Mbyte	1 Mbyte to 2 Mbyte
12	256 K	64 K	1 M	1 M	4.64 Mbyte	1 Mbyte to 4.64 Mbyte
13	256 K	256 K	1 M	1 M	5 Mbyte	1 Mbyte to 5 Mbyte
14	1 M	1 M	1 M	1 M	8 Mbyte	1 Mbyte to 8 Mbyte

Clock Generation Logic

The SAB 82C212 has an oscillator circuit which uses a 14.31818 MHz crystal to generate the OSC and OSC/12 clocks. The 1.19381 MHz OSC/12 clock is used internally to generate the RAS# timeout clocks, one for each bank. RAS# is desserted for each bank when its RAS# timeout counter times out after about 10 Microseconds.

Configuration Registers

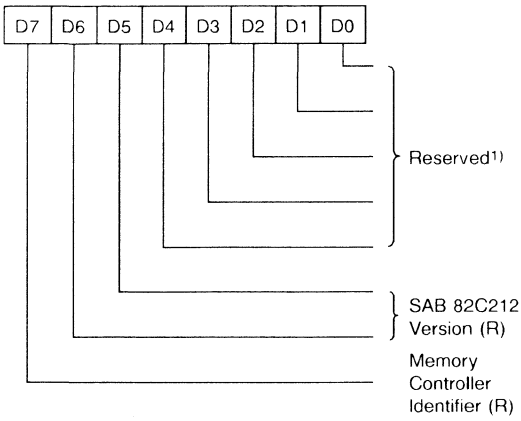
There are twelve configuration and diagnostics registers in the SAB 82C212, RB0-RB11. These are accessed through I/O ports 22 H and 23 H normally found in the interrupt controller module of the SAB 82C206 IPC. An indexing scheme is used to reduce the number of I/O addresses required to access all of the registers needed to configure and control the memory controller. Port 22 H is used as an index register that points to the required data value accessed through port 23 H. A write of the index value for the required data is performed to location 22 H. This is then decoded and controls the multiplexers gating the appropriate register to the output bus. Every access to port 23 H must be preceded by a write of the index value to port 22 H even if the same data register is being accessed again. All bits marked as "Reserved" are set to zero by default and must be maintained that way during write operations. Table 3 lists these registers.

Table 3
Indexes of Configuration Registers

Register Number	Register Name	Index
RB0	Version	64 H
RB1	ROM Configuration	65 H
RB2	Memory Enable-1	66 H
RB3	Memory Enable-2	67 H
RB4	Memory Enable-3	68 H
RB5	Memory Enable-4	69 H
RB6	Bank 0/1 Enable	6AH
RB7	DRAM Configuration	6BH
RB8	Bank 2/3 Enable	6CH
RB9	EMS Base Address	6DH
RB10	EMS Address Extension	6EH
RB11	Miscellaneous	6FH

Table 4
Version Register RB0

Index register port: 22 H
Data register port: 23 H
Index: 64 H

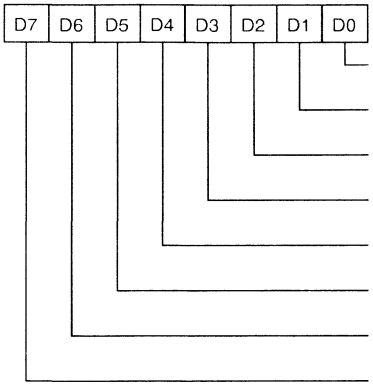


Bits	Function
7	NEAT memory controller identifier. 0 = SAB 82C212
6, 5	SAB 82C212 revision number. 00 = initial revision number
4-0	Reserved and default to 0[1].

1) The reserved bits are recommanded to be initialized to 1.

Table 5
ROM Configuration Register RB1

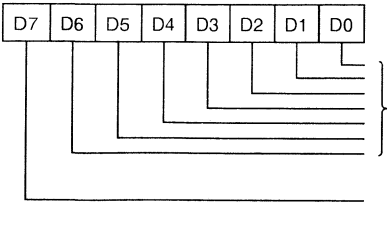
Index register port: 22 H
Data register port: 23 H (R/W)
Index: 65 H



Bits	Function
0	ROM at F0000H-FFFFH (BIOS). Default = 0 = ROM enabled. ROMCS# is generated.
1	ROM at E0000H-EFFFFH. Default = 1 = ROM disabled, Shadow RAM enabled. ROMCS# is not generated unless bit is set to 0.
2	ROM at D0000H-DFFFFH. Default = 1 = ROM disabled, Shadow RAM enabled. ROMCS# is not generated unless bit is set to 0.
3	ROM at C0000H-CFFFFH (EGA). Default = 1 = ROM disabled, Shadow RAM enabled. ROMCS# is not generated unless bit is set to 0.
4	Shadow RAM at F0000H-FFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected).
5	Shadow RAM at E0000H-EFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected).
6	Shadow RAM at D0000H-DFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected).
7	Shadow RAM at C0000H-CFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read only (Write protected).

Table 6
Memory Enable-1 Register RB2

Index register port: 22 H
Data register port: 23 H
Index: 66 H

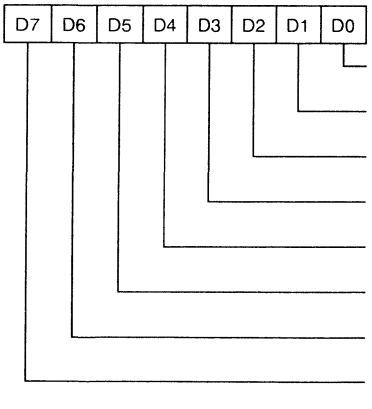


Bits	Function
0-6	Reserved and default to 0[1].
7	Address map RAM on system board in 80000H-9FFFFH area. 0 = Address is on the I/O channel (Default), 1 = Address is on the system board and is put out by the SAB 82C212.

[1] The reserved bits are recommanded to be initialized to 1.

Table 7
Memory Enable-2 Register RB3

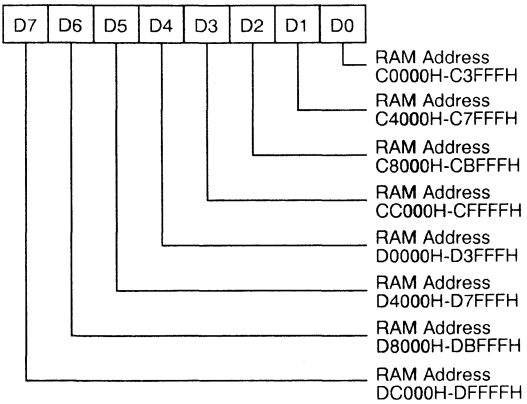
Index register port: 22 H
Data register port: 23 H (R/W)
Index: 67 H



Bits	Function
0	Enable Shadow RAM in B0000H-B3FFFH area. Disable = 0, Enable = 1.
1	Enable Shadow RAM in B4000H-B7FFFH area. Disable = 0, Enable = 1.
2	Enable Shadow RAM in B8000H-BBFFFH area. Disable = 0, Enable = 1.
3	Enable Shadow RAM in BC000H-BFFFFH area. Disable = 0, Enable = 1.
4	Enable Shadow RAM in A0000H-A3FFFH area. Disable = 0, Enable = 1.
5	Enable Shadow RAM in A4000H-A7FFFH area. Disable = 0, Enable = 1.
6	Enable Shadow RAM in A8000H-ABFFFH area. Disable = 0, Enable = 1.
7	Enable Shadow RAM in AC000H-AFFFFH area. Disable = 0, Enable = 1.

Table 8
Memory Enable-3 Register RB4

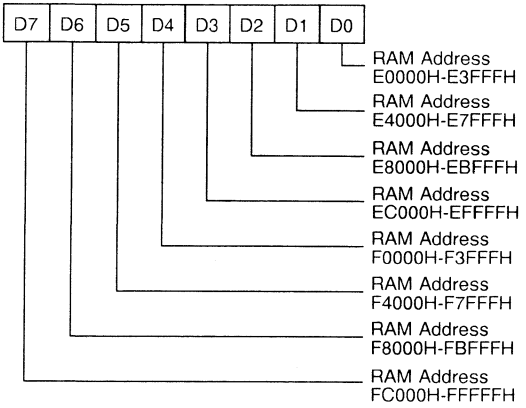
Index register port: 22 H
Data register port: 23 H (R/W)
Index: 68 H



Bits	Function
0	Enable Shadow RAM in C0000H-C3FFFH area. Disable = 0, Enable = 1.
1	Enable Shadow RAM in C4000H-C7FFFH area. Disable = 0, Enable = 1.
2	Enable Shadow RAM in C8000H-CBFFFH area. Disable = 0, Enable = 1.
3	Enable Shadow RAM in CC000H-CFFFFH area. Disable = 0, Enable = 1.
4	Enable Shadow RAM in D0000H-D3FFFH area. Disable = 0, Enable = 1.
5	Enable Shadow RAM in D4000H-D7FFFH area. Disable = 0, Enable = 1.
6	Enable Shadow RAM in D8000H-DBFFFH area. Disable = 0, Enable = 1.
7	Enable Shadow RAM in DC000H-DFFFFH area. Disable = 0, Enable = 1.

Table 9
Memory Enable-4 Register RB5

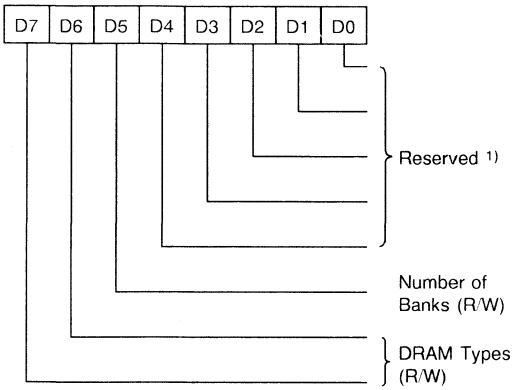
Index register port: 22 H
Data register port: 23 H (R/W)
Index: 69 H



Bits	Function
0	Enable Shadow RAM in E0000H-E3FFFH area. Disable = 0, Enable = 1.
1	Enable Shadow RAM in E4000H-E7FFFH area. Disable = 0, Enable = 1.
2	Enable Shadow RAM in E8000H-EBFFFH area. Disable = 0, Enable = 1.
3	Enable Shadow RAM in EC000H-EFFFFH area. Disable = 0, Enable = 1.
4	Enable Shadow RAM in F0000H-F3FFFH area. Disable = 0, Enable = 1.
5	Enable Shadow RAM in F4000H-F7FFFH area. Disable = 0, Enable = 1.
6	Enable Shadow RAM in F8000H-FBFFFH area. Disable = 0, Enable = 1.
7	Enable Shadow RAM in FC000H-FFFFFH area. Disable = 0, Enable = 1.

Table 10
Bank 0/1 Enable Register RB6

Index register port: 22 H
Data register port: 23 H
Index: 6AH



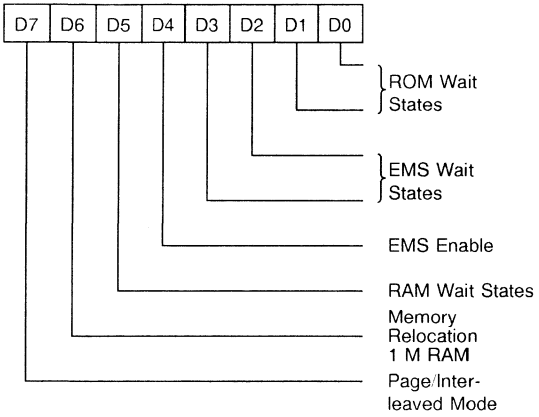
Bits	Function
0-4	Reserved and default to 0. 1)
5	Number of RAM banks used. 0 = one bank, non-interleaved mode (Default), 1 = two banks
7, 6	These bits contain the information for the DRAM types used on the system board. POST/BIOS should use the DRAM configuration data stored in the CMOS RAM of the SAB 82C206 IPC.

7	6	DRAM Types
0	0	Disabled
0	1	256 K and 64 K bit DRAMs used (for 640 Kbyte combination only)
1	0	256 K bit DRAMs used (Default)
1	1	1 Mbit DRAMs used

1) The reserved bits are recommanded to be initialized to 1.

Table 11
DRAM Configuration Register

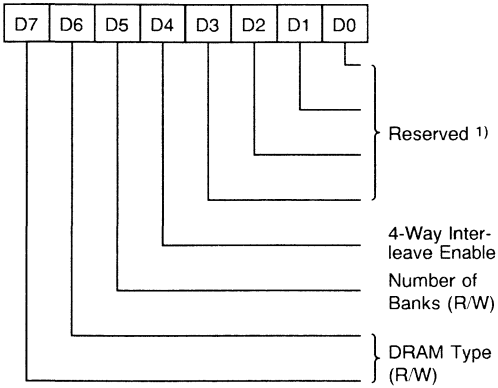
Index register port: 22 H
Data register port: 23 H (R/W)
Index: 6BH



Bits	Function		
1, 0	ROM access wait states control.		
	1	0	Wait States
	0	0	0
	0	1	1
	1	0	2
	1	1	3 (Default)
3, 2	EMS memory access wait states.		
	3	2	Wait States
	0	0	0
4	EMS enable bit. If set to 0, EMS is disabled (Default). If set to 1, EMS is enabled.		
5	RAM access wait states. If set to 0, accesses have 0 wait state. If set to 1 (Default), accesses will have 1 wait state.		
6	640 Kbyte to 1 Mbyte RAM relocation bit. A zero does not relocate local RAM. A one (Default) relocates local RAM from 0A0000-0FFFFF to 100000H-15FFFFH, provided total local RAM is 1 Mbyte only.		
7	Page/Interleaved mode enable. A 0 disables the page/interleaved mode, allowing useage of normal mode for the DRAMs (Default). A 1 enables page/interleaved mode for the DRAMs.		

Table 12
Bank 2/3 Enable Register RB8

Index register port: 22 H
Data register port: 23 H
Index: 6CH

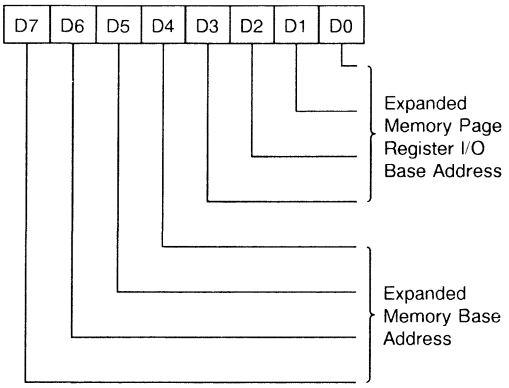


1) The reserved bits are recommanded to be initialized to 1.

Bits	Function		
3-0	Reserved and default to 0[1].		
4	A zero enables the 2-way page interleaved mode. A one (Default) enables the 4-way page interleaved mode if all 4 banks are the same DRAM devices.		
5	Number of local RAM banks used. 0 = one bank used, non-interleaved mode only (Default). 1 = two banks used.		
7, 6	These bits indicate the local DRAM type as listed:		
	7	6	DRAM Type
	0	0	none (Default)
	0	1	Reserved
	1	0	256 Kbit
	1	1	1 Mbit

Table 13
EMS Base Address Register RB9

Index register port: 22 H
Data register port: 23 H (R/W)
Index: 6DH



Bits	Function
0-3	These bits are used for the EMS page register I/O base address. The bits are encoded as follows, with unused combinations being reserved:

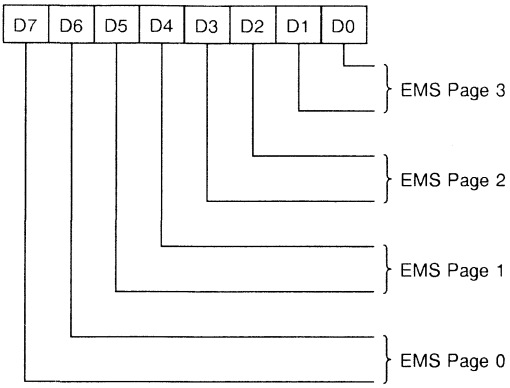
3	2	1	0	I/O Base
0	0	0	0	208H/209H
0	0	0	1	218H/219H
0	1	0	1	258H/259H
0	1	1	0	268H/269H
1	0	1	0	2A8H/2A9H
1	0	1	1	2B8H/2B9H
1	1	1	0	2E8H/2E9H

7-4 These bits are used for selecting the expanded memory base addresses. They are encoded as follows, with all unused combinations being reserved:

7	6	5	4	EMS Base Addresses
0	0	0	0	C0000H,C4000H, C8000H,CC000H
0	0	0	1	C4000H,C8000H, CC000H,D0000H
0	0	1	0	C8000H,CC000H, D0000H,D4000H
0	0	1	1	CC000H,D0000H, D4000H,D8000H
0	1	0	0	D0000H,D4000H, D8000H,DC000H
0	1	0	1	D4000H,D8000H, DC000H,E0000H
0	1	1	0	D8000H,DC000H, E0000H,E4000H
0	1	1	1	DC000H,E0000H, E4000H,E8000H
1	0	0	0	E0000H,E4000H, E8000H,EC000H

Table 14
EMS Extension Register RB10

Index register port: 22 H
Data register port: 23 H (R/W)
Index: 6EH

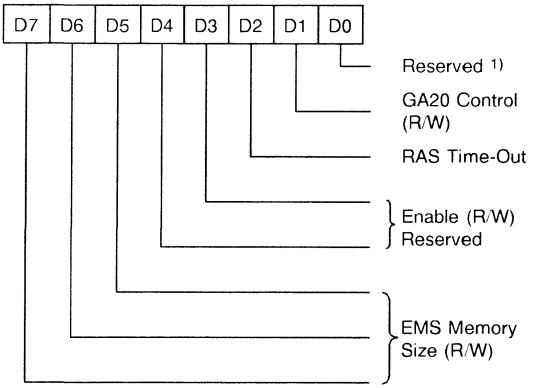


Bits	Function	
1(A22) 0(A21)	EMS Page 3 address extension bits.	
	1 0	Block of EMS Memory
	0 0 0 1 1 0 1 1	0 Mbyte to 2 Mbyte 2 Mbyte to 4 Mbyte 4 Mbyte to 6 Mbyte 6 Mbyte to 8 Mbyte
3(A22) 2(A21)	EMS Page 2 address extension bits.	
	3 2	Block of EMS Memory
	0 0 0 1 1 0 1 1	0 Mbyte to 2 Mbyte 2 Mbyte to 4 Mbyte 4 Mbyte to 6 Mbyte 6 Mbyte to 8 Mbyte
5(A22) 4(A21)	EMS Page 1 address extension bits.	
	5 4	Block of EMS Memory
	0 0 0 1 1 0 1 1	0 Mbyte to 2 Mbyte 2 Mbyte to 4 Mbyte 4 Mbyte to 6 Mbyte 6 Mbyte to 8 Mbyte
7(A22) 6(A21)	EMS Page 0 address extension bits.	
	7 6	Block of EMS Memory
	0 0 0 1 1 0 1 1	0 Mbyte to 2 Mbyte 2 Mbyte to 4 Mbyte 4 Mbyte to 6 Mbyte 6 Mbyte to 8 Mbyte

Address lines A22 and A21 are used in EMS Address translation logic.

Table 15
Miscellaneous Register RB11

Index register port: 22 H
Data register port: 23 H
Index: 6FH



1) The reserved bits are recommanded to be initialized to 1.

Bits	Function
0	Reserved and default to 0[1].
1	This bit is used for address line A20 control and provides OS/2 optimization while switching between real and protected modes: If the bit is set to 0 it enables A20 onto GA20. The bit default to 1 and sets GA20 = 0.
2	This bit is used to enable the RAS# time-out counter for page mode operation. The counter is disabled if set to 0 (Default) and is enabled if set to 1.
3, 4	Reserved and default to 1 (bit 4), 0 (bit 3).
7-5	These bits are used to set the EMS memory space according to the following coding:

7	6	5	EMS Memory Size
0	0	0	less than 1 Mbyte
0	0	1	1 Mbyte
0	1	0	2 Mbytes
0	1	1	3 Mbytes
1	0	0	4 Mbytes
1	0	1	5 Mbytes
1	1	0	6 Mbytes
1	1	1	7 Mbytes

Table 16
EMS Page Registers

Page 0: 2X8/2X9H
Page 1: 42X8/42X9H
Page 2: 82X8/82X9H
Page 3: C2X8/C2X9H

X can be 0, 1, 5, 6, A, B, E

Bits	Function
0-6	0 - A14 1 - A15 2 - A16 3 - A17 4 - A18 5 - A19 6 - A20
7	0 - page disable 1 - page enable

Absolute Maximum Ratings

Ambient temperature under bias . . . . . 0 to 70 °C
Storage temperature . . . . . – 65 to + 150 °C
Supply voltage . . . . . – 0.5 to + 7.0 V
Voltage on any pin with respect to ground . . . . . – 0.5 to V_{CC} + 0.5 V
Power dissipation . . . . . 1 W

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	–	0.8	V	–
Input high voltage	V_{IH}	2.0	–	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 4 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = –4 mA
Input leakage current	I_{IL}	–	+ 10	µA	0 V < V_{IN} < V_{CC}
Power supply current	I_{CC}	–	75	mA	@16 MHz
Output tristate leakage current	I_{OZ1}	–	+ 10	µA	0.45 V < V_{OUT} < V_{CC}
Standby power supply current	I_{CCSB}	–	1.0	mA	–

AC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ±5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
RASi# active delay from CLK2 ↓	t_1	11	16	ns	–
RASi# inactive delay from CLK2 ↓	t_2	15	25	ns	–
DLYOUT active delay from RASi# ↓	t_3	0	4	ns	–
DLYOUT inactive delay from RASi# ↑	t_4	0	6	ns	–
Column address stable from DLY0 ↑	t_5	8	18	ns	–
Column address hold from DLY0 ↓	t_6	6	–	ns	–
CASi# active delay from DLY1 ↑	t_7	7	14	ns	–
CASi# inactive delay from DLY1 ↓	t_8	11	18	ns	–
AF16# active delay from CLK2 ↓	t_9	7	19	ns	SAB 82C212-12
		7	16	ns	SAB 82C212-16
AF16# inactive delay from CLK2 ↓	t_{10}	8	21	ns	SAB 82C212-12
		8	18	ns	SAB 82C212-16
READY# active delay from CLK2 ↓	t_{11}	15	25	ns	–
READY# inactive delay from CLK2 ↓	t_{12}	11	20	ns	–
DRD# active delay from CLK2 ↓	t_{13}	10	19	ns	–
DRD# hold from DLE ↓	t_{14}	13	–	ns	–
DLE active delay from DLY1# ↓	t_{15}	6	16	ns	–
DLE inactive delay from CLK2 ↓	t_{16}	9	18	ns	–
LMEGCS# active from CLK2 ↓	t_{17}	12	21	ns	–
LMEGCS# inactive from CLK2 ↓	t_{18}	11	20	ns	–
GA20 valid delay from CPU A20 valid	t_{19}	7	20	ns	SAB 82C212-12
		7	16	ns	SAB 82C212-16
GA20 invalid delay from CPU A20 invalid	t_{20}	4	16	ns	SAB 82C212-12
		4	12	ns	SAB 82C212-16
MWE# active delay from CLK2 ↓	t_{22}	11	20	ns	–
MWE# inactive delay from CLK2 ↑	t_{23}	4	12	ns	–
CASi# active delay from CLK2 ↓	t_{26}	10	25	ns	SAB 82C212-12
		10	19	ns	SAB 82C212-16
CASi# inactive delay from CLK2 ↓	t_{27}	11	26	ns	SAB 82C212-12
		11	21	ns	SAB 82C212-16

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
DRD# inactive delay from CLK2 ↓	t_{28}	12	23	ns	–
CASi# inactive delay from DLE inactive	t_{29}	2	–	ns	–
RASi# active delay from CLK2 ↓	t_{30}	10.5	16	ns	–
Row address setup time to RASi# ↓	t_{31}	8	–	ns	–
Row address hold time from CLK2 ↓	t_{32}	6	22	ns	–
RASi# inactive delay from CLK2 ↓	t_{33}	15	25	ns	–
RASi# precharge time (interleaved mode)	t_{34}	4 × CLK2	–	–	–
ROMCS# active from CLK2 ↓	t_{35}	11	20	ns	–
ROMCS# inactive from CLK2 ↓	t_{36}	10	20	ns	–
DLE hold time from DRD# ↑	t_{37}	0	7	ns	–
RAS0-3# inactive from REF# ↓	t_{38}	13	24	ns	–
RAS0,3# active from XMEMR# ↓	t_{39}	9	17	ns	–
RAS0,3# inactive from XMEMR# ↑	t_{40}	10	19	ns	–
RAS1,2# active from RAS0,3# ↓	t_{41}	7	15	ns	–
RAS1,2# inactive from RAS0,3# ↑	t_{42}	11	20	ns	–
Address setup time from XMEMR# ↓	t_{43}	10	–	ns	–
Address hold time from REF# ↑	t_{44}	4	–	ns	–
Refresh address delay	t_{45}	0	–	ns	–
LMEGCS# delay from REF# ↓	t_{47}	8	16	ns	–
LMEGCS# delay from REF# ↑	t_{48}	10	19	ns	–
RAS0-3# inactive from HLDA1 ↑	t_{49}	11	20	ns	–
RASi# active from command active	t_{50}	10	18	ns	–
RASi# inactive from command inactive	t_{51}	12	21	ns	–
Column address stable from DLY0 ↑	t_{54}	9	18	ns	–
CASi# active delay from DLY1 ↑ (while XMEMW# active)	t_{55}	6	14	ns	–
CASi# inactive delay from command inactive	t_{56}	9	18	ns	–
AF16# active from command active	t_{57}	9	17	ns	–
AF16# inactive from command inactive	t_{58}	6	14	ns	–

Figure 9
Read Timing, 0 WS, Non-Interleaved Mode

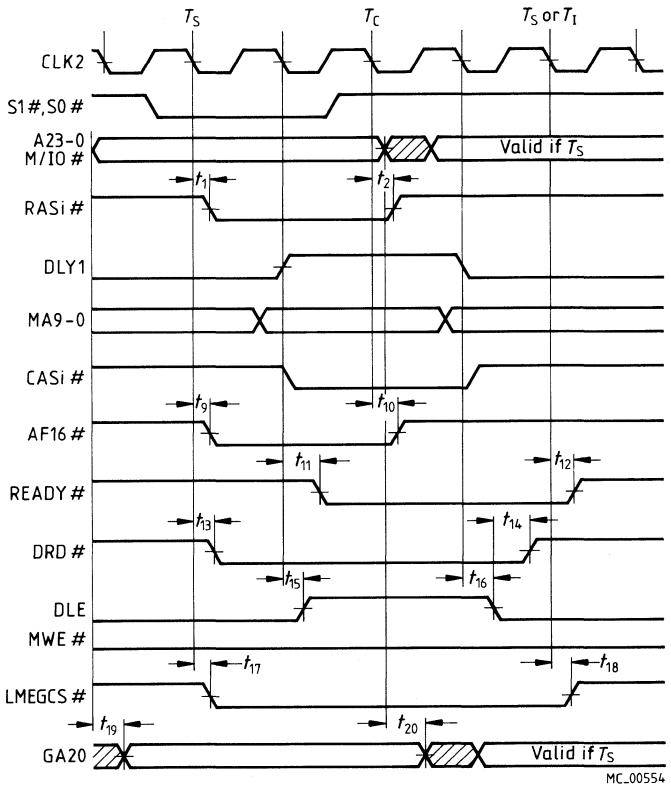


Figure 10
Write-Followed by Read-Timing, 0 WS, Non-Interleaved Mode

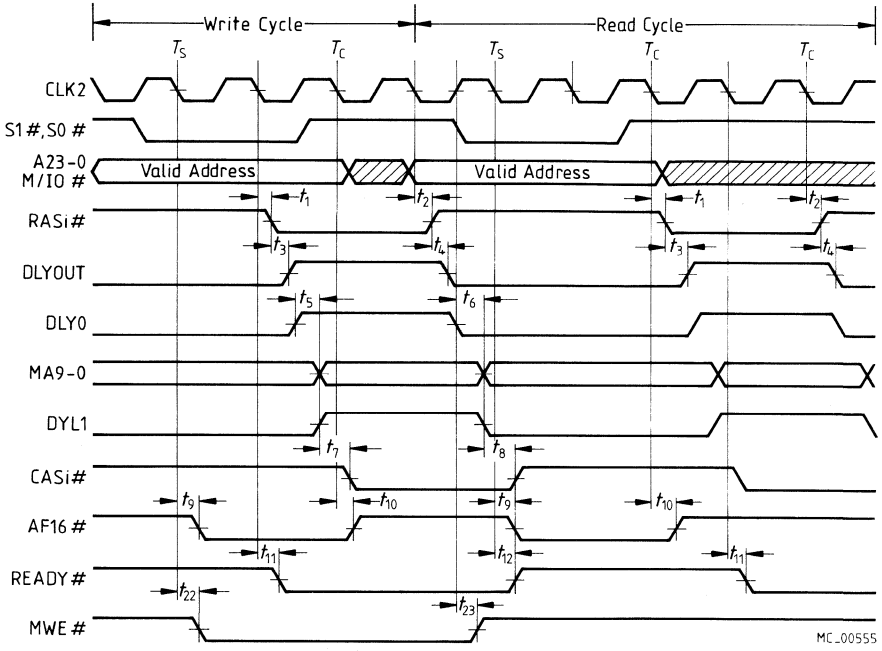


Figure 11
Write Cycle, 0 WS, Non-Interleaved Mode

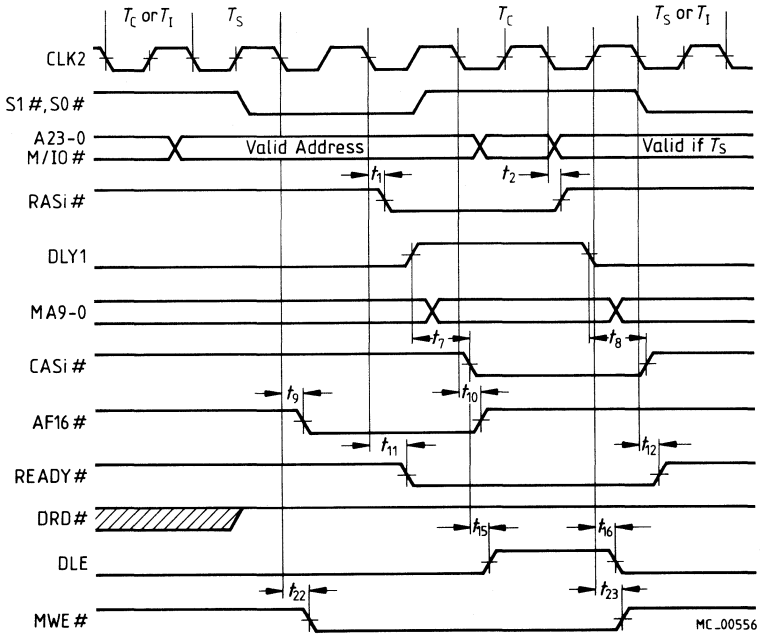


Figure 12
Read/Write, 1 WS, Non-Interleaved Mode

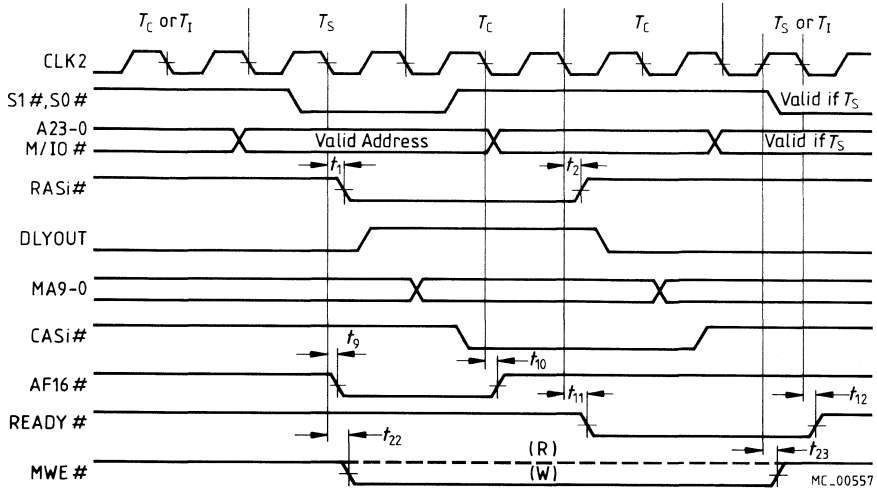


Figure 13
Write Cycle with RAS# Being Inactive, 0 WS, Interleaved Mode

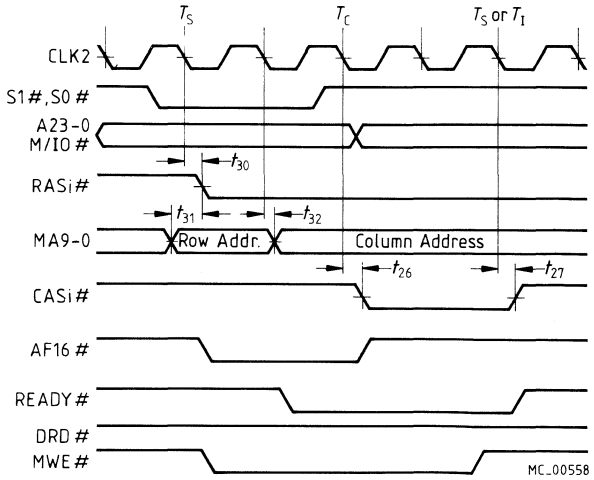


Figure 14
Read Cycle with RAS# Being Inactive, 0 WS, Interleaved Mode

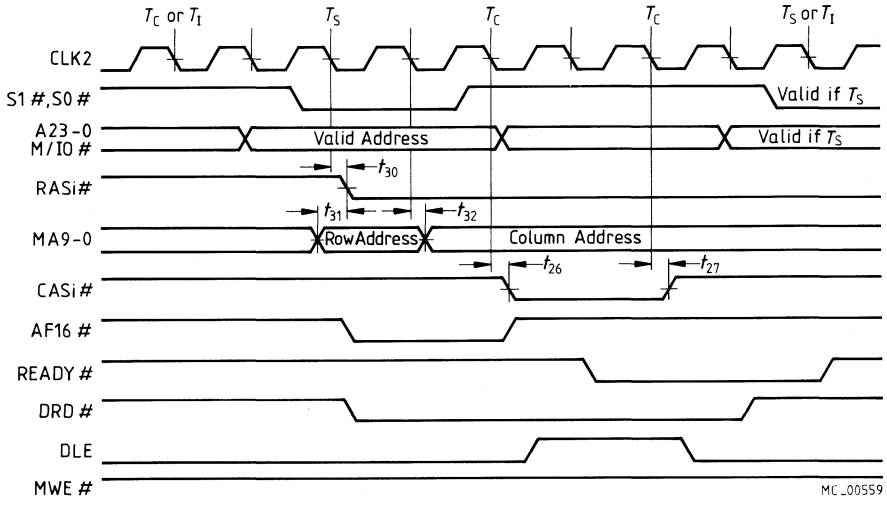


Figure 15
Write Cycle, 0 WS (RAS# active), Interleaved Mode

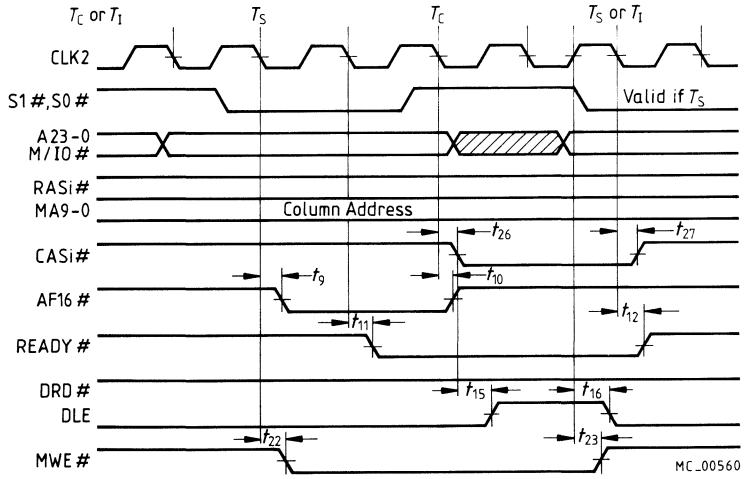


Figure 16
Read after Write, 0 WS (RAS# active), Interleaved Mode

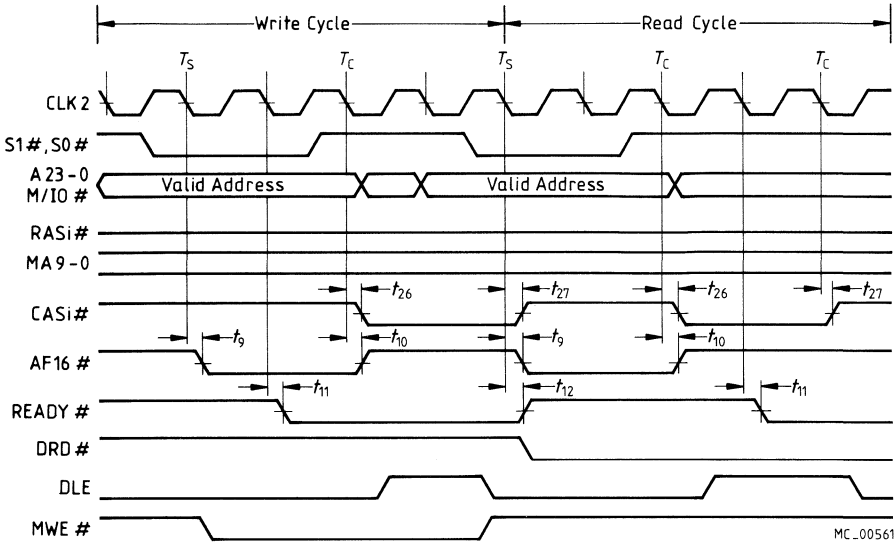


Figure 17
Read Cycle, 0 WS (RAS# active), Interleaved Mode

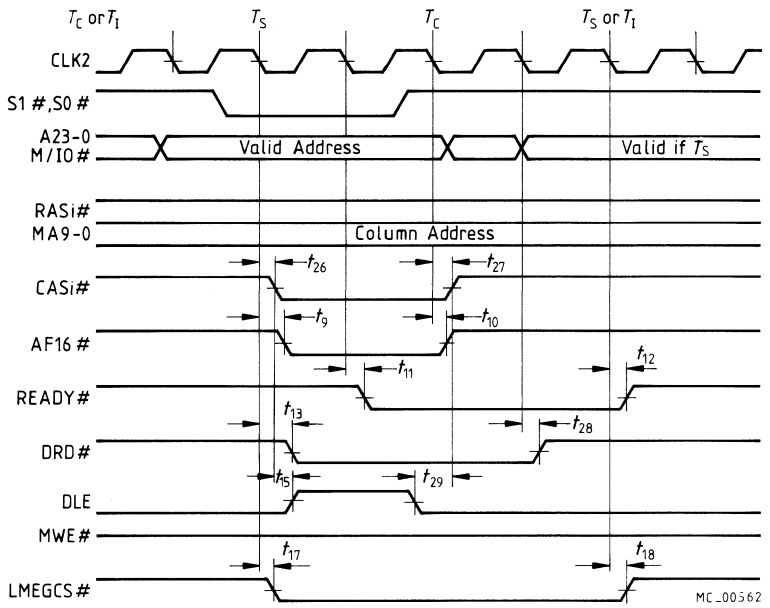


Figure 18
Read Miss Cycle, Interleaved Mode

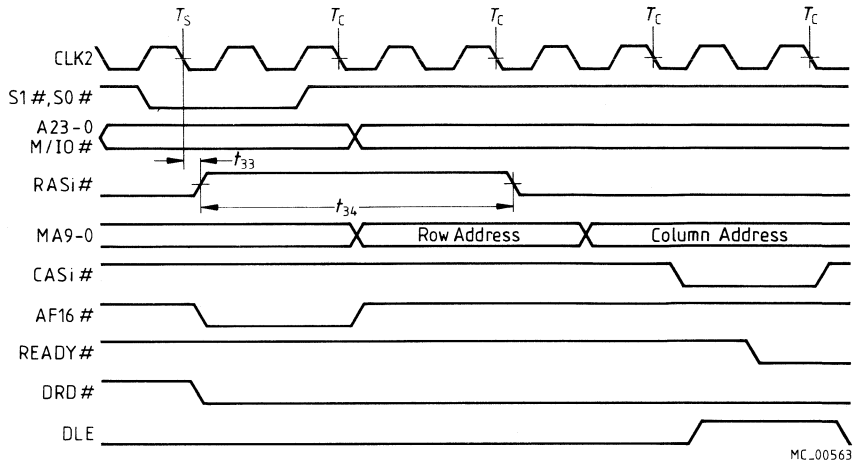


Figure 19
ROM Read Cycle

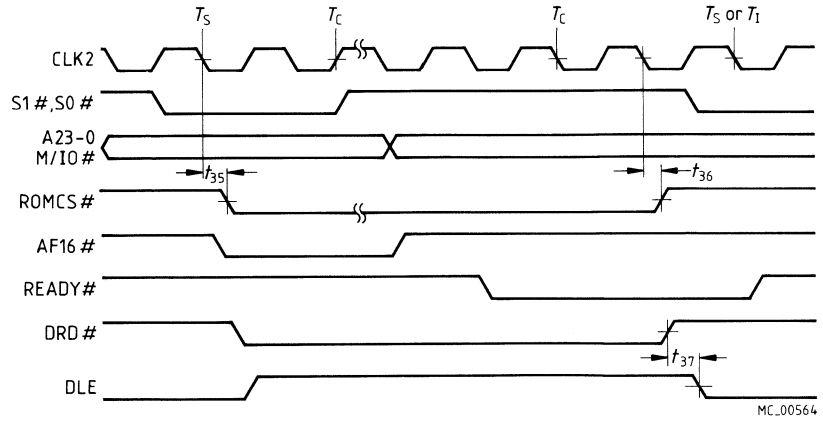


Figure 20
Refresh Cycle

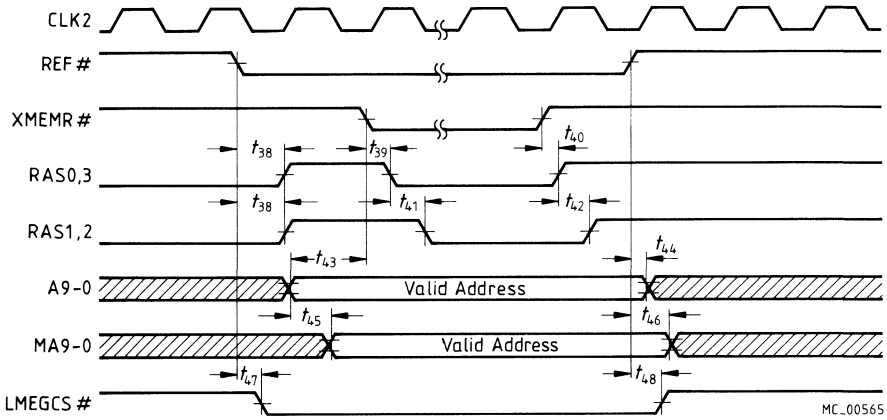


Figure 21
DMA Cycle

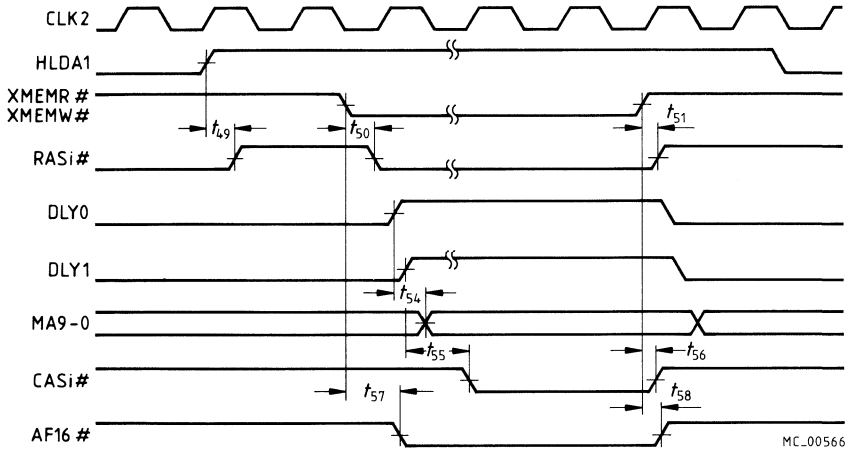
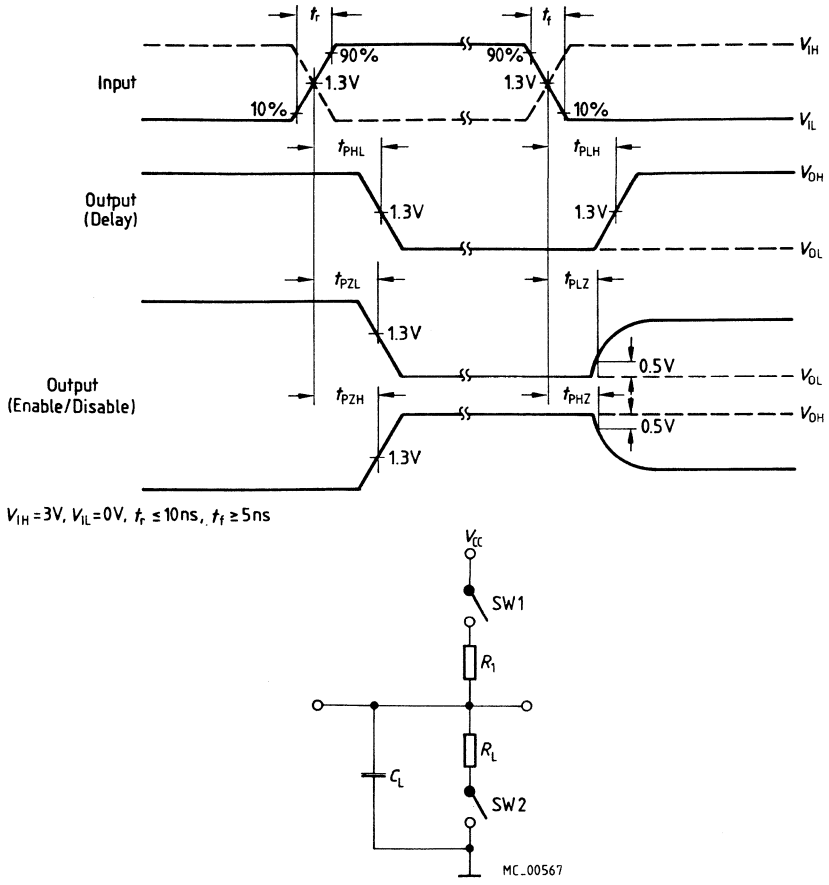


Figure 22
Load Circuit and AC Characteristics Measurement Waveform



V_{IH}=3V, V_{IL}=0V, $t_r \leq 10$ns, $t_f \geq 5$ns

Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L (pF)	R_1 (kΩ)	R_L (kΩ)	SW_1	SW_2
Propagation	Totem Pole						
Delay Time	Tristate	t_{PLH}	50	–	1.0	OFF	ON
	Bidirectional	t_{PHL}	50	–	1.0	OFF	ON
Propagation	Open Drain or	t_{PLH}	50	0.5	–	ON	OFF
Delay Time	Open Collector	t_{PHL}	50	0.5	–	ON	OFF
Disable Time	Tristate	t_{PLZ}	5	0.5	1.0	ON	
	Bidirectional	t_{PHZ}	5	0.5	1.0	OFF	ON
Enable Time	Tristate	t_{PZL}	50	0.5	1.0	ON	ON
	Bidirectional	t_{PZH}	50	0.5	1.0	OFF	ON

SIEMENS

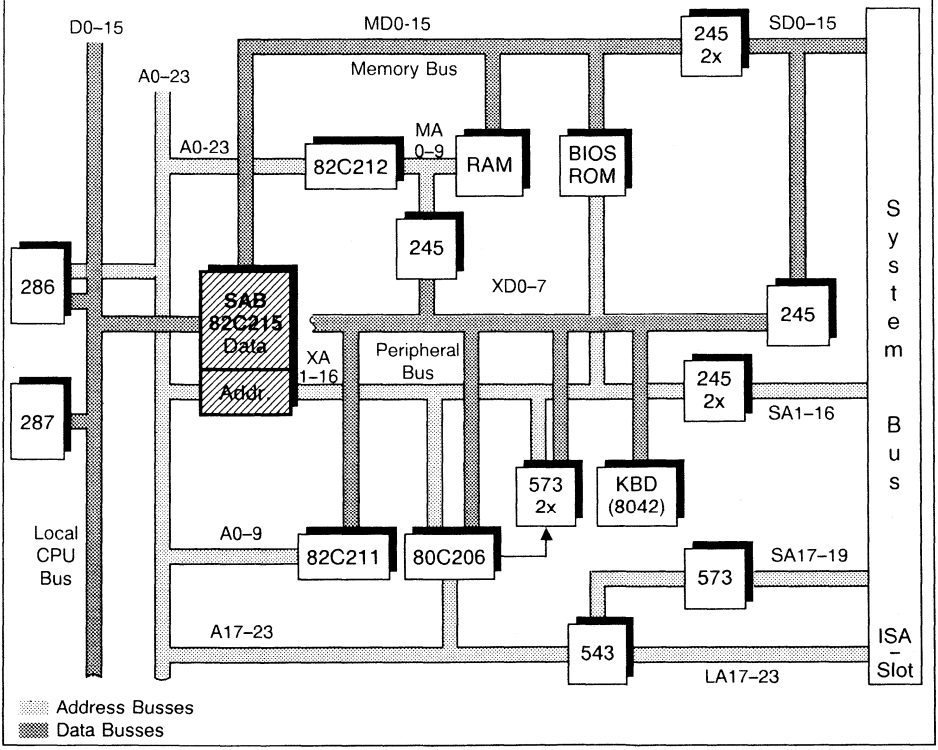
Data / Address Buffer of Siemens PC-AT™ Chipset

SAB 82C215

Advance Information

- Address buffer and latch for local CPU- and X-address bus interface
- Data buffer and latch for local CPU data bus / memory data bus interface
- Bus conversion logic for 16-bit to 8-bit transfers
- Parity generation / detection logic for memory data bus
- CMOS implementation for high speed and low power requirements
- 84-pin plastic leaded chip carrier package (PL-CC-84)

Siemens PC-AT Chipset



As a member of the Siemens PC-AT Chipset the SAB 82C215 provides address buffer / latch, data bus buffer / latch, data bus path conversion logic and parity logic.

The SAB 82C215 data / address buffer, the SAB 82C211 system controller, the SAB 82C212 memory controller and the SAB 82C206 integrated peripheral controller provide a highly integrated high performance system solution for PC-AT compatible systems.

The SAB 82C215 is fabricated in Siemens ACMOS technology and packaged in a 84-pin plastic leaded chip carrier package (PL-CC-84).

Ordering Information

Type	Ordering code	Package	Description
SAB 82C215-12-N	Q67120-P297	PL-CC-84 (SMD)	Data / Address Buffer of Siemens PC-AT Chipset (12 MHz)
SAB 82C215-16-N	Q67120-P298	PL-CC-84 (SMD)	Data / Address Buffer of Siemens PC-AT Chipset (16 MHz)

Figure 1
Logic Symbol

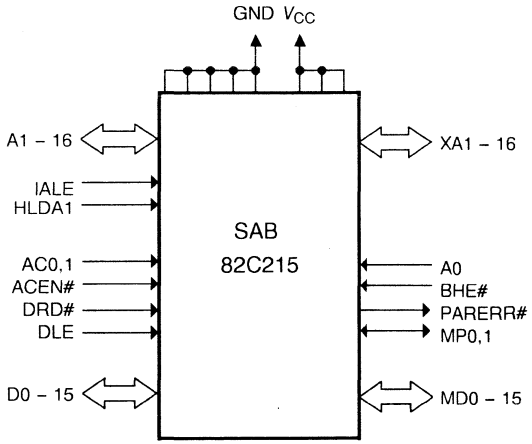
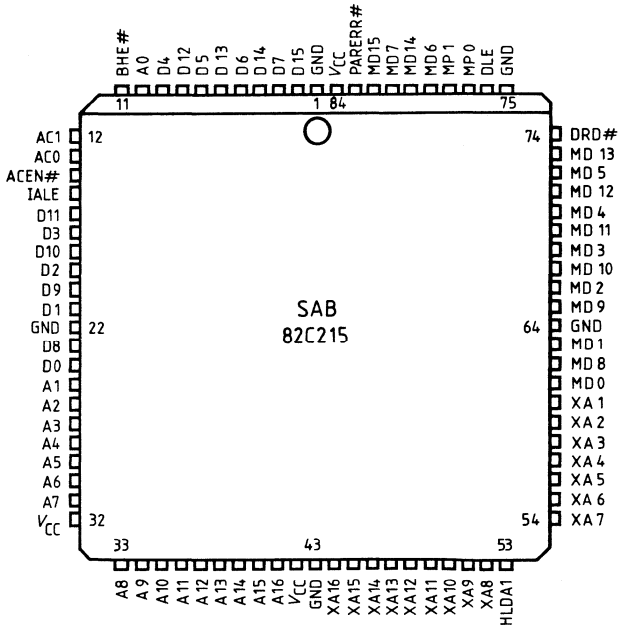


Figure 2
Pin Configuration



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
Address Latch / Buffers			
IALE	15	I	**Address Latch Enable** IALE is the strobe input line of the address latch. It is used to latch the CPU addresses onto the X-address lines.
A1 – A16	25 – 31 33 – 41[1]	I/O	**CPU Address Lines 1 – 16** During CPU cycles (HLDA1 = 0) A1 – A16 are the inputs to the internal address latch of the SAB 82C215. During DMA cycles (HLDA1 = 1) A1 – A16 are outputs. The address latch is controlled by IALE.
XA1 – XA16	60 – 54 52 – 44[1]	I/O	**XBUS Address Lines 1 – 16** During CPU cycles (HLDA1 = 0) XA1 – 16 are the outputs of the address latch. During DMA cycles (HLDA1 = 1) XA1 – 16 are inputs.
HLDA1	53	I	**Hold Acknowledge** HLDA1 indicates the type of cycle currently executing. CPU cycles are executed with HLDA1 = 0. During DMA cycles HLDA1 = 1. HLDA1 controls the direction of the address and data bus transfers.
Data Buffers / Latch			
D0 – D15	24, 23 21 – 16 9 – 2[1]	I/O	**CPU Data Bus Lines 0 – 15** D0 – D15 represent the local CPU data bus lines. The data bus buffers are controlled by HLDA1 and DRD#.
AC0,1	13, 12	I	**Action Code Line 0, 1** The two action code lines control the data path during CPU and DMA cycles. AC0,1 are qualified (enabled) by the ACEN# signal. At the Siemens PC-AT chipset AC0,1 are generated by the SAB 82C211.

[1] For detailed pin numbers see also pin configuration (figure 2).

Pin Definitions and Functions (cont'd)

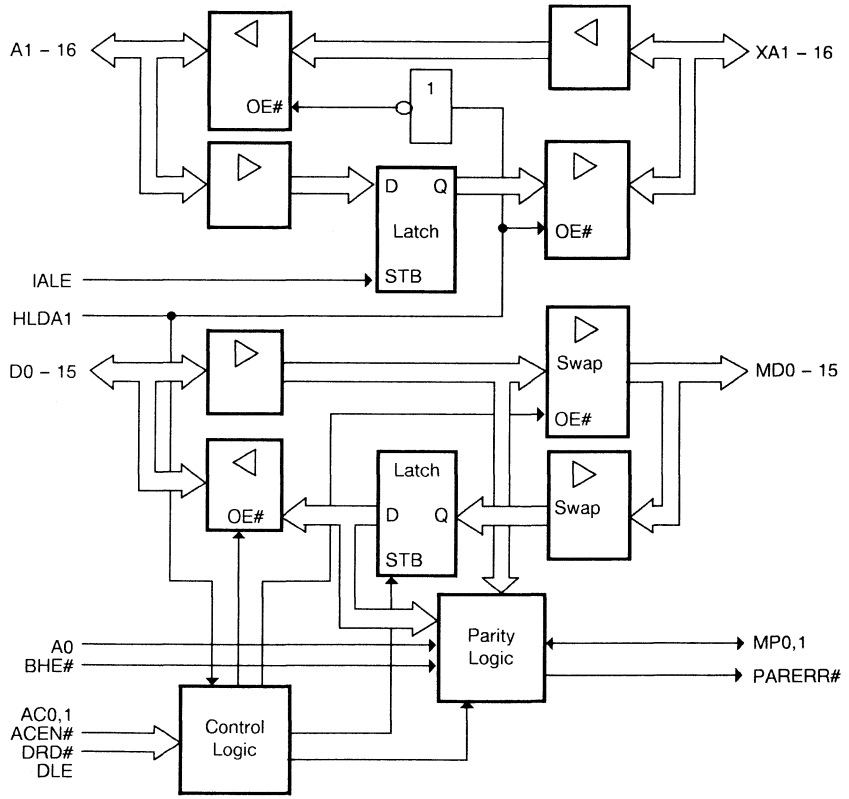
Symbol	Pin	Input (I) Output (O)	Function
Data Buffers / Latch			
ACEN#	14	I	**Action Code Enable#** ACEN# = 0 validates the action code signals AC0,1.
MD0 – MD15	61 – 63 65 – 73 79 – 82[1)]	I/O	**Memory Data Bus 0 – 15** MD0 – MD15 are the memory data bus lines. They are controlled by HLDA1, DRD#, AC1,0 and ACEN#.
DRD#	74	I	**Data Read#** DRD# controls the direction of the data bus buffer path. DRD# = 1 sets the data path from local CPU bus to memory bus. DRD# = 0 sets the data path from memory to local CPU bus.
DLE	76	I	**Data Latch Enable** DLE controls the data bus latch. Memory bus data is stored in the latch with the high-to-low transition of DLE.
Parity Generator / Checker			
A0	10	I	**Address Line 0** A0 is used to enable the low byte parity checking.
BHE#	11	I	**Byte High Enable#** BHE# is used to enable the high byte parity checking.
MP1, MP0	78, 77	I/O	**Memory Parity Bit 1,0** MP1 and MP0 are the parity bits for the high and low order bytes of the system DRAM's. These lines are inputs during memory read operations for parity error detection and are outputs during memory write operations for parity generation.
PARERR#	83	O	**Parity Error#** PARERR# = 0 indicates that a parity error has been detected during a system memory read operation. At the Siemens PC-AT chipset PARERR# is checked by the SAB 82C211 system controller.

1) For detailed pin numbers see also pin configuration (figure 2).

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
Power Supply			
V_{CC}	32, 42, 84	–	**Power Supply** (+ 5 V)
GND	1, 22, 43, 64, 75	–	**Ground** (0 V)

Figure 3
Block Diagram



Functional Description

The SAB 82C215 data / address buffer for the SIEMENS PC-AT chipset provides the following functional units:

- Address buffer and latch
- Data buffer and latch
- Data bus conversion logic
- Parity generation / detection logic

Address Buffer and Latch

For local CPU cycles (HLDA1 = 0) the SAB 82C215 provides the address buffering and latching between the CPU address lines A1 – A16 and the peripheral bus address lines XA1 – XA16. A1 – A16 can be latched by the address latch enable signal IALE. The latch is transparent with IALE = high.

During DMA cycles (HLDA1 = 1) the peripheral address bus XA1 – XA16 is routed to the A1 – A16 address bus lines. The address latch is not available during DMA cycles.

Data Buffer and Latch

The SAB 82C215 provides the buffering between the CPU data bus D0 – D15 and the memory data bus MD0 – MD15 for local cycles (on-board memory read / write cycles) or AT-bus cycles (on-board peripherals or AT-slot read / write cycles).

DRD# is the direction control signal for the data buffer. For local write cycles DRD# is at high level and sets the data path from the CPU data bus to the memory data bus. For local read cycles DRD# = 0 sets the data path from MD-bus to D-bus. DLE controls the data latch. DLE = 1 makes the latch transparent. During local cycles the action code enable signal is inactive (ACEN# = 1).

During AT-bus cycles DLE is inactive (low), and instead of DLE the ACEN# signal is used to strobe the data into the data latch. With ACEN# = 0 the data latch is transparent and data is stored with the low-to-high transition of ACEN#.

During DMA cycles the D-bus of the SAB 82C215 is switched off. During DMA memory write operations (AC1,0 = 0,0 and 1,0), the MD-bus lines are connected to the parity generator. If data bus conversion is required during DMA cycles (AC1,0 = 1,0 and 1,1), the corresponding data path is set between MD0 – 7 and MD8 – 15.

Data Bus Conversion Logic

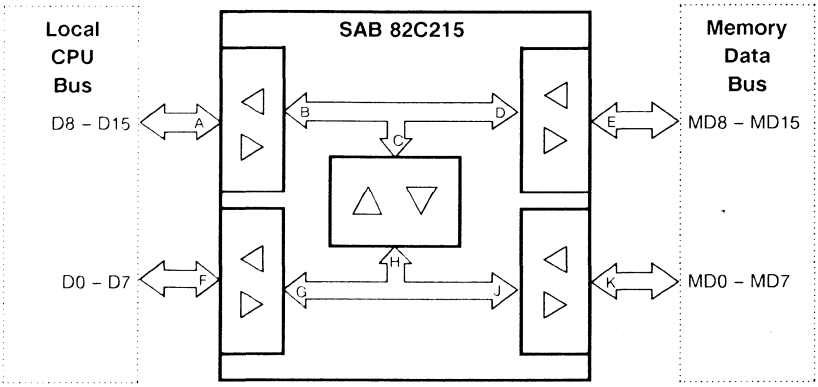
The SAB 82C215 provides data bus conversion when the 16-bit CPU reads from or writes to 8-bit devices. It also provides data bus conversion for DMA cycles. Table 1 lists the possible cases of the data paths for CPU and DMA cycles. The action code signals AC1, 0, which are qualified by ACEN#, control the different data path configurations.

Table 1:
Action Code Functions

AC1	AC0	HLDA1	Operation	Data path 1)
0	0	0	16-bit Write	A-B-D-E and F-G-J-K
			8-bit Low Write	F-G-J-K
0	1	0	16-bit Read	E-D-B-A and K-J-G-F
			8-bit Low Read	K-J-G-F
1	0	0	8-bit High Write to MD-bus low	A-B-C-H-J-K
1	1	0	8-bit Read MD-bus Low to D-bus high	K-J-H-C-B-A
0	0	1	MD-bus tristated: 16-bit/8-bit (low byte) DMA read / write at MD-bus	–
0	1	1	reserved	–
1	0	1	High memory Write to MD8 – 15 from MD0 – 7	K-J-H-C-D-E
1	1	1	High memory Read from MD8 – 15 to MD0 – 7	E-D-C-H-J-K

1) see figure 4

Figure 4
Data Bus Conversion Paths



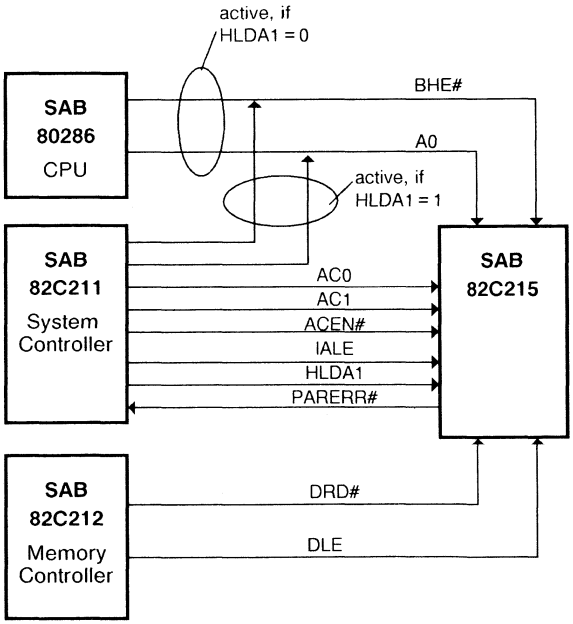
Parity Generation / Detection Logic

For local memory write cycles the SAB 82C215 generates an even parity bit (MP0, MP1) for each of the two data bytes MD0 – 7 and MD8 – 15. The parity bit is set if the corresponding data byte has an even number of 1's. During local memory read cycles the SAB 82C215 checks the data bytes for even parity. If a parity error is detected, the PARERR# output becomes active (low). PARERR# is activated by the falling edge of DLE and deactivated by the rising edge of DRD#. For DMA cycles (HLDA1 = 1) the parity checker is disabled. During parity checking A0 and BHE# select the data bytes to be checked.

SAB 82C215 control lines interface

The SAB 82C215 has several control lines. In a PC-AT design using the Siemens PC-AT chipset the interface of the SAB 82C215 control lines is shown in the next figure.

Figure 5
Interface of the SAB 82C215 control lines in the Siemens PC-AT Chipset



Absolute Maximum Ratings

Ambient temperature under bias ..... 0 to 70 °C
Storage temperature ..... - 65 to + 150 °C
Supply voltage ..... - 0.5 to + 7.5 V
Voltage on any pin with respect to ground ..... - 0.5 to V_{CC} + 0.5 V
Power dissipation ..... 1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = + 5 V ± 5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	– 0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	MD0 – 15: I_{OL} = 8 mA other outputs: I_{OL} = 4 mA
Output high voltage	V_{OH}	2.4	–	V	MD0 – 15: I_{OH} = - 8 mA other outputs: I_{OH} = - 4 mA
Input leakage current	I_{IL}	–	± 10	µA	0 V < V_{IN} < V_{CC}
Output tristate leakage current	I_{OZ}	–	± 10	µA	0.45 V < V_{OUT} < V_{CC}
Power supply current	I_{CC}	–	80	mA	@16 MHz
Standby power supply current	I_{CCSB}	–	1.0	mA	–

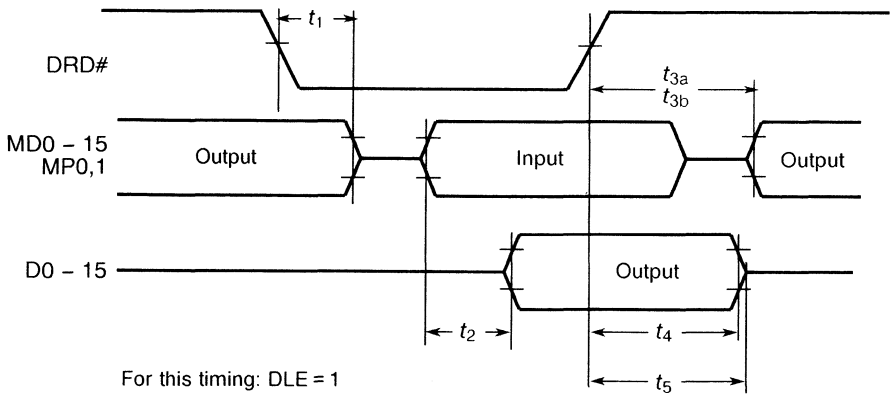
AC Characteristics

T_A = 0 to 70 °C; V_{CC} = +5 V ± 5 %; GND = 0 V

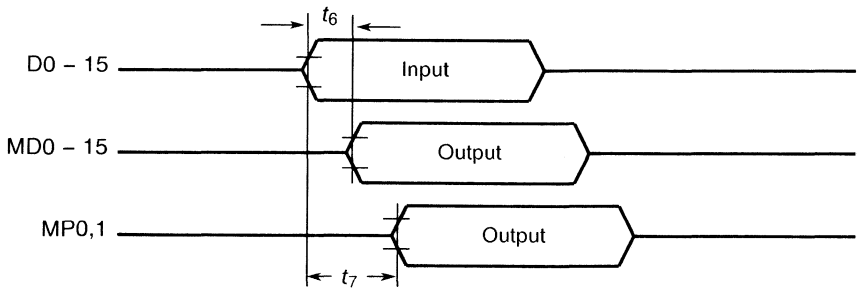
Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
MD-bus tristated after DRD# active	t_1	7.5	24	ns	–
MD-bus valid to D-bus valid	t_2	8	18.5	ns	–
MD-bus being driven after DRD# inactive	t_{3a}	7.5	28	ns	–
MP0, MP1 being driven after DRD# inactive	t_{3b}	6	23	ns	–
D-bus invalid after DRD# inactive	t_4	4	13	ns	–
D-bus tristated after DRD# inactive	t_5	6	15	ns	–
D-bus valid to MD-bus valid	t_6	11	19	ns	–
D-bus valid to MP1, MP0 valid	t_7	11	20	ns	–
ACEN# active to D-bus valid	t_8	16	27	ns	–
Action code valid to MD-bus valid	t_9	10	19	ns	–
Action code invalid to MD-bus invalid	t_{10}	11	20	ns	–
DLE inactive to PARERR# enabled	t_{11}	17	30	ns	–
DRD# inactive to PARERR# disabled	t_{12}	17	28	ns	–
IALE active to XA-bus valid	t_{13}	11	19	ns	–
XA-bus valid to A-bus valid SAB 82C215-12 SAB 82C215-15	t_{14}	7 7	19 16	ns ns	– –
MD, MP setup time to DLE trailing edge	t_{15}	0	–	ns	–
MD, MP hold time from DLE trailing edge	t_{16}	6	–	ns	–
DRD# setup time to DLE trailing edge	t_{17}	12	–	ns	–
MD-bus hold time from ACEN# trailing edge	t_{19}	7.5	–	ns	–
MD-bus valid to MP valid during DMA memory write cycle	t_{20}	14	24	ns	–
MD-bus high byte valid to MD low byte valid during DMA high memory read cycle	t_{21}	10	19	ns	–
Action code valid to MD high byte valid during DMA high memory write cycle	t_{22}	9	18	ns	–
Action code valid to MP valid during DMA high memory write cycle	t_{23}	17	28	ns	–

Timing Diagrams

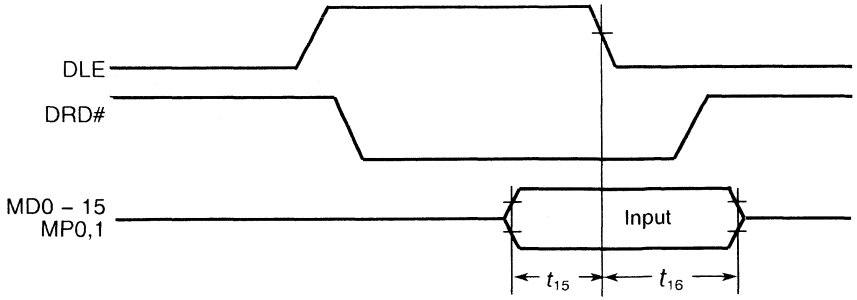
CPU Read Timing



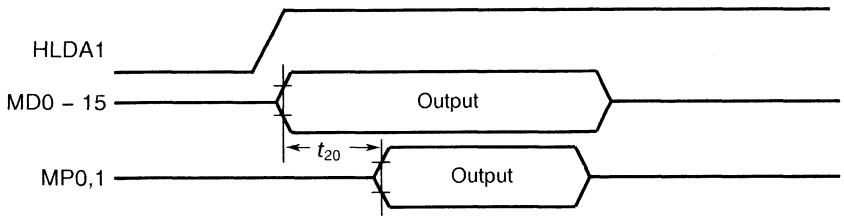
CPU Write Timing



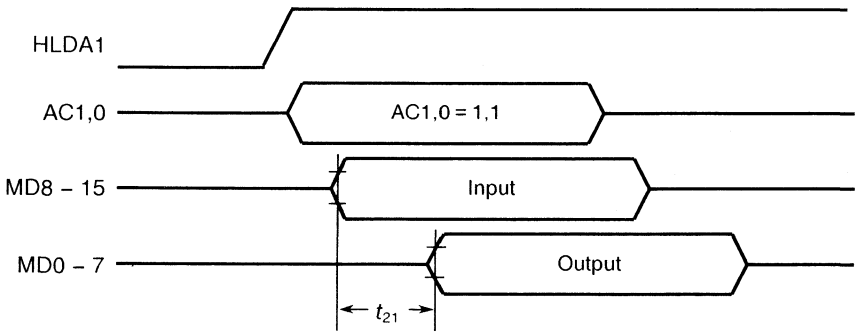
Data Latch Timing (CPU Read)



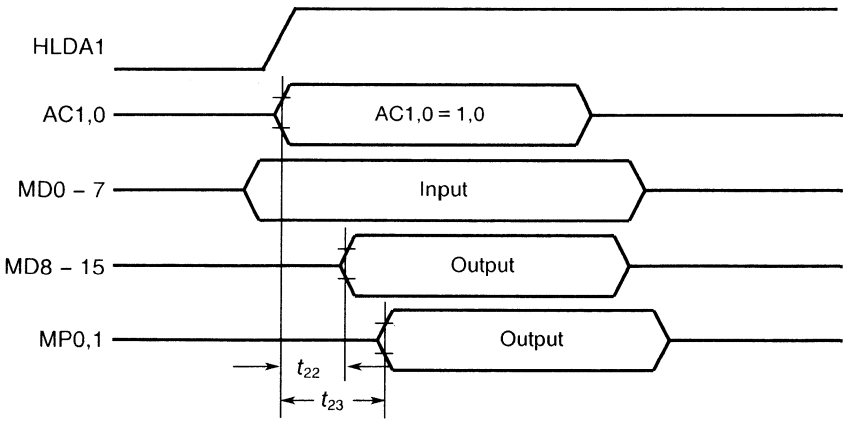
DMA Timing (HLDA1 = 1)
Memory Write Cycle



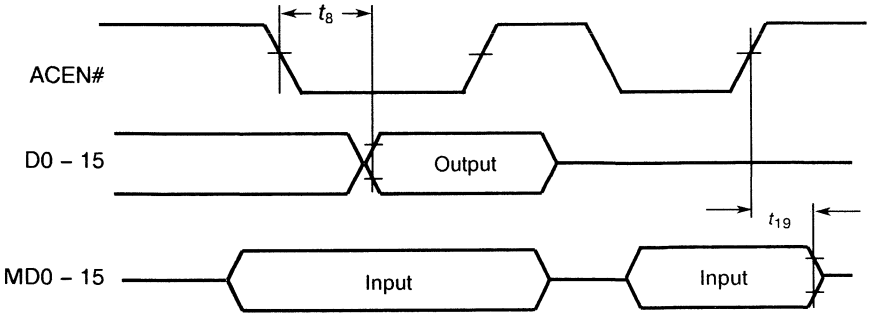
DMA Timing (HLDA1 = 1)
Memory Read High Byte / I/O Write Low Byte



DMA Timing (HLDA1 = 1)
I/O Read Low Byte / Memory Write High Byte

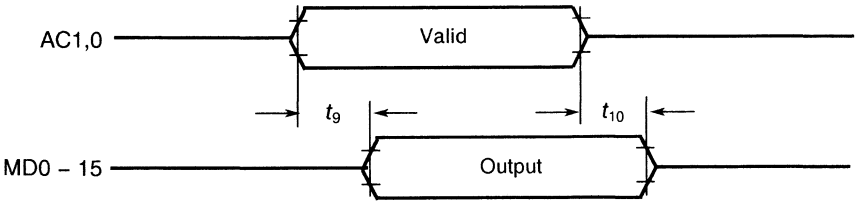


ACEN# Timing



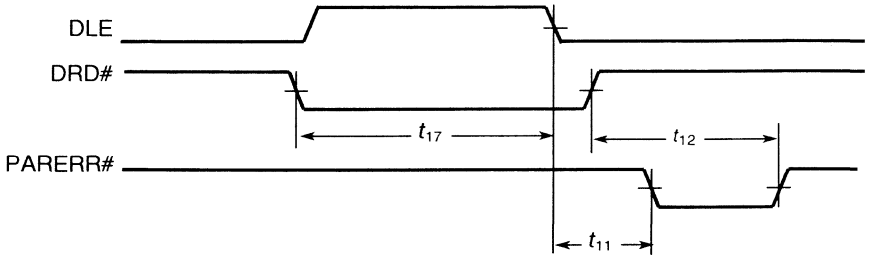
DRD# = DLE = 0

Action Code Timing

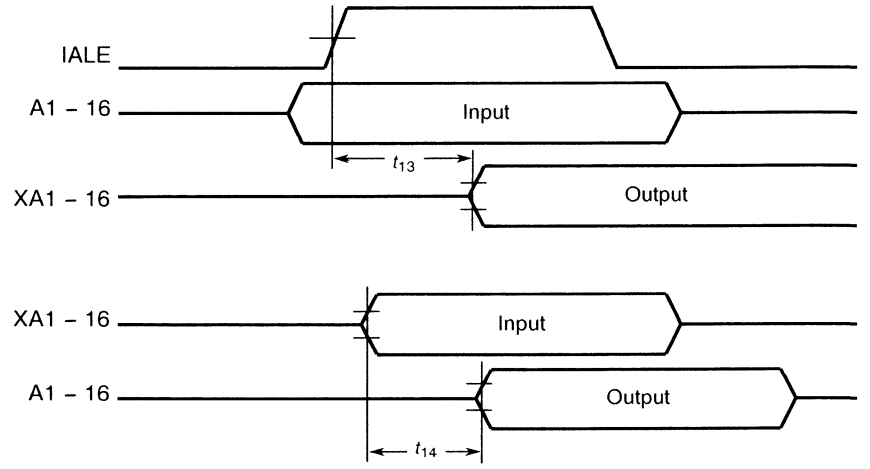


ACEN# = 0

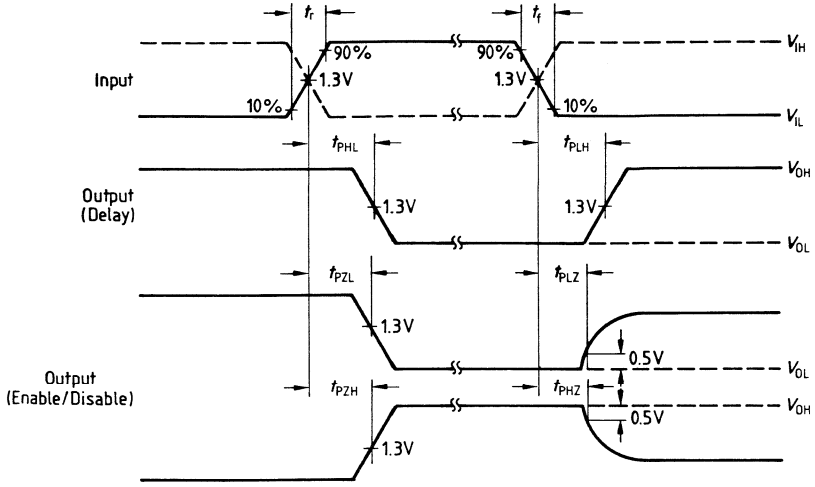
PARERR# Timing



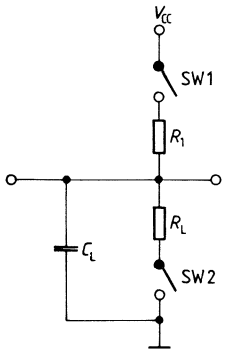
Adress Latch Timing



Load Circuit and AC Characteristics Measurement Waveform



V_{IH} = 3V, V_{IL} = 0V, $t_r \leq 10$ns, $t_f \geq 5$ns



Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L (pF)	R_1 (kΩ)	R_L (kΩ)	SW_1	SW_2
Propagation Delay Time	Totem Pole						
	Tristate	t_{PLH}	50	–	1.0	OFF	ON
	Bidirectional	t_{PHL}	50	–	1.0	OFF	ON
Propagation Delay Time	Open Drain or Open Collector	t_{PLH}	50	0.5	–	ON	OFF
		t_{PHL}	50	0.5	–	ON	OFF
Disable Time	Tristate	t_{PLZ}	5	0.5	1.0	ON	
	Bidirectional	t_{PHZ}	5	0.5	1.0	OFF	ON
Enable Time	Tristate	t_{PZL}	50	0.5	1.0	ON	ON
	Bidirectional	t_{PZH}	50	0.5	1.0	OFF	ON

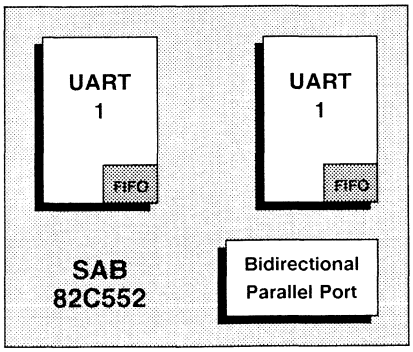
SIEMENS

SAB 82C552/SAB 82C551
Advanced Peripheral Interface Controller with FIFOs

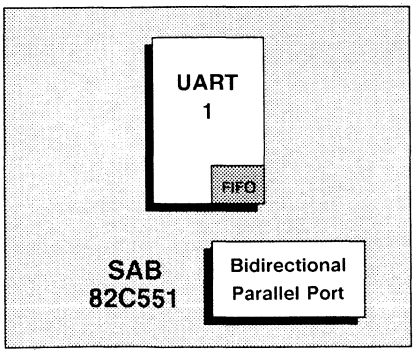
Advance Information

- SAB 82C552: Dual channel asynchronous serial controller with FIFOs
- SAB 82C551: One channel asynchronous serial controller with FIFO
- Implementation of the standard PC-XT™/AT™/PS/2™ application
- SAB 16C550A compatible serial controller
- 8-bit bi-directional parallel port
- Supports fully Centronics printer interface with bi-directional function
- PS/2 register compatible mode for bi-directional parallel port
- Fully programmable serial interface characteristics for each serial channel
  - 5/6/7/8-bit character length
  - Parity generation and detection
  - Error reporting capabilities
  - Common external clock input for the baud rate generators
  - Baud rate up to 512 Kbaud
- Mode selection by pin strapping
- I_{OL}/I_{OH} for printer data pins: 24 mA / – 6 mA
- CMOS implementation for high speed and low power requirements
- 68-pin plastic leaded chip carrier package (PL-CC-68)

SAB 82C552/82C551 Functional Blocks



SSB01400



SSB01401

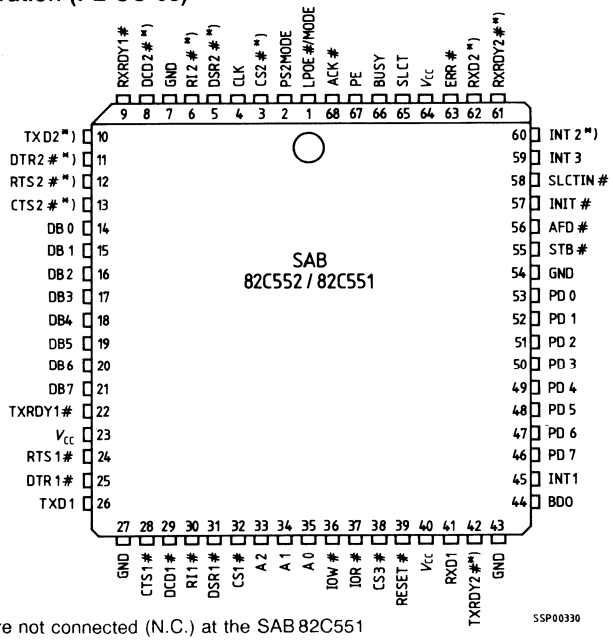
Ordering Information

Type	Ordering code	Package	Description
SAB 82C552-N	Q67120-P322	PL-CC-68 (SMD)	Advanced peripheral interface controller with FIFOs (2 serial port, 1 parallel port)
SAB 82C551-N	Q67120-P321	PL-CC-68 (SMD)	Advanced peripheral interface controller with FIFOs (1 serial port, 1 parallel port)

The SAB 82C552/82C551 are advanced serial/parallel interface controllers for standard and IBM PC-XT™/PC-AT™/PS/2™ compatible interface applications. Their serial channels provide the functionality of the SAB 16C550A universal asynchronous receiver/transmitter. Only one serial channel is available in the SAB 82C551. The parallel port fully supports the standard Centronics printer interface and provides the bi-directional feature of the PS/2 parallel port implementation.

The SAB 82C552/82C551 are fabricated in Siemens ACMOS technology and are available in the 68-pin plastic-leaded-chip-carrier (PL-CC-68) package.

Figure 1
Pin Configuration (PL-CC-68)



*) These pins are not connected (N.C.) at the SAB 82C551

Pin Definitions and Functions

Symbol	Pin Number	Input (I) Output (O)	Function
Bus Interface			
CLK	4	I	**Serial Clock:** External clock input to the baud rate generator(s) of the serial channel(s).
DB0–DB7	14-21	I/O	**Data Bus 0–7:** The data bus provides 8 bi-directional IO-lines for the transfer of data, status and control information between the SAB 82C552/82C551 and the CPU. These lines are inputs except during read operations. DB0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0-A2	35-33	I	**Address lines 0–2:** The address lines are used together with the chip select inputs to select the internal registers of the SAB 82C552/82C551.
IOW#	36	I	**IO Write Strobe#:** This is an active low input which causes the data at the data bus to be written into the selected registers of the SAB 82C552/82C551. The destination of the data depends on the state of CS1#, CS2#, CS3# and A0–A2.
IOR#	37	I	**IO Read Strobe#:** This is an active low input which causes the selected IO-device to output data to the data bus DB0-DB7. The source of the data depends on the state of CS1#, CS2#, CS3# and A0-A2.
RESET#	39	I	**RESET#:** With RESET# = low the two serial ports and the parallel port are put into an initial state.
BDO	44	O	**Bus Buffer Output:** This line goes high whenever either serial channel registers or the parallel port registers are read. This output can be used to control system bus drivers.
V_{CC}	23,40, 64	–	**Power Supply (+5 V)**
GND	7,27,43, 54	–	**Ground (0 V)**

Pin Definitions and Functions (cont'd)

Symbol [1]	Pin Number	Input (I) Output (O)	Function
Serial Interface			
RTS1# RTS2#	24 12	O	**Request To Send#:** When active (low), the UART indicates that data is ready to be transmitted. The RTS# pins are set low by writing a 1 to the appropriate bits of the modem control registers.
DTR1# DTR2#	25 11	O	**Data Terminal Ready#:** When active (low), the UART indicates that it is ready to receive data. The DTR# pins are set low by writing a 1 to the appropriate bits of the modem control registers.
TXD1 TXD2	26 10	O	**Serial Data Outputs:** These lines are the serial data outputs from the UARTs transmitter circuitry.
CTS1# CTS2#	28 13	I	**Clear To Send#:** The states of these pins are reflected in bits of the modem status registers. When CTS = low, data can be transmitted at the TXD lines.
DCD1# DCD2#	29 8	I	**Data Carrier Detect#:** The states of these pins are reflected in bits of the modem control registers. DCD# = low indicates that the data carrier has been detected by the modem.
RI1# RI2#	30 6	I	**Ring Indicator#:** The states of these pins are reflected in bits of the modem control registers. RI# = low indicates that a telephone ringing signal has been received by the modem.
DSR1# DSR2#	31 5	I	**Data Set Ready#:** The states of these pins are reflected in bits of the modem control registers. When DSR# = low, a modem is indicating that it is ready to exchange data with the associated UART.
CS1# CS2#	32 3	I	**Serial Channel Chip Select#:** CS1# and CS2# are the enable lines for the read and write control signals of the SAB 82C552/82C551 serial channels. Only one of the 3 chip select inputs may be active at a time!

1) All signals with extension "2" are not available at the SAB 82C551. The corresponding pins are not connected (N.C.) at the SAB 82C551.

Pin Definitions and Functions (cont'd)

Symbol [1]	Pin Number	Input (I) Output (O)	Function
Serial Interface (cont'd)			
RXD1 RXD2	41 62	I	**Serial Data Input:** These lines are the serial data inputs to the SAB 82C552/82C551 serial channels receiver circuitry.
INT1 INT2	45 60	O	**Serial Channel Interrupts:** These tristate outputs are enabled by the modem control register bits 3. An occurring interrupt condition of the serial channels will activate (set high) these interrupt lines. The interrupts are reset (low) upon an appropriate service.
TXRDY1# TXRDY2#	22 42	O	**Transmitter Ready#:** The transmitter ready output is used to signal DMA transfer to the CPU from the associated UART. Two modes of operation are available when using the FIFO mode and, one (Mode 0) when using the character mode. **TXRDY Mode 0** In character mode (FEWO = 0) or in the FIFO mode (FEWO = 1, DMS = 0), and when there are no characters in the XMIT FIFO or XMIT holding register, the TXRDY# pin will be low active. Once it is activated the TXRDY# pin will go inactive after the first character is loaded into the XMIT FIFO or holding register. **TXRDY Mode 1** In the FIFO mode (FEWO = 1), when DMS = 1 and there is at least one unfilled position in the XMIT FIFO, TXRDY# will go low active. This pin will become inactive when the XMIT FIFO is completely full.

1) All signals with extension "2" are not available at the SAB 82C551. The corresponding pins are not connected (N.C.) at the SAB 82C551.

Pin Definitions and Functions (cont'd)

Symbol [1]	Pin Number	Input (I) Output (O)	Function
Serial Interface (cont'd)			
RXRDY1# RXRDY2#	9 61	O	**Receiver Ready#:** The receiver ready output is used to signal DMA transfer to the CPU from the associated UART. Two modes of operation are available when using FIFO mode, and one (Mode 0) when using character mode. **RXRDY Mode 0** When in character mode (FEWO = 0) or in the FIFO mode (FEWO = 1, DMS = 0), and when there is at least 1 character in the RCVR FIFO or RCVR holding register, the RXRDY# pin will be low active. Once it is activated the RXRDY# pin will go inactive when there are no more characters in the FIFO or holding register. **RXRDY Mode 1** In the FIFO Mode (FEWO = 1) when the DMS = 1 and the trigger level or the time out has been reached, the RXRDY# pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO or holding register.
Parallel Interface			
LPOE# /MODE	1	I	**Printer Output Enable#/Mode Select:** In normal mode (PS2MODE = low) this input signal (low) enables the PD0–PD7 outputs. A high puts the PD0–PD7 lines in the high impedance state allowing them to be used as inputs. With PS2MODE = high, this input also selects between the uni- and bi-directional printer port operation.
PS2MODE	2	I	**Enable Printer PS/2 Mode:** With high at this input, the PS/2 mode of the printer interface is selected. A low level selects normal Centronics compatible mode operation of the parallel interface.

1) All signals with extension "2" are not available at the SAB 82C551. The corresponding pins are not connected (N.C.) at the SAB 82C551.

Pin Definitions and Functions (cont'd)

Symbol [1]	Pin Number	Input (I) Output (O)	Function
Parallel Interface (cont'd)			
CS3#	38	I	**Parallel Port Chip Select#**: CS3# = low enables the read and write control lines of the SAB 82C552/ 82C551 parallel port section. Only one of the 3 chips select inputs may be active at a time!
PD0–PD7	53–46	I/O	**Parallel Data Bits (0–7)**: These lines provide the byte-wide input or output port of the SAB 82C552/ 82C551.
STB#	55	O	**Line Printer Strobe#**: When low, this line provides the line printer with a signal to latch data which is currently available at the parallel port.
AFD#	56	O	**Line Printer Autofeed#**: With AFD# = low the printer does a continuous form feed of the paper.
INIT#	57	O	**Line Printer Initialize**: This signal (low) causes the printer to start its initialization routine.
SLCTIN#	58	O	**Line Printer Select#**: When active (low), this line selects the line printer.
INT3	59	O	**Interrupt Printer Port**: This interrupt output is activated (high) by a low ACK# signal. The function of INT3 is controlled by bit 4 of the parallel port control register.
ERR#	63	I	**Line Printer Error#**: If this input goes low, the line printer reports an error condition.
SLCT	65	I	**Line Printer Select**: This is an input line from the line printer that goes high when the printer has been selected.
BUSY	66	I	**Line Printer Busy**: This is an input line from the line printer that goes high when the printer has a local operation in progress.

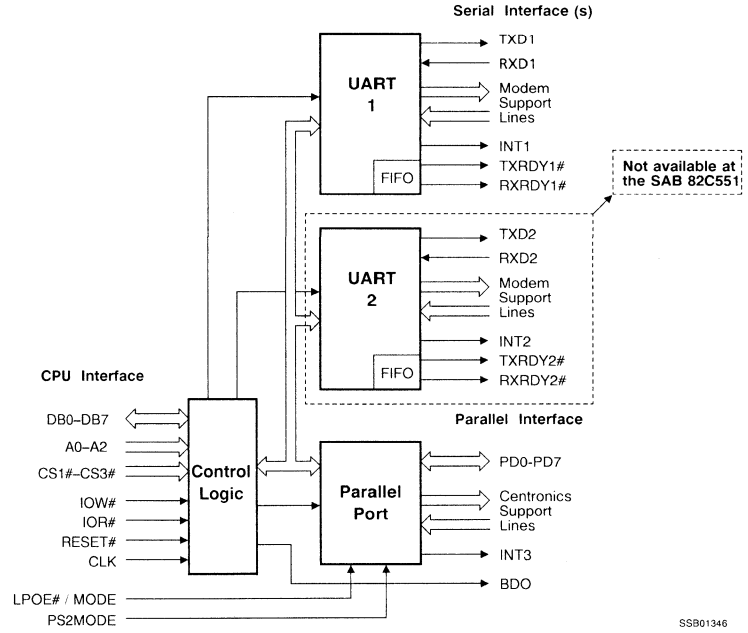
1) All signals with extension "2" are not available at the SAB 82C551. The corresponding pins are not connected (N.C.) at the SAB 82C551.

Pin Definitions and Functions (cont'd)

Symbol 1)	Pin Number	Input (I) Output (O)	Function
Parallel Interface (cont'd)			
PE	67	I	**Line Printer Paper Empty:** This is an input line from the line printer that goes high when the printer runs out of paper.
ACK#	68	I	**Line Printer Acknowledge:** This input goes low if a successful data transfer to the printer has occurred.

1) All signals with extension "2" are not available at the SAB 82C551. The corresponding pins are not connected (N.C.) at the SAB 82C551.

Figure 2
Block Diagram



Serial Channel Description

The SAB 82C552 contains two serial channels. In the SAB 82C551, the second serial channel of the SAB 82C552 is not available. In the following text, no number extensions are used when referring to the signal names. In the SAB 82C552/82C551 the number extension "1" refers to serial channel 1. In the SAB 82C552 the number extension "2" refers to serial channel 2.

Serial Port Register Addressing

When CS1# is low, registers for serial channel 1 can be accessed, and when CS2# is low, registers for serial channel 2 can be accessed. No more than one chip select line should ever be low at a time (invalid condition). Address lines A0, A1 and A2 are used to select the appropriate register of the serial channels (Table 1). The Divisor Latch Access Bit (DLAB) in table 1 is the MSB of the Line Control Register. DLAB must be set by software to access the baud rate generator divisor latches.

Table 1
Serial Channel Register Addressing

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer Register (RBR, read) Transmitter Holding Register (THR)
0	0	0	1	Interrupt Enable Register (IER)
X	0	1	0	Interrupt Identification Register (IIR, read only)
X	0	1	0	FIFO Control Register (FCR, write only)
X	0	1	1	Line Control Register (LCR)
X	1	0	0	Modem Control Register (MCR)
X	1	0	1	Line Status Register (LSR)
X	1	1	0	Modem Status Register (MSR)
X	1	1	1	Scratch Pad Register (SCR)
1	0	0	0	Divisor Latch (DLL, least significant byte)
1	0	0	1	Divisor Latch (DLM, most significant byte)

Register Description

Three types of internal registers are used in the serial channels of the SAB 82C552/82C551: control, status and data registers. The control registers are two divisor latches for the baud rate generator, the Line Control Register (LCR), the Interrupt Enable Register (IER), the FIFO Control Register (FCR), and the Modem Control Register (MCR). Two status registers are available: Line Status Register (LSR) and Modem Status Register (MSR). The data registers are the Receiver Buffer Register (RBR) for read operations, and the Transmitter Holding Register (THR) for write operations. Table 2 shows the contents of the SAB 82C250/82C251 serial channel registers in detail.

Receiver/Transmitter Buffer Register

The Receiver Buffer Register and the Transmitter Buffer Register are data registers, which hold between five and eight bits of data. If less than eight data bits are transmitted, then the data will be right justified to the LSB. Bit 0 of a data byte is always the first serial data bit received and transmitted.

Table 2
Summary of Registers

Bit No.	Register Address					
	0 (DLAB = 0)	0 (DLAB = 0)	1 (DLAB = 0)	2	2	3
	Receiver buffer register (read only)	Transmitter holding register (write only)	Interrupt enable register	Interrupt ident. register (read only)	FIFO control register (write only)	Line control register
	RBR	THR	IER	IIR	FCR	LCR
0	Data bit 0 [1]	Data bit 0 [1]	Enable received data available interrupt (ERBFI)	"0" if interrupt is pending (IP)	FIFO enable (FEWO)	Word length select bit 0 (WLS0)
1	Data bit 1	Data bit 1	Enable transmitter holding register empty (ETBEI)	Interrupt ID bit 0 (IIDB0)	Receiver FIFO reset (RFR)	Word length select bit 1 (WLS1)
2	Data bit 2	Data bit 2	Enable receiver line status interrupt (ERLSI)	Interrupt ID bit 1 (IIDB1)	Transmitter FIFO reset (TFR)	Number of stop bits (STB)
3	Data bit 3	Data bit 3	Enable modem status interrupt (EDSSI)	Interrupt ID bit 2 (IIDB 2)	DMA mode select (DMS)	Parity enable (PEN)
4	Data bit 4	Data bit 4	0	0	Reserved	Even parity select (EPS)
5	Data bit 5	Data bit 5	0	0	Reserved	Stick parity (STP)
6	Data bit 6	Data bit 6	0	FIFOs enabled (FE) [2]	RCVR FIFO trigger level (LSB)	Set break (SBR)
7	Data bit 7	Data bit 7	0	FIFOs enabled (FE) [2]	RCVR FIFO trigger level (MSB)	Divisor latch access bit (DLAB)

Table 2
Summary of Registers (cont'd)

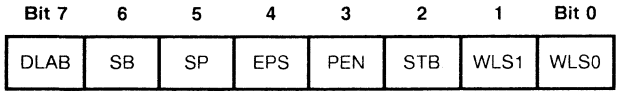
Bit No.	Register Address					
	4	5	6	7	0 (DLAB = 1)	1 (DLAB = 1)
	Modem control register	**Line status register**	**Modem status register**	**Scratch register**	**Divisor latch (LS)**	**Divisor latch (MS)**
	MCR	**LSR**	**MSR**	**SCR**	**DLL**	**DLM**
0	Data terminal ready (DTR)	Data ready (DR)	Delta clear to send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to send (RTS)	Overrun error (OE)	Delta data set ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not connected	Parity error (PE)	Trailing edge ring indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt output enable (IOE)	Framing error (FE)	Delta data carrier detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Loop (LOOP)	Break interrupt (BI)	Clear to send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter holding register (THRE)	Data set ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter empty (TEMT)	Ring indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO (EIRF) [2]	Data carrier detect (DCD)	Bit 7	Bit 7	Bit 15

1) Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
2) These bits are always 0 im character mode.

Line Control Register (LCR)

The format of the asynchronous data communication exchange and the access to the divisor latch is controlled via the line control register.

Figure 3
Line Control Register



Bit 0 and 1: (WLS0, WLS1) These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: (STB) This bit specifies the number of stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one stop bit is generated or checked in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop-bit only, regardless of the number of stop bits selected.

Bit 3: (PEN) This bit is the parity enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).

Bit 4: (EPS) This bit is the even parity select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's is transmitted or checked.

Bit 5: (STP) This bit is the stick parity bit. When bits 3, 4 and 5 are logic 1 the parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is logic 0 then the parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 stick parity is disabled.

Bit 6: (SBR) This bit is the break control bit. It causes a break condition to be transmitted by the UART. When it is set to a logic 1, the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by clearing bit 6 to a logic 0. The break control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. *Load an all O's pad character in response to THRE.*
2. *Set break after the next THRE.*
3. *Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission is to be restored. During the break, the transmitter can be used as a character timer to accurately establish the break duration.*

Bit 7: (DLAB) This bit is the divisor latch access bit. It must be set high (logic 1) to access the divisor latches of the baud generator during a read or write operation. It must be set low (logic 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

Programmable Baud Rate Generator

The serial channels of the SAB 82C552/82C551 contain a programmable baud rate generator, which is capable of taking any clock input from DC to 8.0 MHz and dividing it by any divisor from 1 to $2^{16} - 1$. The output frequency of the baud rate generator is 16× the baud rate.

$$\text{Divisor} = \frac{\text{Input frequency at CLK}}{\text{Desired baud rate} \times 16}$$

Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud rate generator.
By loading one of the divisor latches, the 16-bit baud rate counter is immediately loaded.
Tables 3, 4 and 5 provide decimal divisors to use with CLK clock frequencies of 1.8432 MHz, 3.072 MHz and 8 MHz, respectively. The maximum operating frequency of the baud rate generator is 8.0 MHz. In this case, the data rate can be 512 Kbaud maximum.

Table 3
Baud Rates Using 1.8432 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 × clock	Percent error difference between desired and actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Table 4
Baud Rates Using 3.072 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 × clock	Percent error difference between desired and actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–
56000	3	14.285

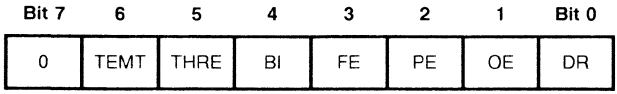
Table 5
Baud Rates Using 8 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 × clock	Percent error difference between desired and actual
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

Line Status Register (LSR)

This 8-bit register provides the CPU with status information concerning the data transfer.

Figure 4
Line Status Register



Bit 0: (DR) This bit is the receiver data ready indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the receiver buffer register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the receiver buffer register or the FIFO.

Bit 1: (OE) This bit is the overrun error indicator. Bit 1 indicates that data in the receiver buffer register was not read by the CPU before the next character was transferred into the receiver buffer register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition, and reset whenever the CPU reads the contents of the line status register. If in the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

Bit 2: (PE) This bit is the parity error indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the line status register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: (FE) This bit is the framing error indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic 1 whenever the stop bit following the last data bit or parity bit is detected as a logic 0 bit (spacing level). The FE indicator is reset whenever the CPU reads the contents of the line status register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".

Bit 4: (BI)
This bit is the break interrupt indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits).The BI indicator is reset whenever the CPU reads the contents of the line status register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to.This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: (THRE)
This bit is the transmitter holding register empty indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the transmit holding register empty interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: (TEMT)
This bit is the transmitter empty indicator. Bit 6 is set to a logic 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: (EIRF)
In the character mode this is a 0. In the FIFO mode EIRF is set when there is at least one parity error, framing error or break indication in the FIFO. EIRF is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

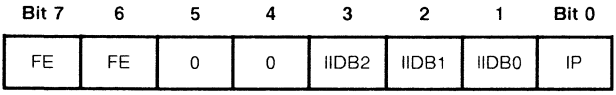
Note: The line status register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

Interrupt Identification Register

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt identification register. The four levels of interrupt conditions in order of priority are receiver line status, received data ready, transmitter holding register empty, and modem status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete.

Figure 5
Interrupt Identification Register



Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: (IIDB0; IIDB1) These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 6.

Bits 3: (IIDB2) In the character mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5: These two bits of the IIR are always logic 0.

Bits 6 and 7: (FE) These two bits are set when FEWO = 1.

Table 6
Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	–	None	None	–
0	1	1	0	Highest	Receiver line status	Overrun error or parity error or framing error or break interrupt	Reading the line status register
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	Reading the receiver buffer register or the FIFO drops below the trigger level
1	1	0	0	Second	Character timeout indication	No characters have been removed from or input to the RCVR FIFO during the last 4 char. times and there is at least 1 char. in it during this time	Reading the receiver buffer register
0	0	1	0	Third	Transmitter holding register empty	Transmitter holding register empty	Reading the IIR register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	Fourth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect	Reading the modem status register

Interrupt Enable Register (IER)

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (INT1/INT2) output signals. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt enable register (IER). Similarly, setting bits of this register to a logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INT1/INT2 output signals. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. Figure 6 shows the contents of the IER.

Figure 6
Interrupt Enable Register

Bit 7	6	5	4	3	2	1	Bit 0
0	0	0	0	EDSSI	ERLSI	ETBEI	ERBFI

Bit 0: (ERBFI) This bit enables the received data available interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1: (ETBEI) This bit enables the transmitter holding register empty interrupt when set to logic 1.

Bit 2: (ERLSI) This bit enables the receiver status interrupt when set to logic 1.

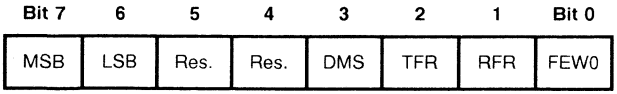
Bit 3: (EDSSI) This bit enables the modem status interrupt when set to logic 1.

Bit 4 through 7: These four bits are always logic 0.

FIFO Control Register

This is a write only register at the same address location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Figure 7
FIFO Control Register



Bit 0: (FEWO) Writing a 1 to FEWO enables both the XMIT and RCVR FIFOs. Resetting FEWO will clear all bytes in both FIFOs. When changing from FIFO mode to character mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to, or they will not be programmed.

Bit 1: (RFR) Writing a 1 to RFR clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: (TFR) Writing a 1 to TFR clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: (DMS) Setting DMS to a 1 will cause the RXRDY and TXRD pins to change from mode 0 to mode 1 if FEWO = 1 (see description of RXRDY and TXRDY pins).

Bit 4 and 5: These bits are reserved for future use.

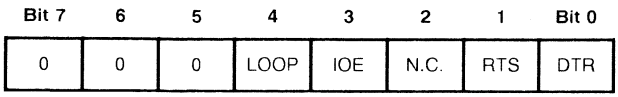
Bit 6 and 7: FCR6 and FCR 7 are used to set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (Bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Modem Control Register (MCR)

This register controls the interface to the Modem or data set (or a peripheral device emulating a Modem).

Figure 8
Modem Control Register



Bit 0: (DTR) This bit controls the data terminal ready output. When bit 0 is set to a logic 1, the DTR# output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR# output is forced to a logic 1.

Note: The DTR# output of the UART may be applied to an EIA inverting line driver (such as the 1488) to obtain the proper polarity input at the succeeding modem or data set.

Bit 1: (RTS) This bit controls the request to send output. Bit 1 affects the RTS# output in a manner identical to that described above for bit 0.

Bit 2: This bit is not connected. In loop mode this bit is connected to the modem status register bit 6.

Bit 3: (IOE) This bit enables the INT1/INT2 output pin. When this bit is a logic 0 the INT output pin is tri-stated. In loop mode this bit is connected to bit 7 of the modem status register.

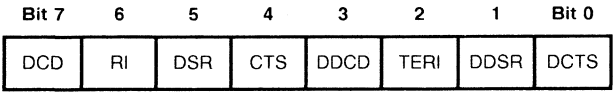
Bit 4: (LOOP) This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter serial output (SOUT) is set to the marking (logic 1) state; the receiver serial input (SIN) is disconnected; the output of the transmitter shift register is "looped back" into the receiver shift register input; the four modem control inputs (CTS#, DSR#, RI#, and DCD#) are disconnected; and the outputs 0–3 of the modem control register are internally connected to the four modem control inputs. The modem control output pins DTR# and RTS# are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupt's sources are now the lower four bits of the modem control register instead of the four modem control inputs. The interrupts are still controlled by the interrupt enable register.

Bits 5 through 7: These bits are permanently set to logic 0.

Modem Status Register

This register provides the current state of the control lines from the modem (or peripheral device) to the CPU. In addition to this current-state information, four bits of the modem status register provide change information. These bits are set to a logic 1 whenever a control input from the modem changes state. They are reset to logic 0 whenever the CPU reads the modem status register.

Figure 9
Modem Status Register



Bit 0: (DCTS) This bit is the delta clear to send indicator. Bit 0 indicates that the CTS# input to the chip has changed state since the last time it was read by the CPU.

Bit 1: (DDSR) This bit is the delta data set ready indicator. Bit 1 indicates that the DSR# input to the chip has changed state since the last time it was read by the CPU.

Bit 2: (TERI) This bit is the trailing edge of ring indicator detector. Bit 2 indicates that the RI# input to the chip has changed from a low to a high state.

Bit 3: (DDCD) This bit is the delta data carrier detect indicator. Bit 3 indicates that the DCD# input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a modem status interrupt is generated.

Bit 4: (CTS) This bit is the complement of the clear to send input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: (DSR) This bit is the complement of the data set ready input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: (RI) This bit is the complement of the ring indicator input. If bit 4 of the MCR is set to a 1, this bit is equivalent to bit 2 in the MCR.

Bit 7: (DCD) This bit is the complement of the data carrier detect input. If bit 4 of the MCR is set to a 1, this bit is equivalent to IOE in the MCR.

Scratchpad Register

This 8-bit read/write register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Reset Operation

A low level at the RESET# input pin causes the UART to reset to the condition listed in table 7.

Table 7
Register Reset Functions

Register/signal	Reset Control	Reset state
Receiver Buffer Register	First byte received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All bits low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high, bits 1 and 2 low, bits 3–7 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	All bits low, except bits 5 and 6 are high
Modem Status Register	Master Reset	Bits 0-3 low, bits 4–7 input signal
FIFO Control Register	Master Reset	All bits low
Divisor Latch (LSB)	Writing into the latch	Data
Divisor Latch (MSB)	Writing into the latch	Data
SOUT	Master Reset	High
BDO	Master Reset	Low
Interrupt (RCVR ERRS)	Master Reset/Read LSR	Low
Interrupt (RCVR Data Ready)	Master Reset/Read RBR	Low
Interrupt (THRE)	Master Reset/Read IIR/ Write THR	Low
Interrupt (Modem status changes)	Master Reset/Read MSR	Low
RTS#	Master Reset	High
DTR#	Master Reset	High
Interrupt output line	Master Reset	tristated
RCVR FIFO	MR/RFR + FEWO/ΔFEWO	All bits low
XMIT FIFO	MR/TFR + FEWO/ΔFEWO	All bits low

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FEWO = 1, ERBFI = 1) RCVR interrupts will occur as follows:

a) The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

b) The IIR receive data available indicaton also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

c) The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.

d) The data ready bit (DR) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

a) A FIFO timeout interrupt will occur, if the following conditions exist:
   - at least one character is in the FIFO
   - the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
   - the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

   This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with a 12-bit character.

b) Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).

c) When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

d) When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FEWO = 1, ETBEI = 1), XMIT interrupts will occur as follows:

a) The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

b) The transmitter FIFO empty indication will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE = 1, and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FEWO will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation

With FEWO = 1 resetting ERBFI, ETBEI, ERLSI, EDSSI or all to zero puts the UART in the FIFO polled mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

- DR will be set as long as there is one byte in the RCVR FIFO.
- LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since ERLSI = 0.
- THRE will indicate when the XMIT FIFO is empty.
- TEMT will indicate that both the XMIT FIFO and shift register are empty.
- EIRF will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO polled mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Parallel Port Description

Register Selection

The internal data, status and control registers of the parallel port are selected by two address lines, the chip select line CS3# and the read/write control inputs.

Table 8
Parallel Port Register Addresses

CS3#	A1	A0	IOR#	IOW#	Operation
1	X	X	X	X	No Operation
0	0	0	1	0	Write Data Register
0	0	0	0	1	Read Data Register
0	0	1	0	1	Read Status Register
0	1	0	1	0	Write Control Register
0	1	0	0	1	Read Control Register

While CS3# is activated, CS1# and CS2# must be inactive. Other combinations of A0, A1, IOR#, and IOW# together with CS3# = 0 as shown in table 8 are illegal combinations.

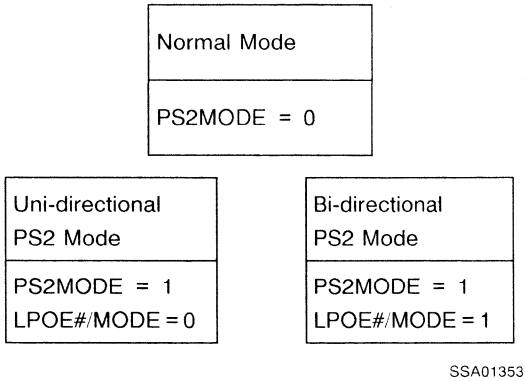
Table 9
Parallel Port Register Definition

	Register Address		
	0	1	2
Bit No.	Data Register	Status Register	Control Register
0	Data Bit 0	1	STB
1	Data Bit 1	1	AFD
2	Data Bit 2	PS2MODE = 0:1 PS2MODE = 1:IRQSTAT	INIT
3	Data Bit 3	ERROR	SLCTIN
4	Data Bit 4	SLCT	IRQEN
5	Data Bit 5	PE	PS2MODE = 0:1 PS2MODE = 1:DIR
6	Data Bit 6	ACK	1
7	Data Bit 7	BUSY	1

Parallel Port Mode Selection

The parallel port of the SAB 82C552/82C551 can work in two basic operating modes: the normal mode and the PS/2 mode. In PS/2 mode a uni-directional or bi-directional operation is possible. Two strapping pins are used to select the operating mode. With PS2MODE = 0 the normal mode is selected. In PS/2 mode, the LPOE#/MODE pin selects further mode operations (figure 10).

Figure 10
Parallel Port Mode Selection



In the normal mode, the SAB 82C552/82C551 parallel port operates in a XT/AT and 16C452/16C451 compatible mode. The input line LPOE#/MODE acts as an output enable input for PD0–PD7. With LPOE#/MODE = 1, PD0–PD7 may be used as an 8-bit input port.

Data Register

The data register is a read/write register for the 8-bit data of the parallel port. The data transfer to or from the PD0-PD7 pins is handled via this register. The source of data during a read operation of the data register depends on the selected mode of the parallel port. Either the data register itself or the data at the PD0–7 pins may be read back (figure 11).

The PS/2 mode is divided into an uni-directional and a bi-directional operation mode. In the uni-directional PS/2 mode output drivers are always enabled. In this mode a read access to the data register directly returns the data register content.
In the bi-directional PS/2 mode, bit 5 of the control register (DIR) controls the direction of the data paths. If DIR is set, data at PD0–7 can be read (output driver disabled). With DIR = 0, the data register information is available at PD0-7 (output driver enabled).

Figure 11
Parallel Port Internal Data Path

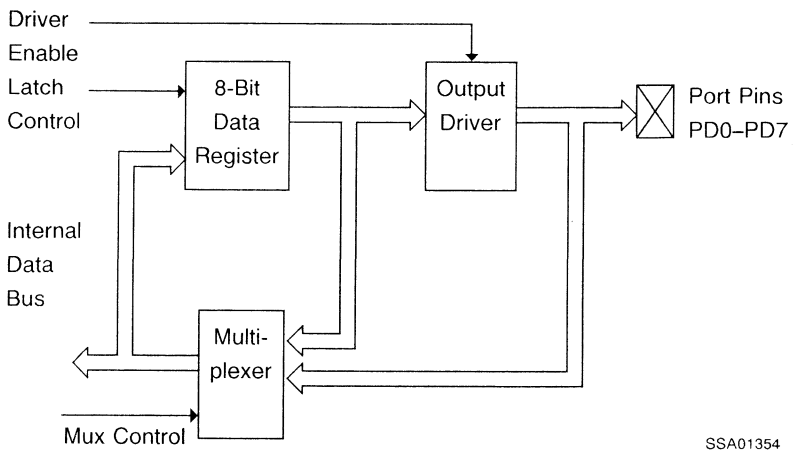


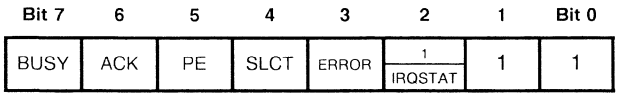
Table 10
Parallel Port Data Register Access Combinations

Mode		Pin PS2MODE	Pin LPOE#/ MODE	Bit DIR	Read Operation	Write Operation
Normal Mode		0	0	X	Read data register via the enabled output driver	Latch data in data register with output driver enabled
		0	1	X	Output driver disabled; Read data from PD0–7	Latch data in data register with output driver disabled
PS/2 Mode	Uni-directional	1	0	X	Read data of data register with output driver enabled	Latch data in data register with output driver enabled
	Bi-directional	1	1	0	Read data of data register with output driver enabled	Latch data in data register with output driver enabled
		1	1	1	Output driver disabled; Read data from PD0–7	Latch data in data register with output driver disabled

Status Register

The status register is a read-only register. A read operation of this register presents the real-time status of the parallel port interface input lines to the CPU.

Figure 12
Parallel Port Status Register



Bit 0,1: Permanently set to 1

Bit 2: (IRQSTAT) If PS2MODE = 0 this bit is permanently set to 1. If PS2MODE = 1, this bit indicates an interrupt request status. IRQSTAT is cleared with every transition of the ACK# input signal, if the interrupt requests are enabled by the IRQEN bit of the control register (IRQEN = 1). If IRQSTAT = low, a read operation of the status register sets IRQSTAT back to high level. IRQSTAT is also set high by writing the control port with IRQEN = 0 (interrupt disable).

Bit 3: (ERROR) ERROR indicates the non-inverted state of the ERR# input.

Bit 4: (SCLT) SCLT indicates the non-inverted state of the SLCT input.

Bit 5: (PE) PE indicates the non-inverted state of the PE input.

Bit 6: (ACK) ACK indicates the non-inverted sstate of the ACK# input. If the parallel port interrupt is enabled (IRQEN = 1), the ACK# input is directly connected to the INT3 output.

Bit 7: (BUSY) BUSY indicates the inverted state of the BUSY input.

Control Register

The control register of the parallel port may be read or written. A write operation to the control register latches the five (PS/2 mode : six) least significant bits of the write data.

Figure 13
Parallel Port Control Register

Bit 7	6	5	4	3	2	1	Bit 0
1	1	1 / DIR	IRQEN	SLCTIN	INIT	AFD	STB

Bit 0: (STB) STB controls or indicates the inverted state of the STB# output.

Bit 1: (AFD) AFD controls or indicates the inverted state of the AFD# output.

Bit 2: (INIT) INIT controls or indicates the non-inverted state of the INIT# output.

Bit 3: (SLCTIN) SLCTIN controls or indicates the inverted state of the SLCTIN# output.

Bit 4: (IRQEN) With IRQEN = 0 parallel port interrupt is disabled and the INT3 output is tri-stated. IRQEN = 1 enables the INT3 output and the parallel port interrupt.

Bit 5: (DIR) If PS2MODE = 0, this bit is permanently set to 1. If PS2MODE = 1, DIR controls the data transfer direction of the parallel port. Details about DIR are listed in table 10.

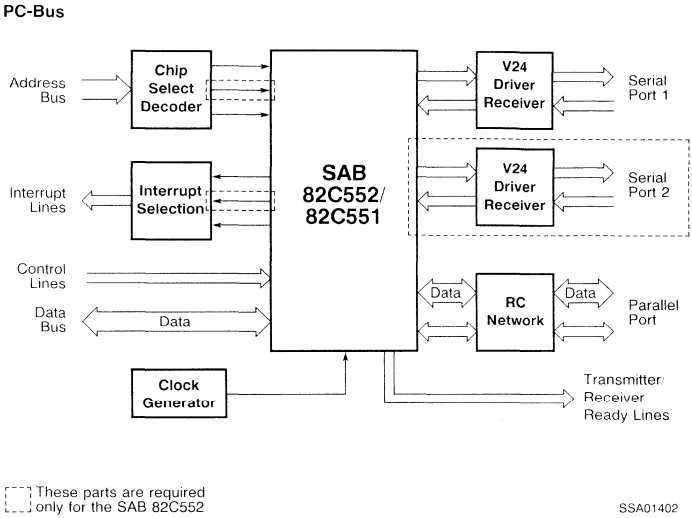
Bit 6,7: These bits are permanently set to 1.

After a reset operation (RESET# = 0) the active bits of the control register are set in the following way:

STB, AFD, SLCTIN = 0

INIT, IRQEN, DIR = 0

Figure 14
SAB 82C552/82C551 Typical Application



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 65 to + 150 °C
Supply voltage ..... – 0.5 to + 70 V
Voltage on any pin with respect to ground ..... – 0.5 to V_{CC} + 0.5 V
Power dissipation ..... 500 mW

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Clock input low voltage	V_{IL}	–0.5	+ 0.8	V	–
Clock input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Input low voltage	V_{IL}	–0.5	+ 0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.4	V	I_{OL} = 24 mA on PD0–PD7 I_{OL} = 10 mA on INIT#, AFD#, STB#, SLCTIN# I_{OL} = 4.0 mA on other outputs
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = –6 mA on PD0–PD7 I_{OH} = –0.4 mA on INIT#, AFD#, STB#, SLCTIN# I_{OH} = –2.5 mA on other outputs
Input leakage current	I_{IL}	–	± 10	µA	V_{CC} = 5.25 V; GND = 0 V; 0 V ≤ V_{IN} ≤ V_{CC} All other pins floating
Clock leakage current	I_{CL}	–	± 10	µA	V_{IN} = 0 V, 5.25 V
Tristate leakage current	I_{OZ}	–	± 20	µA	V_{CC} = 5.25 V; GND = 0 V; V_{OUT} = 0 V, 5.25 V 1. Chip selected 2. Chip and write mode selected
Power supply current	I_{CC}	–	20	mA	V_{CC} = 5.25 V; No loads on RXD0,1, DSR0,1#, DCD0,1#, CTS0,1#; RI0,1# = 2.0 V; Other inputs = 0.8 V; Baud rate = 256 K; Baud rate gen. = 8 MHz
Reset Schmitt V_{IL}	$V_{IL(RES)}$	–	0.8	V	–
Reset Schmitt V_{IH}	$V_{IH(RES)}$	2.0	–	V	–

Capacitance [1]

T_A = 25 °C; f = 1 MHz; V_{CC} = GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Clock input capacitance	C_{XIN}	–	10	pF	f_C = 1 MHz
Input capacitance	C_{IN}	–	10	pF	Unmeasured pins are returned to GND
Output capacitance	C_{OUT}	–	10	pF	Unmeasured pins are returned to GND

AC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5 %; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Bus Interface Timing					
IOR# delay from address	t_{AR}	30	–	ns	–
IOW# delay from address	t_{AW}	30	–	ns	–
IOR# delay from chip select	t_{CSR}	25	–	ns	–
IOW# delay from chip select	t_{CSW}	25	–	ns	–
Data hold time	t_{DH}	25	–	ns	–
Data setup time	t_{DS}	30	–	ns	–
BDO delay from IOR#	t_{DD}	–	30	ns	1 TTL load
IOR# to floating data delay	t_{HZ}	0	100	ns	150 pF loading [2]
Parallel port data hold time	t_{PDH}	20	–	ns	–
Parallel port data setup time	t_{PDS}	20	–	ns	–
Address hold time from IOR#	t_{RA}	20	–	ns	–
Chip select hold time from IOR#	t_{RCS}	20	–	ns	–
IOR# strobe width	t_{RD}	125	–	ns	–
Delay from IOR# to data	t_{RVD}	–	110	ns	150 pF loading [2]
Address hold time from IOW#	t_{WA}	20	–	ns	–
Chip select hold time from IOW#	t_{WCS}	20	–	ns	–
Parallel port data valid after IOW#	t_{WOL}	–	90	ns	–
IOW# strobe width	t_{WR}	100	–	ns	–
Clock cycle time	t_{XC}	125	–	ns	–
Clock high time	t_{XH}	55	–	ns	–
Clock low time	t_{XL}	55	–	ns	–
Read cycle	R_C	280	–	ns	–
Write cycle	W_C	280	–	ns	–

For notes see page 35.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Receiver/Transmitter Timing					
Delay from IOR# to reset interrupt (read RBR or read LSR)	t_{RINT}	–	175	ns	150 pF loading
Delay from stop to set interrupt	t_{SINT}	–	1	t_{XC}	150 pF loading 4)
Delay from IOW# to reset interrupt (write THR)	t_{HR}	–	175	ns	150 pF loading
Delay from IOR# to reset interrupt (write THR)	t_{IR}	–	175	ns	150 pF loading
Delay from Initial interrupt reset to transmit start	t_{IRS}	8	24	3)	–
Delay from initial write to interrupt	t_{SI}	16	24	3)	–
Delay from stop to interrupt (THRE)	t_{STI}	8	8	3)	–
Delay from start to TXRDY# active	t_{SXA}	–	8	3)	150 pF loading
Delay from write to TXRDY# inactive	t_{WXI}	–	195	ns	150 pF loading
Delay from read to RXRDY# inactive	t_{RXI}	–	290	ns	–
Modem Control Timing					
Delay from IOW# to output(write MCR)	t_{MDO}	–	200	ns	150 pF loading
Delay from IOW# to interrupt active/tri-state	t_{WI}	–	200	ns	150 pF loading
Delay to reset interrupt from MODEM input	t_{SIM}	–	200	ns	150 pF loading
Delay to reset interrupt from IOR# (read MSR)	t_{RIM}	–	200	ns	150 pF loading
Reset Timing					
Output float from reset	I_{RSF}	–	100	ns	150 pF loading 2)
Output low from reset	I_{RSL}	–	100	ns	–
Output high from reset	I_{RSH}	–	100	ns	–
Reset pulse width	t_{RW}	500	–	ns	–

For notes see page 35.

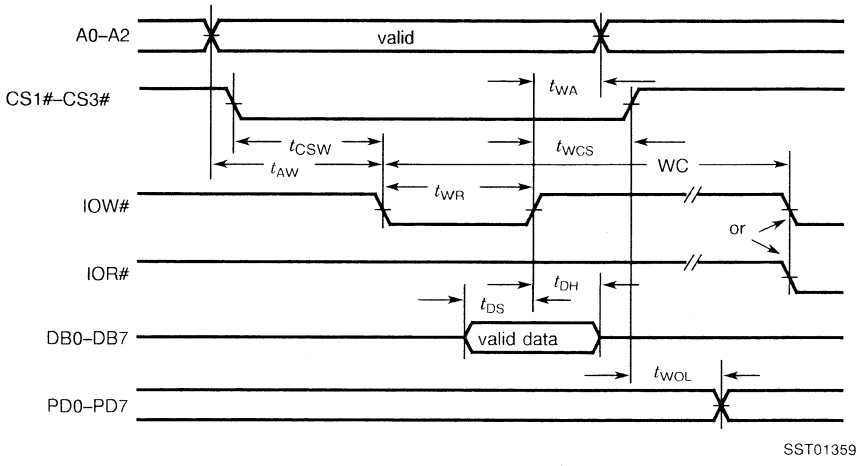
AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Parallel Port Timing					
Data to STB# setup/hold time	t_{DT}	1	–	µs	–
STB# width	t_{SB}	1	500	µs	–
BUSY# start to ACK#	t_{BSA}	–	–	µs	Printer dependent
BUSY# delay from STB#	t_{BSD}	–	–	µs	Printer dependent
BUSY# width	t_{BSY}	–	–	µs	Printer dependent
ACK# width	t_{AK}	–	–	µs	Printer dependent
ACK# delay	t_{AKD}	–	–	µs	Printer dependent
INT3 delay to ACK# transition	t_{ID}	–	50	ns	–
INT3 disable time	t_{IDI}	–	50	ns	150 pF loading 2)
INT3 enable time	t_{IEN}	–	50	ns	150 pF loading 2)

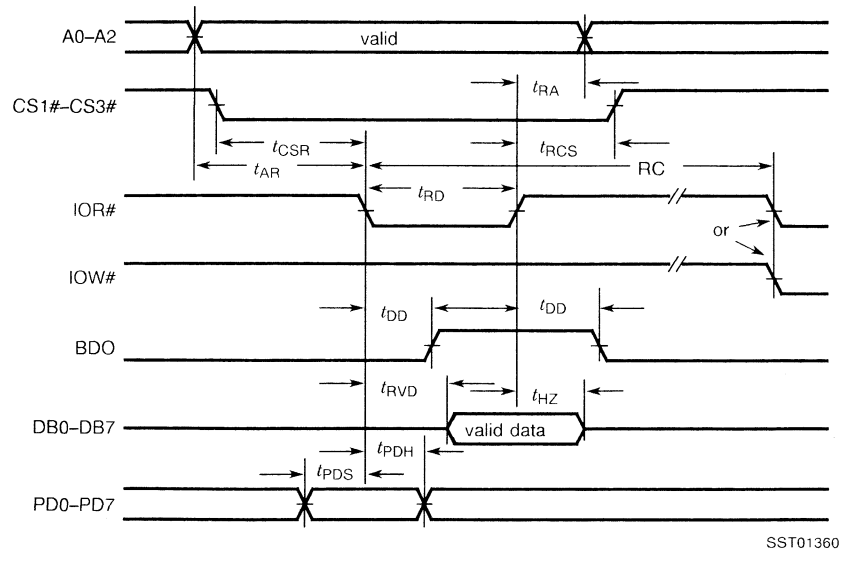
Notes for pages 32 to 35

1) These parameters are periodically sampled, not 100 % tested.
2) Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.
3) The unit is the clock frequency (baud rate) which is defined by dividing the CLK input frequency by the specified divisor in the baud generator divisor latches.
4) In the FIFO mode (FCRO = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RD RBR goes inactive. Timeout interrupt is delayed 8 RCLKs.

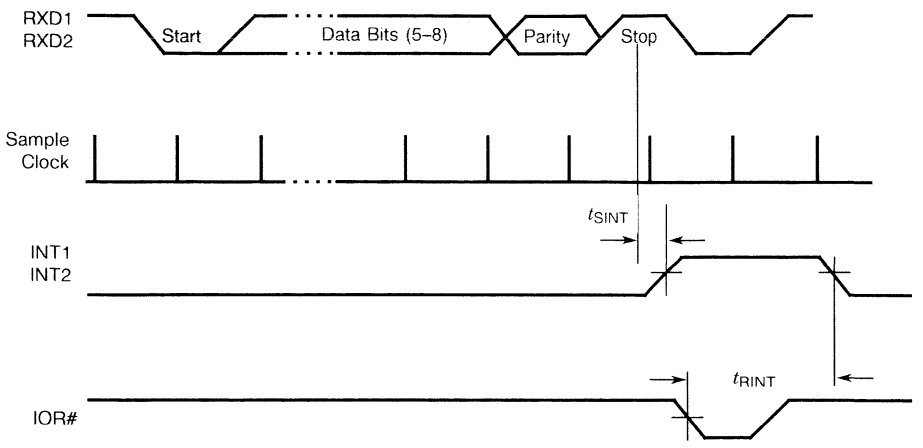
Write Cycle Timing



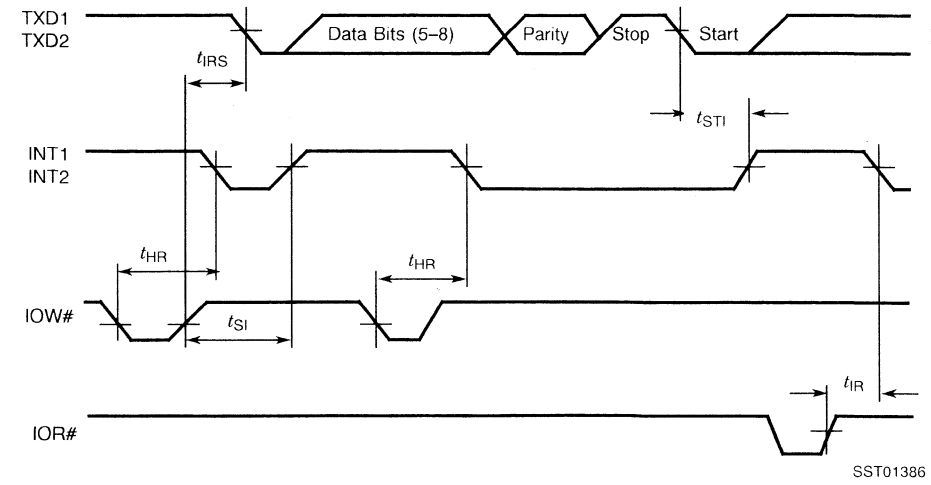
Read Cycle Timing



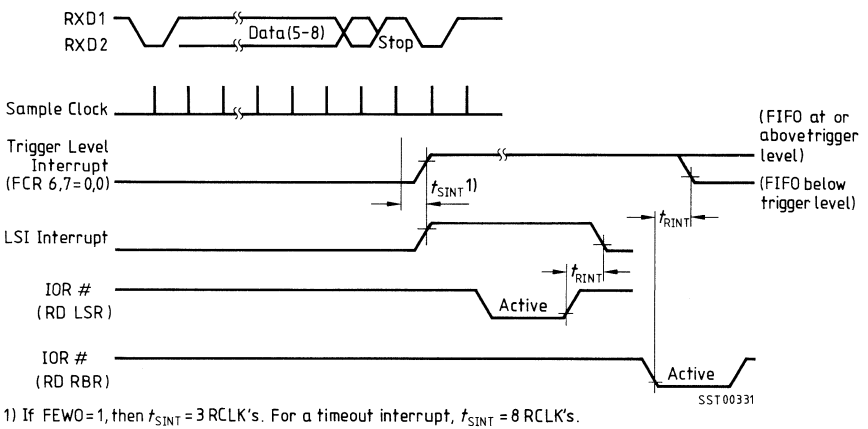
Receiver Timing
Compatible Mode



Transmitter Timing

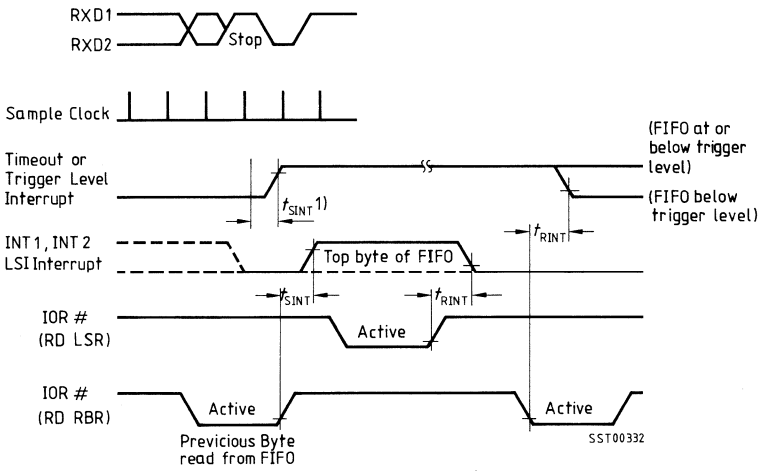


Receiver FIFO First Byte (this sets RDR)



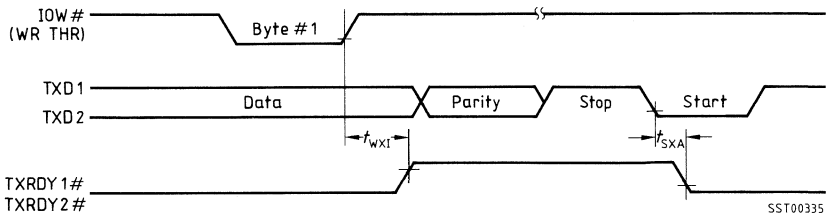
1) If FEWO=1, then t_{SINT} = 3 RCLK's. For a timeout interrupt, t_{SINT} = 8 RCLK's.

Receiver FIFO Bytes other than the First Byte (RDR is already set)

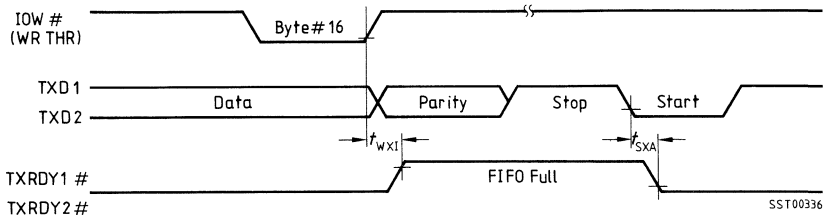


1) If FEWO = 1, then t_{SINT} = 3 RCLK's. For a timeout interrupt, t_{SINT} = 8 RCLK's.

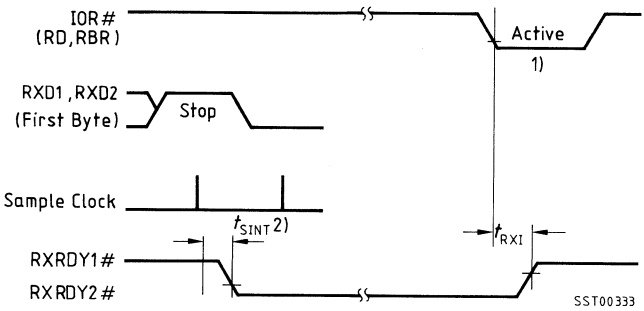
Transmitter Ready FEWO = 0 or FEWO = 1 and DMS = 0 (Mode 0)



Transmitter Ready FEWO = 1 and DMS = 1 (Mode 1)

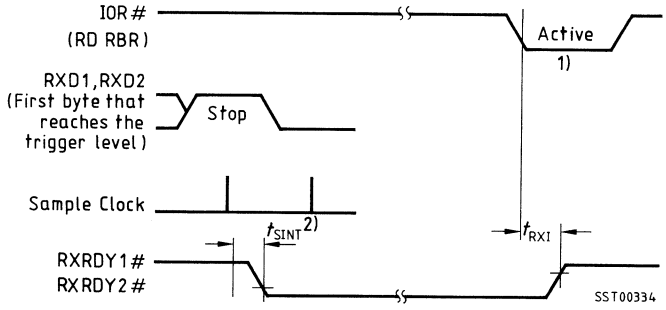


Receiver Ready FEWO = 0 or FEWO = 1 and DMS = 0 (Mode 0)



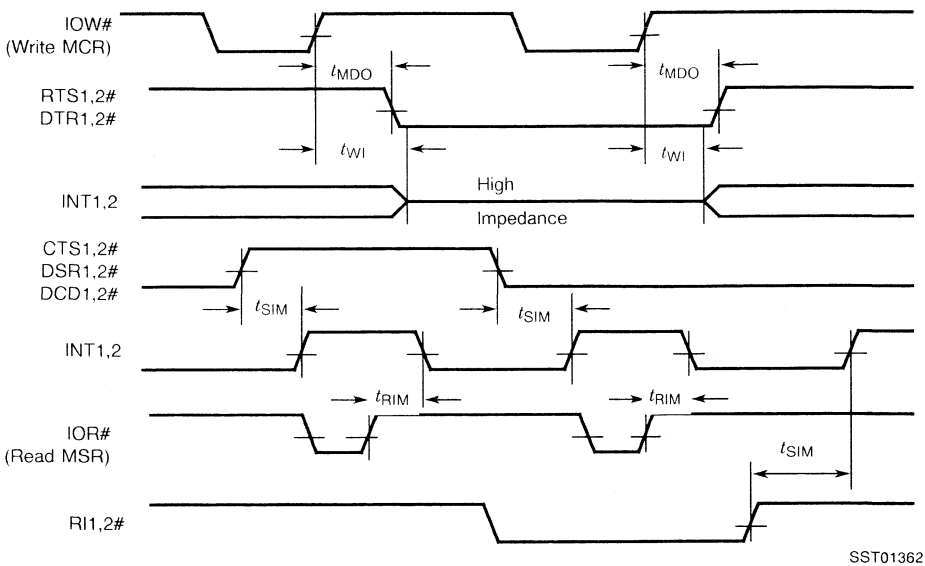
1) This is the reading of the last byte in the FIFO.
2) If FEWO=1, then t_{SINT} = 3 RCLK's. For a timeout interrupt t_{SINT} = 8 RCLK's.

Receiver Ready FEWO = 1 and DMS = 1 (Mode 1)

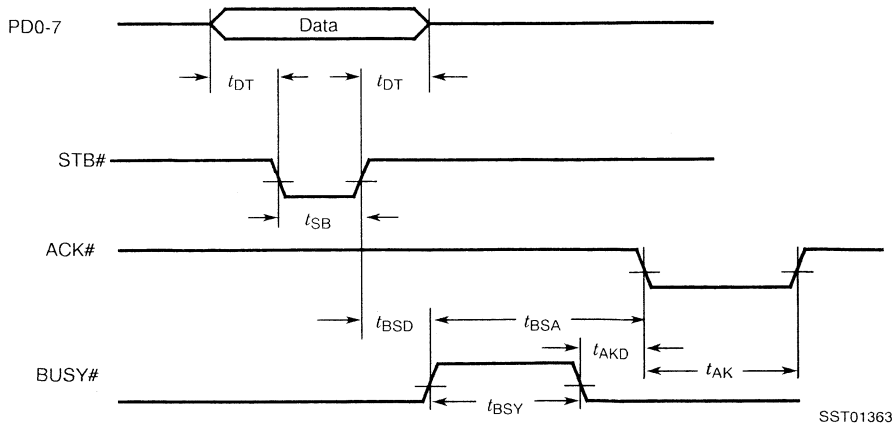


1) This is the reading of the last byte in the FIFO.
2) If FEWO = 1, then t_{SINT} = 3 RCLK's. For a timeout interrupt, t_{SINT} = 8 RCLK's.

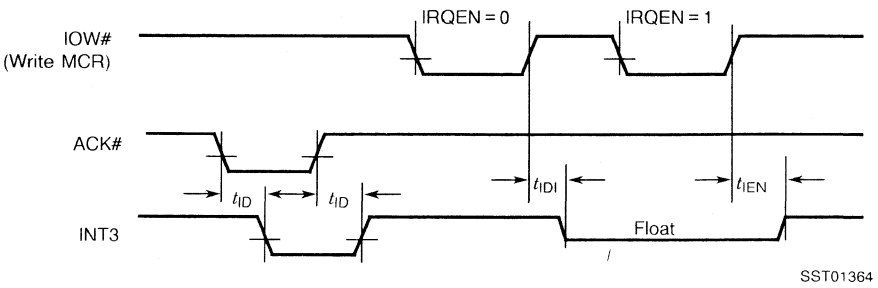
Modem Timing



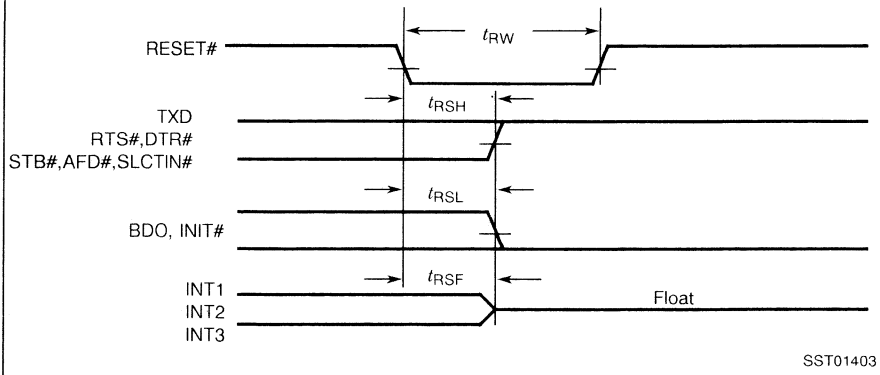
Typical Centronics Parallel Port Timing



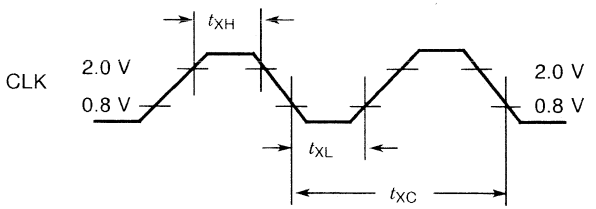
Parallel Port Interrupt Timing



Reset Timing

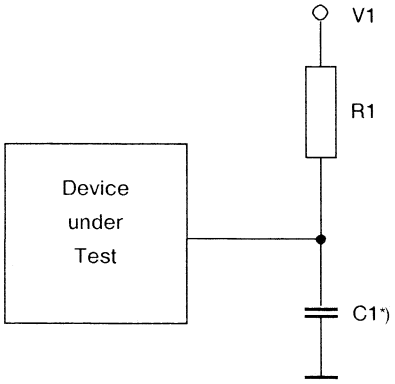


CLK Input



SST01404

AC Test Circuits



Related Device Pins	V1	R1	C1
PD0 – PD7	1.63 V	220 Ω	150 pF
INIT#, AFD#, STB#, SLCTIN#	2.54 V	510 Ω	150 pF
All other Pins	1.63 V	308 Ω	150 pF

*) Includes stray and jig capacitance

SST01405

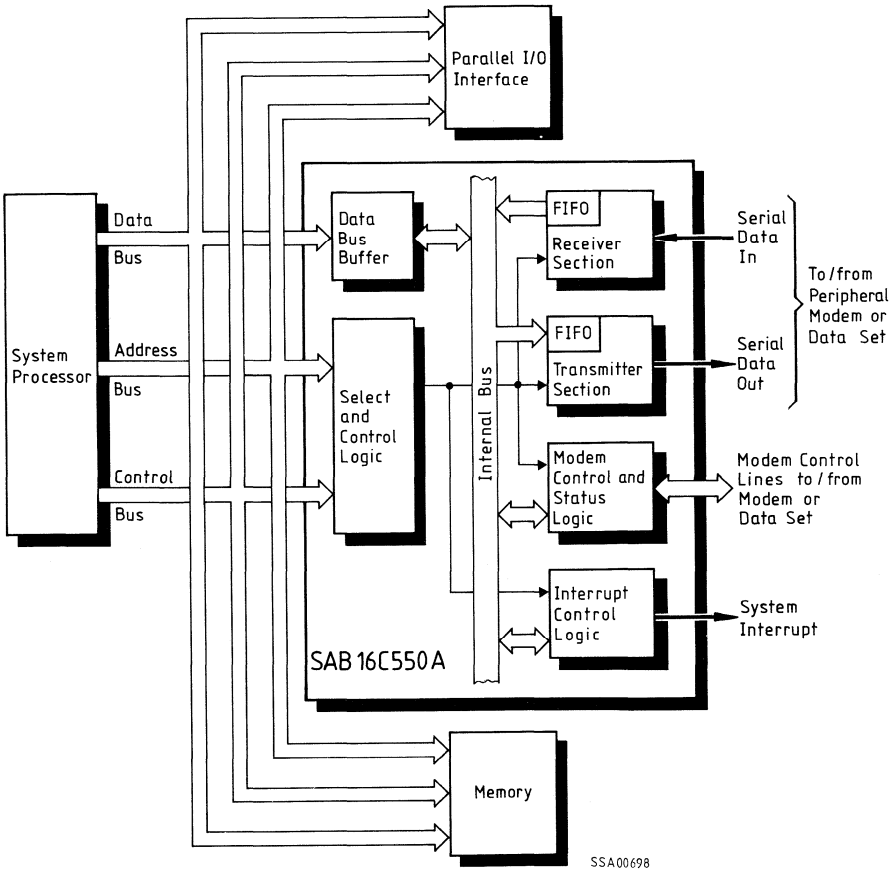
System Components

SIEMENS

SAB 16C550A
Universal Asynchronous Receiver/Transmitter with FIFOs

Advance Information

General System Configuration



- Capable of running all existing 16450 software
- Pin for pin compatible with the existing SAB 16C450 except for CSOUT (24) and NC (29). The former CSOUT and NC pins are TXRDY and RXRDY, respectively
- After reset, all registers are identical to the SAB 16C450 register set
- In the FIFO mode transmitter and receiver are each buffered with 16 byte FIFO's to reduce the number of interrupts presented to the CPU
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data stream
- Holding and shift registers eliminate the need for precise synchronization between the CPU and the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud generator allows division of any input clock by 1 to(2^{16}–1) and generates the internal 16× clock
- Independent receiver clock input
- Modem control functions (CTS, RTS, DSR, DTR, RI and DCD)
- False start bit detection
- Complete status reporting capabilities
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, $1\frac{1}{2}$-, or 2-stop bit generation
  - Baud generation (DC to 512 Kbaud)
- Tri-state TTL drive capability for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls
- Packages: P-DIP-40 and PL-CC-44

Ordering Information

Type	Ordering code	Package	Function
SAB 16C550A-P	Q67120-P319	P-DIP-40	Programmable communication interface with FIFOs
SAB 16C550A-N	Q67120-P318	PL-CC-44	Programmable communication interface with FIFOs

The SAB 16C550A is an improved version of the SAB 16C450 Universal Asynchronous Receiver/Transmitter (UART). The improved specifications ensure compatibility with state-of-the-art CPUs. Functionally identical to the SAB 16C450 on powerup (character mode) [1] the SAB 16C550A can be put into an alternate mode (FIFO mode) to relieve the CPU of excessive software overhead.

In this mode internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. All the logic is on chip to minimize system overhead and maximize system efficiency. Two pin functions have been changed to allow signalling of DMA transfers.

The SAB 16C550A performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error condition (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by 1 to (2^{16}–1), and of producing a 16× clock for driving the internal transmitter logic. Provisions have also been made to use this 16× clock for driving the receiver logic.

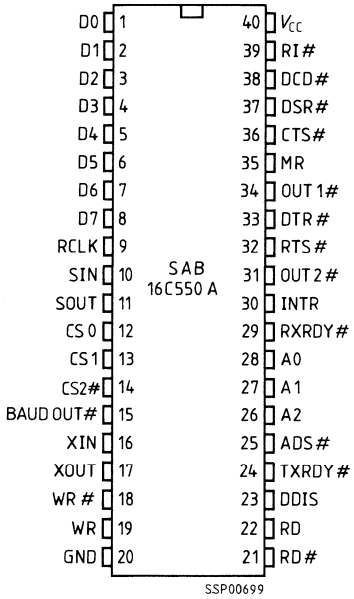
The UART features full modem-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required for handling the communications link.

The SAB 16C550A is fabricated in Siemens ACMOS technology and comes in a 40-pin plastic dual-in-line package (P-DIP-40) or in a 44-pin plastic leaded chip carrier (PL-CC-44).

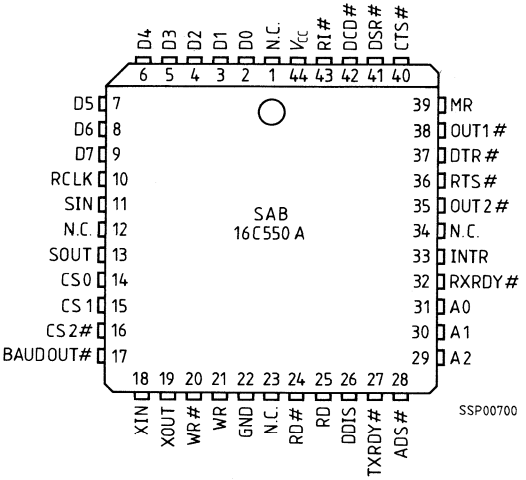
1) Can also be reset to 16450 mode under software control

Pin Configuration

P-DIP-40



PL-CC-44



Pin Definitions and Functions

Note: In the following descriptions, a low represents a logic 0 and a high represents a logic 1. Pin numbers are related to the plastic dual-in-line package (P-DIP-40).

Symbol	Pin	Input (I) Output (O)	Function
D0–D7	1–8	I/O	**Data bus** This bus comprises 8 tri-state input/ output lines. The bus provides bidirectional communication between the UART and the CPU. Data, control words, and status information are transferred via the D0–D7 Data Bus.
RCLK	9	I	**Receiver clock** This input is the 16× Baud rate clock input for the receiver section of the chip.
SIN	10	I	**Serial data in** Serial data input from the communications link (peripheral device, modem, or data set).
SOUT	11	O	**Serial data out** This is the composite serial data output to the communications link (peripheral, modem or data set). The SOUT signal is set to the marking (logic 1) state upon a master reset operation.
CS0 CS1 CS2#	12 13 14	I I I	**Chip select** When CS0 and CS1 are high and CS2# is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active address strobe signal latches the decoded chip select signals, completing chip selection. If ADS# is always low, valid chip selects should stabilize according to the t_{CSW} parameter.
BAUDOUT#	15	O	**Baud rate out#** This is the 16× clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud rate generator divisor latches. The BAUDOUT# may also be used for the receiver section by tying this output to the RCLK input of the chip.
XIN XOUT	16 17	I O	**Oscillator in / out** These two pins connect the main timing reference (crystal or signal clock) to the UART. When a crystal oscillator or a clock signal is provided, it drives the UART via XIN (see typical clock circuits).

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
WR# WR	18 19	I I	**Write / Write#** When WR is high or WR# is low while the chip is selected, the CPU can write control words or data into the selected UART register. *Note: Only one active WR or WR# input is required to transfer data to the UART during a write operation. Therefore, tie either the WR input permanently low or the WR# input permanently high, when it is not used.*
RD# RD	21 22	I I	**Read / Read#** When RD is high or RD# is low while the chip is selected, the CPU can read status information or data from the selected UART register. *Note: Only one active RD or RD# input is required to transfer data from the UART during a read operation. Therefore, tie either the RD input permanently low the RD# input permanently high, when it is not used.*
DDIS	23	O	**Driver disable** This signal goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the UART.
TXRDY# RXRDY#	24 29	O O	**Transmitter ready# / Receiver ready#** Transmitter and Receiver DMA signalling is available through two pins. When operating in the FIFO mode, one of two types of DMA signalling per pin can be selected via DMS. When operating as in the 16450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multitransfer DMA where multiple transfers are made continuously until the RCVR FIFO has been emptied or the XMIT FIFO has been filled. **RXRDY Mode 0** When in the 16450 Mode (FEWO = 0) or in the FIFO Mode (FEWO = 1, DMS = 0), and when there is at least 1 character in the RCVR FIFO or RCVR holding register, the RXRDY# pin will be low active. Once it is activated the RXRDY# pin will go inactive when there are no more characters in the FIFO or holding register.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
TXRDY# RXRDY# (cont'd)			**RXRDY Mode 1** In the FIFO Mode (FEWO = 1) when the DMS = 1 and the trigger level or the timeout has been reached, the RXRDY# pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO or holding register. **TXRDY Mode 0** In the 16450 Mode (FEWO = 0) or in the FIFO Mode (FEWO = 1, DMS = 0), and when there are no characters in the XMIT FIFO or XMIT holding register, the TXRDY# pin will be low active. Once it is activated the TXRDY# pin will go inactive after the first character is loaded into the XMIT FIFO or holding register. **TXRDY Mode 1** In the FIFO Mode (FEWO = 1), when DMS = 1 and there is at least one unfilled position in the XMIT FIFO, it will go low active. This pin will become inactive when the XMIT FIFO is completely full.
ADS#	25	I	**Address strobe#** The positive edge of an active address strobe (ADS#) signal latches the register select (A0, A1, A2) and chip select (CS0, CS1, CS2#) signals. *Note: An active ADS# input is required when the register select (A0, A1, A2) signals are not stable for the duration of a read or write operation.* *If not required, tie the ADS# input permanently low.*
A2–A0	26–28	I	**Address 2–0** Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the divisor latch access bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the baud rate generator divisor latches.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A2–A0 (cont'd)			

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver buffer (read), Transmitter holding register (write)
0	0	0	1	Interrupt enable
X	0	1	0	Interrupt identification (read)
X	0	1	0	FIFO control (write)
X	0	1	1	Line control
X	1	0	0	Modem control
X	1	0	1	Line status
X	1	1	0	Modem status
X	1	1	1	Scratch
1	0	0	0	Divisor latch (least significant byte)
1	0	0	1	Divisor latch (most significant byte)

INTR	30	O	**Interrupt request** This signal goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER. Receiver error flag; received data available; timeout (FIFO mode only); transmitter holding register empty; and modem status. The INTR signal is reset low upon the appropriate interrupt service or a master reset operation.
OUT2#	31	O	**Output 2#** This user-designated output can be set to an active low by programming bit 3 (OUT 2) of the modem control register to a high level. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
RTS#	32	O	**Request to send#** When low, this informs the modem or data set that the UART is ready to exchange data. The RTS# output signal can be set to an active low by programming bit 1 (RTS) of the modem control register. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

Pin Definitions and Functions (cont'd)

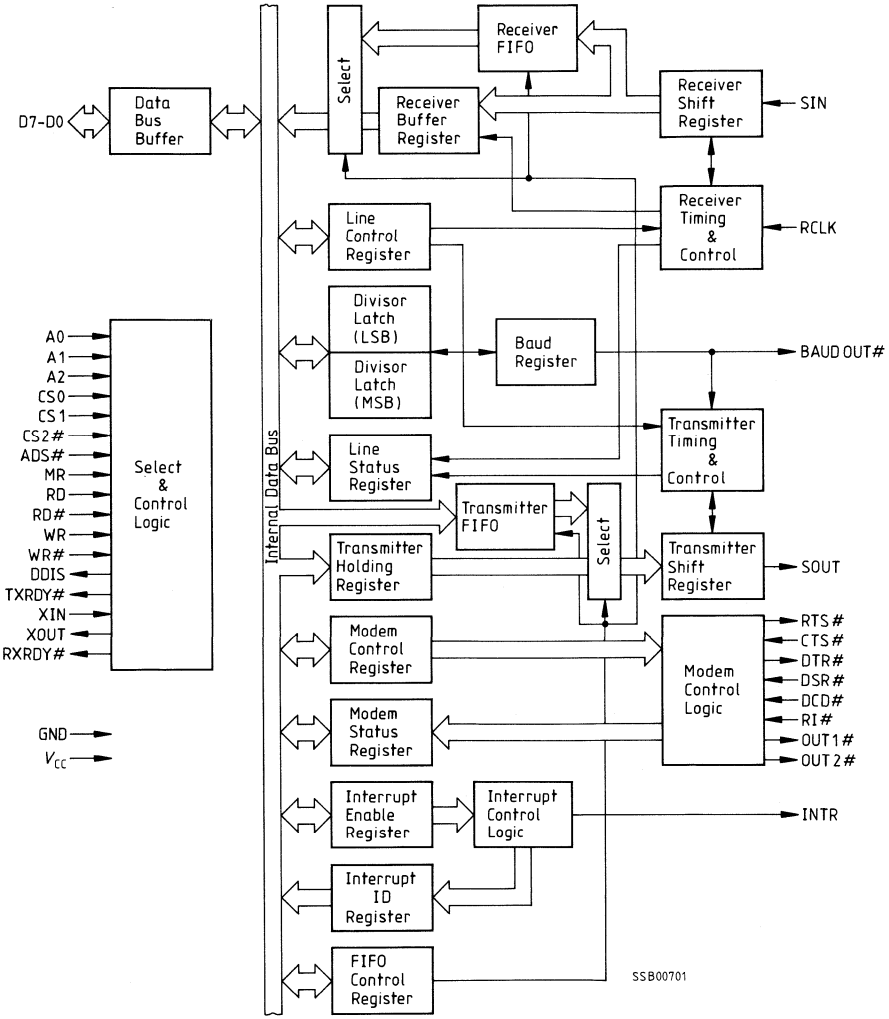
Symbol	Pin	Input (I) Output (O)	Function
DTR#	33	O	**Data terminal ready#** When low, this informs the modem or data set that the UART is ready to establish a communications link. The DTR# output signal can be set to an active low by programming bit 0 (DTR) of the modem control register to a high level. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
OUT1#	34	O	**Output 1#** This user-designated output can be set to an active low by programming bit 2 (OUT1) of the modem control register to a high level. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
MR	35	I	**Master reset** When this input is high, all the registers (except for the receiver buffer, transmitter holding, and divisor latches) and the control logic of the UART are cleared. The states of various output signals (SOUT, INTR, OUT1#, OUT2#, RTS#, DTR#) are affected by an active MR input (refer to Table 2). This input is buffered with a TTL-compatible Schmitt trigger with 0.5 V typical hysteresis.
CTS#	36	I	**Clear to send#** When low, this indicates that the modem or data set is ready to exchange data. The CTS# signal is a modem status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the modem status register. Bit 4 is the complement of the CTS# signal. Bit 0 (DCTS) of the modem status register indicates whether the CTS# input has changed state since the previous reading of the modem status register. CTS# has no effect on the transmitter. *Note: Whenever the CTS bit of the modem status register changes state, an interrrupt is generated if the modem status interrupt is enabled.*

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
DSR#	37	I	**Data set ready#** When low, this signal indicates that the modem or data set is ready to establish the communications link with the UART. The DSR# signal is a modem status input whose condition can be tested by the CPU reading bit 5 (DSR) of the modem status register. Bit 5 is the complement of the DSR# signal. Bit 1 (DDSR) of the modem status register indicates whether the DSR# input has changed state since the previous reading of the modem status register. *)
DCD#	38	I	**Data carrier detect#** When low, it indicates that the data carrier has been detected by the modem or data set. The DCD# signal is a modem status input whose condition can be tested by the CPU reading bit 7 (DCD) of the modem status register. Bit 7 is the complement of the DCD# signal. Bit 3 (DDCD) of the modem status register indicates whether the DCD# input has changed state since the previous reading of the modem status register. DCD# has no effect on the receiver. *)
RI#	39	I	**Ring indicator#** When low, this signal indicates that a telephone ringing signal has been received by the modem or data set. The RI# signal is a modem status input whose condition can be tested by the CPU reading bit 6 (RI) of the modem status register. Bit 6 is the complement of the RI# signal. Bit 2 (TERI) of the modem status register indicates whether the RI# input signal has changed from a low to a high state since the previous reading of the modem status register. *Note: Whenever the RI bit of the modem status register changes from a high to a low state, an interrupt is generated if the modem status interrupt is enabled.*
V_{CC}	40	–	**Power supply** (+ 5 V)
GND	20	–	**Ground** (O V)

*) *Whenever the DSR bit etc. DCD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.*

Block Diagram



Register Description

Table 1
Summary of Registers

Bit No.	Register Address					
	0 (DLAB = 0)	0 (DLAB = 0)	1 (DLAB = 0)	2	2	3
	Receiver buffer register (read only)	Transmitter holding register (write only)	Interrupt enable register	Interrupt ident. register (read only)	FIFO control register (write only)	Line control register
	RBR	THR	IER	IIR	FCR	LCR
0	Data bit 0 [1]	Data bit 0 [1]	Enable received data available interrupt (ERBFI)	"0" if interrupt is pending	FIFO enable (FEWO)	Word length select bit 0 (WLS0)
1	Data bit 1	Data bit 1	Enable transmitter holding register empty (ETBEI)	Interrupt ID bit 0 (IIDB0)	Receiver FIFO reset (RFR)	Word length select bit 1 (WLS1)
2	Data bit 2	Data bit 2	Enable receiver line status interrupt (ERLSI)	Interrupt ID bit 1 (IIDB1)	Transmitter FIFO reset (TFR)	Number of stop bits (STB)
3	Data bit 3	Data bit 3	Enable modem status interrupt (EDSSI)	Interrupt ID bit 2 (IIDB 2)	DMA mode select (DMS)	Parity enable (PEN)
4	Data bit 4	Data bit 4	0	0	Reserved	Even parity select (EPS)
5	Data bit 5	Data bit 5	0	0	Reserved	Stick parity (STP)
6	Data bit 6	Data bit 6	0	FIFOs enabled (FE) [2]	RCVR FIFO trigger level (LSB)	Set break (SBR)
7	Data bit 7	Data bit 7	0	FIFOs enabled (FE) [2]	RCVR FIFO trigger level (MSB)	Divisor latch access bit (DLAB)

Table 1
Summary of Registers (cont'd)

Bit No.	Register Address					
	4	5	6	7	0 (DLAB = 1)	1 (DLAB = 1)
	Modem control register	**Line status register**	**Modem status register**	**Scratch register**	**Divisor latch (LS)**	**Divisor latch (MS)**
	MCR	**LSR**	**MSR**	**SCR**	**DLL**	**DLM**
0	Data terminal ready (DTR)	Data ready (DR)	Delta clear to send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to send (RTS)	Overrun error (OE)	Delta data set ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Out 1	Parity error (PE)	Trailing edge ring indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Out 2	Framing error (FE)	Delta data carrier detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Loop	Break interrupt (BI)	Clear to send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter holding register (THRE)	Data set ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter empty (TEMT)	Ring indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO (EIRF) [2]	Data carrier detect (DCD)	Bit 7	Bit 7	Bit 15

1) Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
2) These bits are always 0 in the SAB 16C450 compatible mode.

Table 2
Register Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt enable register	Master reset	**0000** 0000 1)
Interrupt identification register	Master reset	0**000** 0001
FIFO control register	Master reset	0**000** 0000
Line control register	Master reset	0000 0000
Modem control register	Master reset	**0000** 0000
Line status register	Master reset	0110 0000
Modem status register	Master reset	XXXX 0000 2)
SOUT	Master reset	High
INTR (RCVR errors)	Read LSR/MR	Low
INTR (RCVR data ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/write THR/MR	Low
INTR (Modem status changes)	Read MSR/MR	Low
OUT2#	Master reset	High
RTS#	Master reset	High
DTR#	Master reset	High
OUT1#	Master reset	High
RCVR FIFO	MR/RFR • FEWO/ΔFEWO	All bits low
XMIT FIFO	MR/RFR • FEWO/ΔFEWO	All bits low

1) Boldface bits are permanently low.
2) Bits 7-4 are driven by the input signals.

The sytem programmer may access any of the UART registers summarized in Table 1 via the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table 1 has its name and reset state shown in Table 2.

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange and sets the divisor latch access bit via the line control register (LCR). The programmer can also read the contents of the line control register. The read capability simplifies system programming and eliminates the need for separate storage of the line characteristics in system memory.

Table 1 shows the contents of the LCR. Details on each bit follow:

Bit 0 and 1: (WLS0, WLS1) These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: (STB) This bit specifies the number of stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one stop bit is generated or checked in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop-bit only, regardless of the number of stop bits selected.

Bit 3: (PEN) This bit is the parity enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).

Bit 4: (EPS) This bit is the even parity select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's is transmitted or checked.

Bit 5: (STP) This bit is the stick parity bit. When bits 3, 4 and 5 are logic 1 the parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is logic 0 then the parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 stick parity is disabled.

Bit 6: (SBR) This bit is the break control bit. It causes a break condition to be transmitted by the UART. When it is set to a logic 1, the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by clearing bit 6 to a logic 0. The break control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. *Load an all O's pad character in response to THRE.*
2. *Set break after the next THRE.*
3. *Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission is to be restored. During the break, the transmitter can be used as a character timer to accurately establish the break duration.*

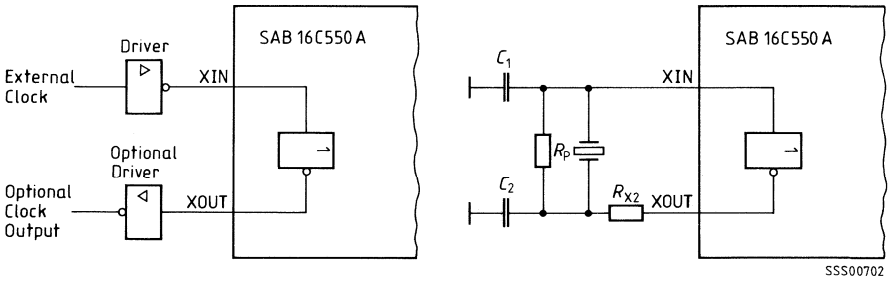
Bit 7: (DLAB) This bit is the divisor latch access bit. It must be set high (logic 1) to access the divisor latches of the baud generator during a read or write operation. It must be set low (logic 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

Programmable Baud Rate Generator

The UART contains a programmable baud rate generator capable of taking any clock input from DC to 8.0 MHz and dividing it by any divisor from 1 to 2^{16}. The output frequency of the baud rate generator is 16 × the baud rate [divisor = (frequency input) ÷ (baud rate × 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded.

Tables 3, 4 and 5 provide decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 8 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended.

Typical Clock Circuits



Typical Oscillator Networks

Crystal	R_P	R_{X2}	C_1	C_2
1.8 – 8.0 MHz	1 MΩ	1.5 k	10 – 30 pF	40 – 60 pF

Table 3
Baud Rates Using 1.8432 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 × clock	Percent error difference between desired and actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Table 4
Baud Rates Using 3.072 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 × clock	Percent error difference between desired and actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–
56000	3	14.285

Table 5
Baud Rates Using 8 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 × clock	Percent error difference between desired and actual
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

Line Status Register (LSR)

This 8-bit register provides the CPU with status information to concerning the data transfer. Table 1 shows the contents of the Line Status Register. Details on each bit follow:

Bit 0: (DR) This bit is the receiver data ready indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the receiver buffer register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the receiver buffer register or the FIFO.

Bit 1: (OE) This bit is the overrun error indicator. Bit 1 indicates that data in the receiver buffer register was not read by the CPU before the next character was transferred into the receiver buffer register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition, and reset whenever the CPU reads the contents of the line status register. If in the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

Bit 2: (PE) This bit is the parity error indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the line status register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: (FE) This bit is the framing error indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic 1 whenever the stop bit following the last data bit or parity bit is detected as a logic 0 bit (spacing level). The FE indicator is reset whenever the CPU reads the contents of the line status register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".

Bit 4: (BI)
This bit is the break interrupt indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits).The BI indicator is reset whenever the CPU reads the contents of the line status register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to.This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: (THRE)
This bit is the transmitter holding register empty indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the transmit holding register empty interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: (TEMT)
This bit is the transmitter empty indicator. Bit 6 is set to a logic 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: (EIRF)
In the 16450 mode this is a 0. In the FIFO mode EIRF is set when there is at least one parity error, framing error or break indication in the FIFO. EIRF is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

Note: The line status register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

FIFO Control Register

This is a write only register at the same address location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Bit 0: (FEWO) Writing a 1 to FEWO enables both the XMIT and RCVR FIFOs. Resetting FEWO will clear all bytes in both FIFOs. When changing from FIFO mode to 16450 mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to, or they will not be programmed.

Bit 1: (RFR) Writing a 1 to RFR clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: (TFR) Writing a 1 to TFR clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: (DMS) Setting DMS to a 1 will cause the RXRDY and TXRD pins to change from mode 0 to mode 1 if FEWO = 1 (see description of RXRDY and TXRDY pins).

Bit 4 and 5: These bits are reserved for future use.

Bit 6 and 7: FCR6 and FCR 7 are used to set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Interrupt Identification Register

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt identification register. The four levels of interrupt conditions in order of priority are receiver line status; received data ready; transmitter holding register empty; and modem status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table 1 shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: (IIDB0; IIDB1) These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 6.

Bits 3: (IIDB2) In the SAB 16C450 mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5: These two bits of the IIR are always logic 0.

Bits 6 and 7: (FE) These two bits are set when FEWO = 1.

Table 6
Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	–	None	None	–
0	1	1	0	Highest	Receiver line status	Overrun error or parity error or framing error or break interrupt	Reading the line status register
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	Reading the receiver buffer register or the FIFO drops below the trigger level
1	1	0	0	Second	Character timeout indication	No characters have been removed from or input to the RCVR FIFO during the last 4 char. times and there is at least 1 char. in it during this time	Reading the receiver buffer register
0	0	1	0	Third	Transmitter holding register empty	Transmitter holding register empty	Reading the IIR register (if source of interrupt) or writing into the transmitter holding register
0	0	0	0	Fourth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect	Reading the modem status register

Interrupt Enable Register

This register enables the five types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt enable register (IER). Similarly, setting bits of this register to a logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. Table 1 shows the contents of the IER. Details on each bit follow:

Bit 0: (ERBFI) This bit enables the received data available interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1: (ETBEI) This bit enables the transmitter holding register empty interrupt when set to logic 1.

Bit 2: (ERLSI) This bit enables the receiver status interrupt when set to logic 1.

Bit 3: (EDSSI) This bit enables the modem status interrupt when set to logic 1.

Bit 4 through 7: These four bits are always logic 0.

Modem Control Register

This register controls the interface with the modem or data set (or a peripheral device emulating a modem). The contents of the modem control register (MCR) are indicated in Table 1. Details on each bit follow:

Bit 0: (DTR) This bit controls the data terminal ready output. When bit 0 is set to a logic 1, the DTR# output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR# output is forced to a logic 1.

Note: The DTR# output of the UART may be applied to an EIA inverting line driver (such as the 1488) to obtain the proper polarity input at the succeeding modem or data set.

Bit 1: (RTS) This bit controls the request to send output. Bit 1 affects the RTS# output in a manner identical to that described above for bit 0.

Bit 2: (OUT1) This bit controls the output 1 signal, which is an auxiliary user-designated output. Bit 2 affects the OUT1# output in a manner identical to that described above for bit 0.

Bit 3: (OUT2) This bit controls the output 2 signal, which is an auxiliary user-designated output. Bit 3 affects the OUT2# output in a manner identical to that described above for bit 0.

Bit 4: (LOOP) This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter serial output (SOUT) is set to the marking (logic 1) state; the receiver serial input (SIN) is disconnected; the output of the transmitter shift register is "looped back" into the receiver shift register input; the four modem control inputs (CTS#, DSR#, RI#, and DCD#) are disconnected; and the four modem control outputs (DTR#, RTS#, OUT 1#, and OUT2#) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupt's sources are now the lower four bits of the modem control register instead of the four modem control inputs. The interrupts are still controlled by the interrupt enable register.

Bits 5 through 7: These bits are permanently set to logic 0.

Modem Status Register

This register provides the current state of the control lines from the modem (or peripheral device) to the CPU. In addition to this current-state information, four bits of the modem status register provide change information. These bits are set to a logic 1 whenever a control input from the modem changes state. They are reset to logic 0 whenever the CPU reads the modem status register.

Table 1 shows the contents of the MSR. Details on each bit follow.

Bit 0: (DCTS) This bit is the delta clear to send indicator. Bit 0 indicates that the CTS# input to the chip has changed state since the last time it was read by the CPU.

Bit 1: (DDSR) This bit is the delta data set ready indicator. Bit 1 indicates that the DSR# input to the chip has changed state since the last time it was read by the CPU.

Bit 2: (TERI) This bit is the trailing edge of ring indicator detector. Bit 2 indicates that the RI# input to the chip has changed from a low to a high state.

Bit 3: (DDCD) This bit is the delta data carrier detect indicator. Bit 3 indicates that the DCD# input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a modem status interrupt is generated.

Bit 4: (CTS) This bit is the complement of the clear to send input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: (DSR) This bit is the complement of the data set ready input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: (RI) This bit is the complement of the ring indicator input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.

Bit 7: (DCD) This bit is the complement of the data carrier detect input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

Scratchpad Register

This 8-bit read/write register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FEWO = 1, ERBFI = 1) RCVR interrupts will occur as follows:

a) The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

b) The IIR receive data available indicaton also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

c) The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.

d) The data ready bit (DR) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

a) A FIFO timeout interrupt will occur, if the following conditions exist:
   - at least one character is in the FIFO
   - the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
   - the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

   This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with a 12-bit character.

b) Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).

c) When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

d) When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FEWO = 1, ETBEI = 1), XMIT interrupts will occur as follows:

a) The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

b) The transmitter FIFO empty indication will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE = 1, and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FEWO will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation

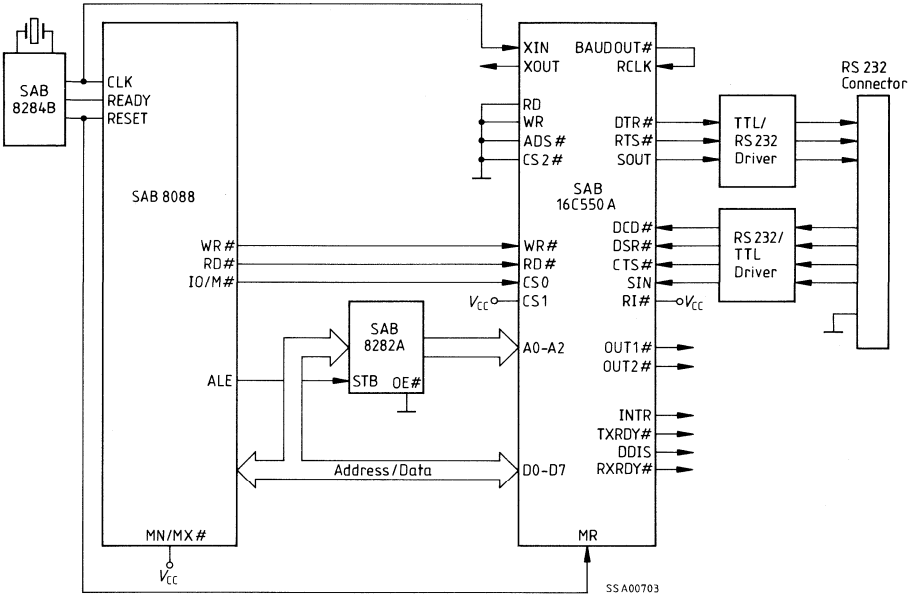
With FEWO = 1 resetting ERBFI, ETBEI, ERLSI, EDSSI or all to zero puts the UART in the FIFO polled mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check RCVR and XMITTER status via the LSR. As stated previously:

- DR will be set as long as there is one byte in the RCVR FIFO.
- LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since ERLSI = 0.
- THRE will indicate when the XMIT FIFO is empty.
- TEMT will indicate that both the XMIT FIFO and shift register are empty.
- EIRF will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO polled mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Typical Application



Absolute Maximum Ratings

Ambient temperature under bias . . . . . 0 to + 70 °C
Storage temperature . . . . . – 65 to + 150 °C
Supply storage . . . . . – 0.5 to + 7 V
Voltage on any pin with respect to ground . . . . . – 0.5 to V_{CC} + 0.5 V
Power dissipation . . . . . 1 W

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5%; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	– 0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.4	V	I_{OL} = 1.6 mA 1)
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = – 1.0 mA 1)
Avg. power supply current	I_{CC} (AV)	–	10	mA	V_{CC} = 5.25 V, T_A = 25 °C; no loads on output SIN, DSR#, DCD#, CTS#, RI# = 2.0 V; all other inputs = 0.8 V; Baud rate generator is 8 MHz; Baud rate is 512 KBaud
Input leakage current	I_{IL}	–	± 10	µA	V_{CC} = 5.25 V; GND = 0 V; all other pins floating; V_{IN} = 0 V, 5.25 V
Clock leakage current	I_{CL}				
Tri-state leakage current	I_{OZ}	–	± 20	µA	V_{CC} = 5.25 V; GND = 0 V; V_{OUT} = 0 V, 5.25 V 1. Chip deselected 2. WRITE mode, chip selected
MR Schmitt V_{IL}	V_{ILMR}	–	0.8	V	–
MR Schmitt V_{IH}	V_{IHMR}	2.0	–	V	–

Capacitance 2)

T_A = 25 °C; V_{CC} = GND = 0 V

Clock input capacitance	C_{XIN}	–	20	pF	f_C = 1 MHz Unmeasured pins returned to GND
Clock output capacitance	C_{XOUT}	–	30	pF	
Input capacitance	C_{IN}	–	10	pF	
Output capacitance	C_{OUT}	–	20	pF	

1) Does not apply to pin XOUT.
2) These parameters are periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 5%; GND = 0 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Address strobe width	t_{ADS}	60	–	ns	–
Address hold time	t_{AH}	0	–	ns	–
RD, RD# delay from address	t_{AR}	30	–	ns	1)
Address setup time	t_{AS}	60	–	ns	–
WR, WR# delay from address	t_{AW}	30	–	ns	1)
Chip select hold time	t_{CH}	0	–	ns	–
Chip select setup time	t_{CS}	60	–	ns	–
RD, RD# delay from chip select	t_{CSR}	30	–	ns	1)
WR, WR# delay from select	t_{CSW}	30	–	ns	1)
Data hold time	t_{DH}	30	–	ns	–
Data setup time	t_{DS}	30	–	ns	–
RD, RD# to floating data delay	t_{HZ}	0	100	ns	100 pF loading 2)
Master reset pulse width	t_{MR}	5	–	µs	–
Address hold time from RD, RD#	t_{RA}	20	–	ns	1)
Read cycle delay	t_{RC}	125	–	ns	–
Chip select hold time from RD, RD#	t_{RCS}	20	–	ns	1)
RD, RD# strobe width	t_{RD}	125	–	ns	–
RD, RD# to driver disable delay	t_{RDD}	–	60	ns	100 pF loading 2)
Delay from RD, RD# to data	t_{RVD}	–	125	ns	100 pF loading
Address hold time from WR, WR#	t_{WA}	20	–	ns	1)
Write cycle delay	t_{WC}	150	–	ns	–
Chip select hold time from WR, WR#	t_{WCS}	20	–	ns	1)
WR, WR# strobe width	t_{WR}	100	–	ns	–
Duration of clock high pulse	t_{XH}	55	–	ns	External clock = 8 MHz max.
Duration of clock low pulse	t_{XL}	55	–	ns	External clock = 8 MHz max.
Read cycle = $t_{AR} + t_{RD} + t_{RC}$	RC	280	–	ns	–
Write cycle = $t_{AW} + t_{WR} + t_{WC}$	WC	280	–	ns	–

1) Applicable only when ADS# is tied low.

2) Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

AC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Baud Rate Generator					
Baud divisor	N	1	$2^{16}-1$		–
Baud output positive edge delay	t_{BHD}	–	175	ns	100 pF load
Baud output negative edge delay	t_{BLD}	–	175	ns	100 pF load
Baud output up time	t_{HW}	75	–	ns	1)
Baud output down time	t_{LW}	100	–	ns	1)
Receiver and Transmitter					
Delay from RD, RD# (RD RBR or RD LSR) to reset interrupt	t_{RINT}	–	1	µs	100 pF load
Delay from RCLK to sample time	t_{SCD}	–	2	µs	–
Delay from stop to set interrupt	t_{SINT}	–	1	4)	2)
Delay from WR, WR# (WR THR) to reset interrupt	t_{HR}	–	175	ns	100 pF load
Delay from RD, RD# (RD IIR) to reset interrupt (THRE)	t_{IR}	–	250	ns	100 pF load
Delay from initial INTR reset to transmit start	t_{IRS}	8	24	5)	3)
Delay from initial to write to interrupt	t_{SI}	16	24	5)	3)
Delay from stop to interrupt (THRE)	t_{STI}	8	8	5)	–
Delay from start to TXRDY active	t_{SXA}	–	8	5)	100 pF load
Delay from write to TXRDY inactive	t_{WXI}	–	195	ns	100 pF load
Modem control					
Delay from WR, WR# (WR MCR) to output	t_{MDO}	–	200	ns	100 pF load
Delay to reset interrupt from RD, RD# (RD MSR)	t_{RIM}	–	250	ns	100 pF load
Delay to set interrupt from Modem input	t_{SIM}	–	250	ns	100 pF load

1) $f_x = 8.0$ MHz, ÷2, 100 pF load

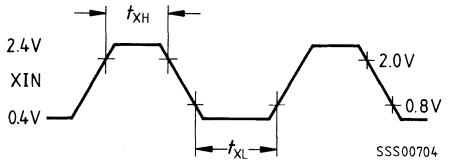
2) In the FIFO mode (FCRO = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RD RBR goes inactive. Timeout interrupt is delayed 8 RCLKs.

3) This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active. (See FIFO interrupt mode operation).

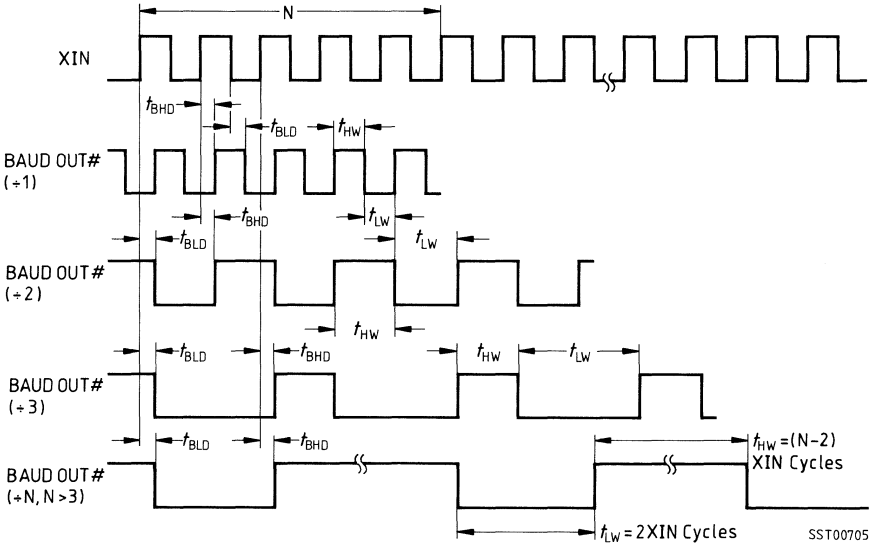
4) RCLK cycles.

5) BAUD-OUT cycles.

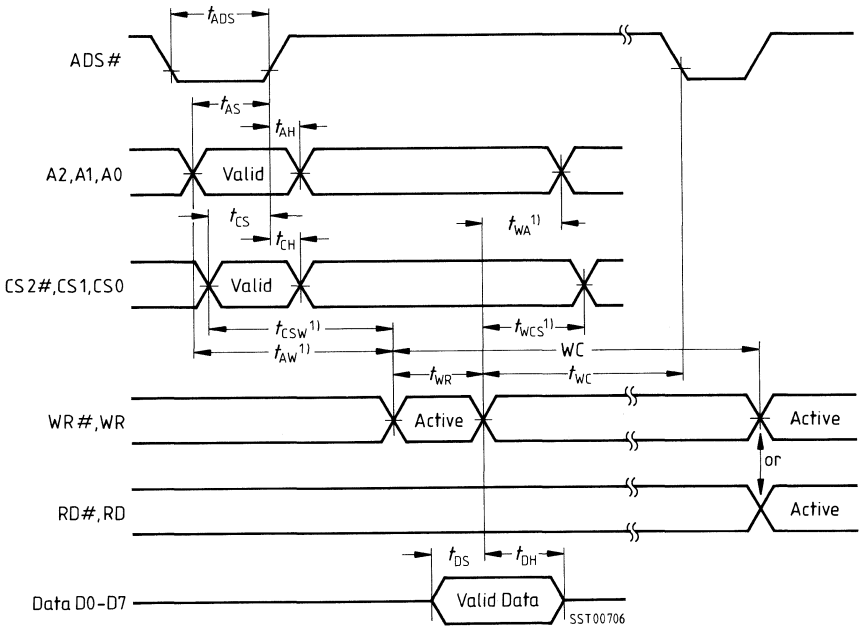
External Clock Input Timing



BAUDOUT Timing

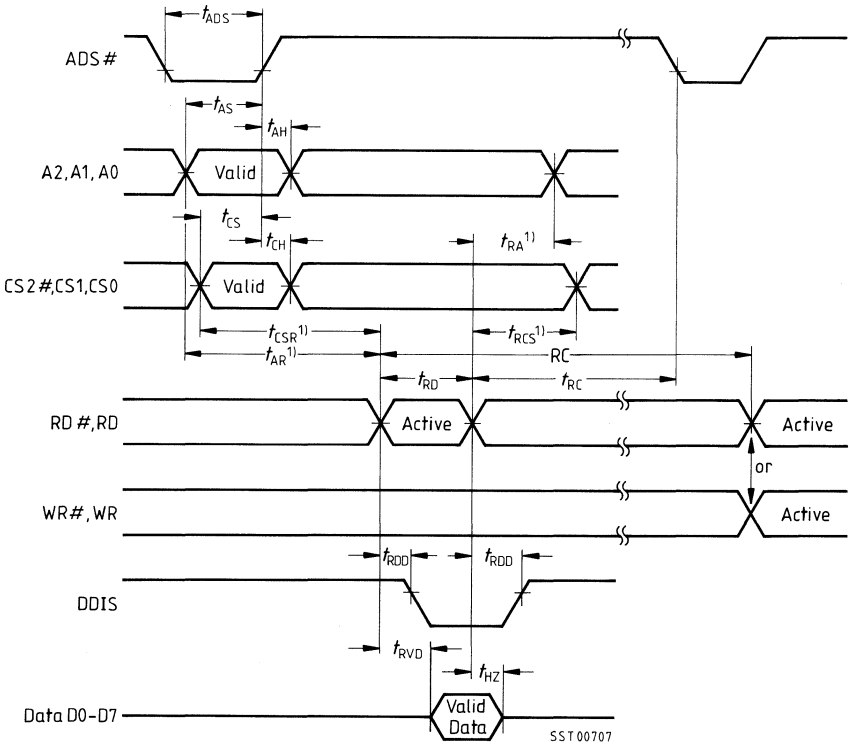


Write Cycle Timing



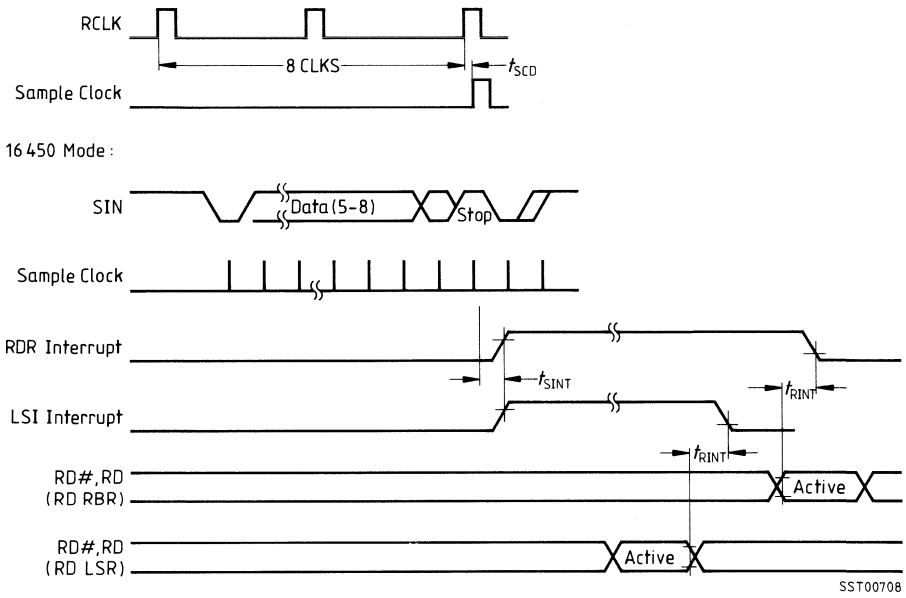
1) Applicable only when ADS # is tied low.

Read Cycle Timing

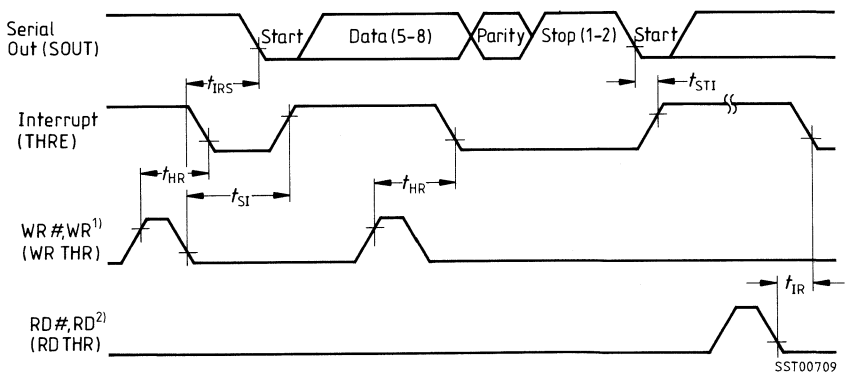


1) Applicable only when ADS # is tied low.

Receiver Timing

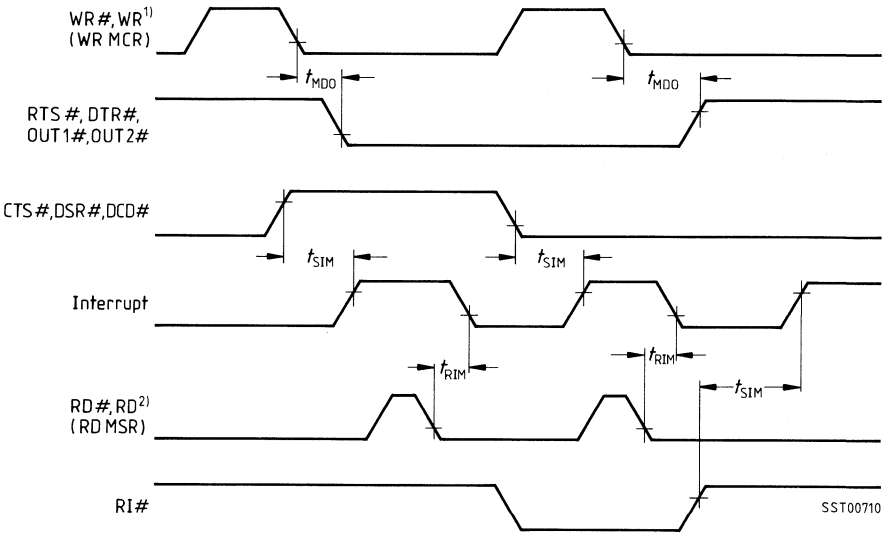


Transmitter Timing



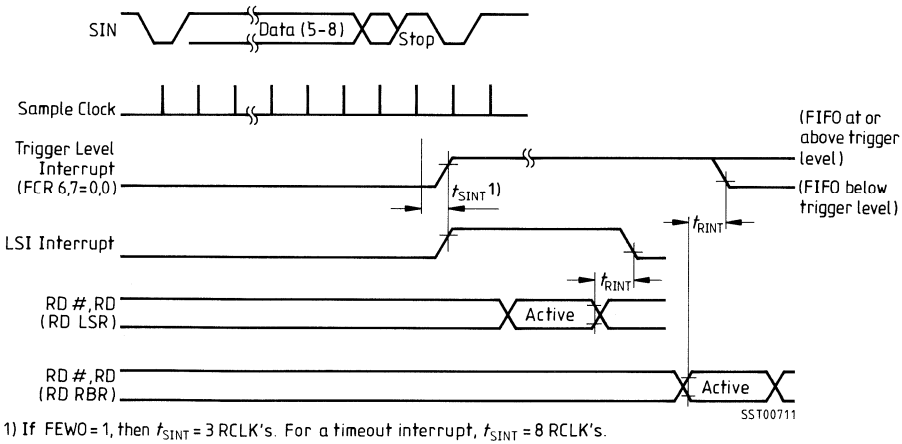
[1)] See Write Cycle Timing
[2)] See Read Cycle Timing

Modem Control Timing



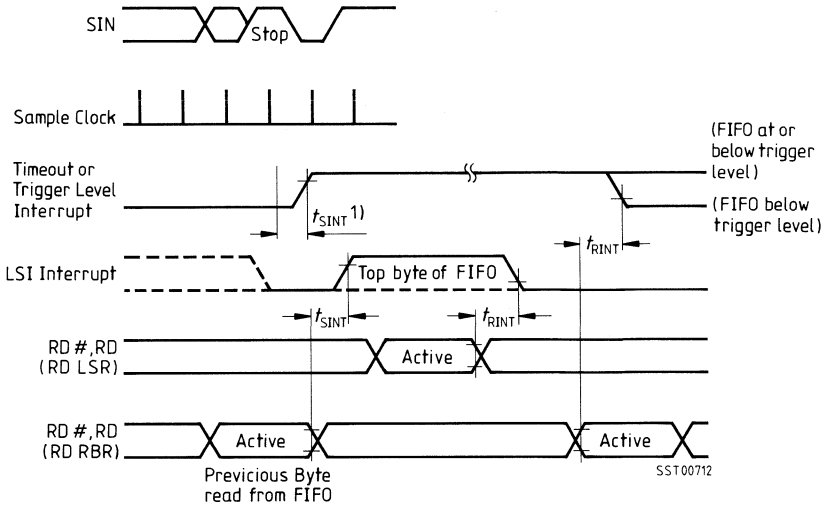
[1] See Write Cycle Timing
[2] See Read Cycle Timing

Receiver FIFO First Byte (this sets RDR)



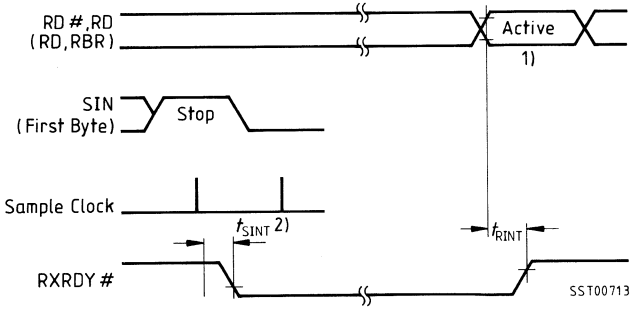
1) If FEWO = 1, then t_{SINT} = 3 RCLK's. For a timeout interrupt, t_{SINT} = 8 RCLK's.

Receiver FIFO Bytes other than the First Byte (RDR is already set)



1) If FEWO = 1, then t_{SINT} = 3 RCLK's. For a timeout interrupt, t_{SINT} = 8 RCLK's

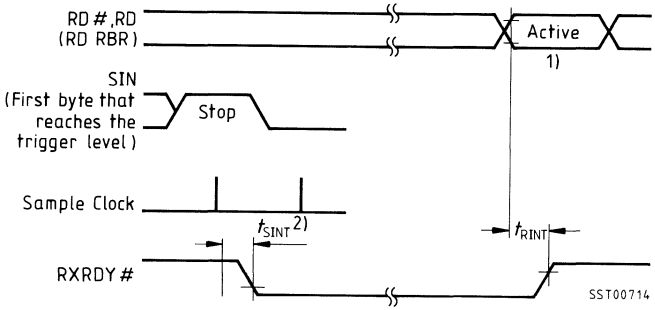
Receiver Ready (Pin 29) FEWO = 0 or FEWO = 1 and DMS = 0 (Mode 0)



1) This is the reading of the last byte in the FIFO.

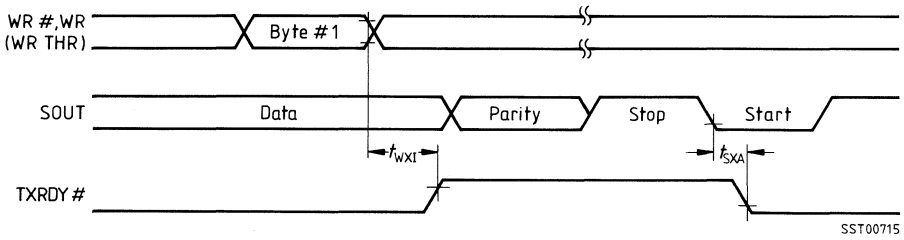
2) IF FEWO = 1, then t_{SINT} = 3 RCLK's. For a timeout interrupt, t_{SINT} = 8 RCLK's.

Receiver Ready (Pin 29) FEWO = 1 and DMS = 1 (Mode 1)

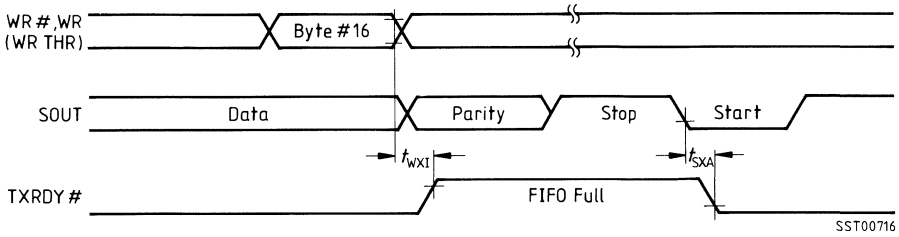


1) This is the reading of the last byte in the FIFO.
2) If FEWO = 1, then t_{SINT} = 3 RCLK's. For a timeout interrupt, t_{SINT} = 8 RCLK's.

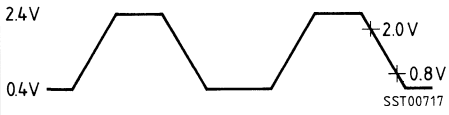
Transmitter Ready (Pin 24) FEWO = 0 or FEWO = 1 and DMS = 0 (Mode 0)



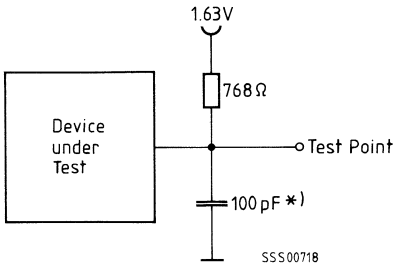
Transmitter Ready (Pin 24) FEWO = 1 and DMS = 1 (Mode 1)



AC Test Points



AC Test Circuit



*) Includes stray and jig capacitance

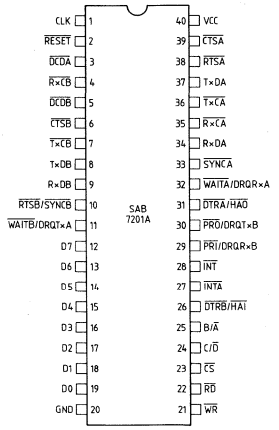
SIEMENS

Advance Information

SAB 7201A Multi-Protocol Serial Communication Controller

- Two independent full-duplex serial channels
- Four independent DMA channels for transmitted/received data for both serial inputs/outputs
- Modem control signals
- Variable software-programmable data rate, up to 1.25 Mbaud at 5 MHz clock
- Double-buffered transmitter data and quadruple-buffered received data
- Programmable CRC algorithm
- Selection of interrupt, DMA or polling mode
- Asynchronous operation
  - character length: 5, 6, 7, or 8 bits
  - stop bits: 1, 1½, 2
  - clock frequency: x1, x16, x32 or x64 transmission speed
  - parity: odd, even, or disable
  - break generation and detection
  - interrupt on parity, overrun, or framing errors
- Programmable interrupt vectors and interrupt priorities
- Monosync, bisync, and external sync operations
  - software-selectable sync characters
  - automatic sync insertion
  - CRC generation and checking
- HDLC and SDLC operations
  - abort sequence generation and detection
  - automatic zero insertion and detection
  - address field recognition
  - CRC generation and checking
  - I-field residue handling
- High-performance MYMOS technology
- Single +5 V power supply; interfaces most microprocessors including SAB 8080, 8085, 8086, and others
- Single-phase TTL clock
- Available in plastic dual-in line packages

Pin Configuration



Pin Names

CLK	System Clock	DRQTxA	DMA Request, Transmit
RESET	Reset	DRQTxB	and Receive,
DCDA	Data Carrier Detect,	DRQRxA	Channel A and B
DCDB	Channel A and B	DRQRxB	
RxCA	Receiver Clock,	WAITA	Wait, Channel A and B
RxCB	Channel A and B	WAITB	
CTSA	Clear to Send,	D0-D7	Data Bus
CTSB	Channel A and B	WR	Write
TxCA	Transmit Clock,	RD	Read
TxCB	Channel A and B	CS	Chip Select
TxDA	Transmit Data,	C/D	Control/Data Select
TxDB	Channel A and B	B/A	Channel Select
RxDA	Receive Data,	HAI	Hold Acknowledge In
RxDB	Channel A and B	HAO	Hold Acknowledge Out
SYNCA	Synchronization,	DTRA	Data Terminal Ready,
SYNCB	Channel A and B	DTRB	Channel A and B
RTSA	Request to Send,	INT	Interrupt Request
RTSB	Channel A and B	INTA	Interrupt Acknowledge
		PRI	Interrupt Priority In
		PRO	Interrupt Priority Out

The Siemens SAB 7201A Multi-Protocol Serial Communication Controller (MPSC) is designed to interface high-speed communications lines using asynchronous, IBM bisync or HDLC/SDLC protocol. It can be interfaced with all Siemens micro-controllers, 8 and 16-bit microprocessors and the SAB 8237 DMA controller in polled, interrupt-driven, or DMA-driven modes of operation. The MPSC is a 40-pin device fabricated using Siemens high-performance MYMOS technology.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{TxCA}}$ $\overline{\text{TxCB}}$	7, 36	I	$\overline{\text{TRANSMITTER CLOCK}}$ The transmitter clock controls the rate at which data is shifted out from TxD. The MPSC may be programmed such that the clock rate is 1x, 16x, 32x or 64x the data rate. Data changes on the falling edge of $\overline{\text{TxC}}$. $\overline{\text{TxC}}$ features a Schmitt-trigger input for relaxed rise and fall time requirements (active low).
TxDA TxDB	8, 37	O	TRANSMIT DATA Serial data from the MPSC is output on these pins (marking high).
RxDA RxDB	9, 34	I	RECEIVE DATA Serial data to the MPSC is input on these pins (marking high).
$\overline{\text{SYNCA}}$ $\overline{\text{SYNCB}}$	10, 33	I/O	$\overline{\text{SYNCHRONIZATION}}$ The function of the sync pin depends on the MPSC operating mode. In asynchronous mode, sync is an input that can be read by the processor. Sync can be programmed to generate an interrupt in the same manner as $\overline{\text{DCD}}$ or $\overline{\text{CTS}}$. In external sync mode $\overline{\text{SYNC}}$ is also an input that informs the MPSC when synchronization has been achieved (see the timing waveforms for details). Once synchronization has been achieved, $\overline{\text{SYNC}}$ should be held low until synchronization is lost or a new message is about to start. In internal synchronization modes (monosync, bisync, HDLC/SDLC) $\overline{\text{SYNC}}$ is an output which is active each time a synchronization pattern is recognized. There is no qualifying logic associated with this function. Regardless of character boundaries, $\overline{\text{SYNC}}$ is active on any match (active low).
$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	10, 38	O	$\overline{\text{REQUEST TO SEND}}$ When the MPSC is operated in one of the synchronous modes, $\overline{\text{RTSA}}$ and $\overline{\text{RTSB}}$ are general-purpose outputs that may be set or reset with commands to the MPSC. In asynchronous mode, $\overline{\text{RTS}}$ becomes active as soon as it is programmed on. When programmed off, however, $\overline{\text{RTS}}$ remains active until the transmitter is completely empty. This feature simplifies programming which is required to perform modem control (active low).
DRQTxA DRQTxB DRQRxA DRQRxB	11, 29, 30, 32	O	DMA REQUEST When these lines are active, they indicate to a DMA controller that a transmitter or receiver is requesting DMA data transfer (active high).
$\overline{\text{WAITA}}$ $\overline{\text{WAITB}}$	11, 32	O	$\overline{\text{WAIT}}$ These outputs synchronize the processor with the MPSC when block transfer mode is used. It may be programmed to operate with either the receiver or transmitter, but not with both simultaneously. $\overline{\text{WAIT}}$ is normally inactive. But, for example, if the processor tries to perform an inappropriate data transfer, such as write to the transmitter when the transmitter buffer is full, the $\overline{\text{WAIT}}$ output for the channel is active until the MPSC is ready to accept data. The $\overline{\text{CS}}$, C/$\overline{\text{D}}$, B/$\overline{\text{A}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ inputs must remain stable while $\overline{\text{WAIT}}$ is active (open drain).

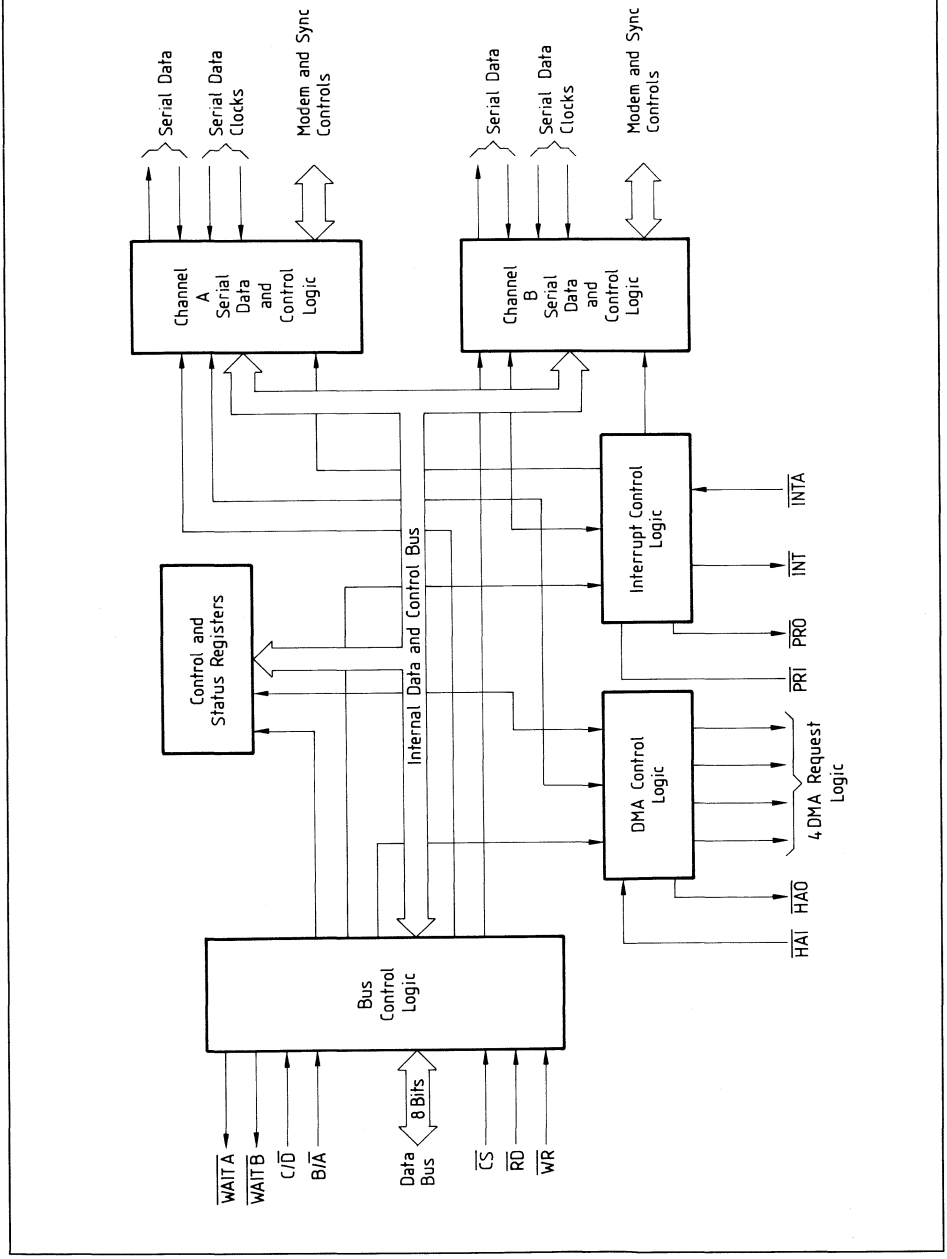
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
D0-D7	12–19	I/O	DATA BUS The data bus lines are connected to the system data bus. Data or status from the MPSC is output on these lines when $\overline{CS}$ and $\overline{RD}$ are active; data or commands are latched into the MPSC with the rising edge of $\overline{WR}$ when $\overline{CS}$ is active (tristate).
$\overline{WR}$	21	I	$\overline{WRITE}$ This input (with either $\overline{CS}$ during read cycle or $\overline{HAI}$ during DMA cycle) activates the MPSC to write data or control information to the device (active low).
$\overline{RD}$	22	I	$\overline{READ}$ This input (with either $\overline{CS}$ during read cycle or $\overline{HAI}$ during DMA cycle) activates the MPSC to read data or status from the device (active low).
$\overline{CS}$	23	I	$\overline{CHIP\ SELECT}$ Chip select allows the MPSC to transfer data or commands during a read or write cycle (active low).
C/$\overline{D}$	24	I	CONTROL/$\overline{DATA\ SELECT}$ This input, together with $\overline{RD}$, $\overline{WR}$ and B/$\overline{A}$, selects the data register (C/$\overline{D}$ = 0) or the control and status registers (C/$\overline{D}$ = 1) for access over the data bus.
B/$\overline{A}$	25	I	CHANNEL SELECT A low signal selects channel A and a high selects channel B for access during a read or write cycle.
$\overline{HAI}$	26	I	$\overline{HOLD\ ACKNOWLEDGE\ IN}$ This input informs the MPSC that the host processor has acknowledged the DMA request and has placed itself in the hold state. The MPSC then performs a DMA cycle for the highest-priorty outstanding DMA request, if there is any (active low).
$\overline{DTRA}$ $\overline{DTRB}$	26, 31	O	$\overline{DATA\ TERMINAL\ READY}$ The $\overline{DTR}$ pins are general-purpose outputs which may be set or reset with commands to the MPSC (active low).
$\overline{INTA}$	27	I	$\overline{INTERRUPT\ ACKNOWLEDGE}$ The processor generates two or three $\overline{INTA}$ pulses (depending on the processor type) to signal all peripheral devices that an interrupt acknowledge sequence takes place. During the interrupt acknowledge sequence, the MPSC, if programmed so, puts information on the data bus to vector the processor to the appropriate interrupt service location (active low).
$\overline{INT}$	28	O	$\overline{INTERRUPT\ REQUEST}$ $\overline{INT}$ is pulled low when an internal interrupt request is accepted (active low, open drain).

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{PRI}$	29	I	$\overline{INTERRUPT\ PRIORITY\ IN}$ This input informs the MPSC that the highest priority device is requesting interrupt. It is used with $\overline{PRO}$ to form a priority-resolution daisy chain when there is more than one interrupting device. The state of $\overline{PRI}$ and the programmed interrupt mode determine the MPSC's response to an interrupt acknowledge sequence (active low).
$\overline{PRO}$	30	O	$\overline{INTERRUPT\ PRIORITY\ OUT}$ This output is active when $\overline{HAI}$ is active and the MPSC is not requesting interrupt ($\overline{INT}$ is inactive). The active state informs the next lower priority device that there are no higher priority interrupt requests pending during an interrupt acknowledge sequence (active low).
$\overline{HAO}$	31	O	$\overline{HOLD\ ACKNOWLEDGE\ OUT}$ This output with $\overline{HAI}$ implements a priority daisy chain for multiple DMA devices. $\overline{HAO}$ is active when $\overline{HAI}$ is active and there are no DMA requests pending in the MPSC (active low).
VCC	40	–	POWER SUPPLY (+5 V)
GND	20	–	GROUND (0 V)

Block Diagram



Functional Description

The SAB 7201A is a dual-channel multi-protocol serial communication controller designed to satisfy a wide variety of serial data communications applications in computer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller and within that range it can be configured by system software so its features can be optimized for the individual application.

The SAB 7201A is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for other applications than data communications.

The SAB 7201A can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls on both channels. In applications where these controls are not needed the modem controls can be used for general-purpose I/O.

Programming the MPSC

Software operation of the MPSC is very straightforward. Its consistent register organization and high-level command structure help minimize the number of operations required to implement complex protocol designs. Programming is further simplified by the MPSC's extensive interrupt and status reporting capabilities. This section is divided into two parts.

Reset

When the SAB 7201A RESET line is activated, both MPSC channels enter the idle state. The serial output lines are forced to the marking state (high) and the modem interface signals ($\overline{RTS}$, $\overline{DTR}$) are forced high. In addition, the pointer registers are set to zero.

The MPSC Registers

The MPSC interfaces to the system software with a number of write and read registers associated with each channel. Commonly used commands and status bits are accessed directly through write and read register 0. Other functions are accessed indirectly with a register pointer to minimize the address space that must be dedicated to the MPSC.

Write Registers

Write Register	Function
0	Frequently used commands and register pointer control
1	Interrupt control
2	Processor/bus interface control
3	Receiver control
4	Mode control
5	Transmitter control
6	Sync/address character
7	Sync character

Read Registers

Read Register	Function
0	Buffer and "external/status" status
1	Received character error and special condition status
2	Interrupt vector (channel B only)
3	Tx length register, low byte
4	Tx length register, high byte

All write and read registers except RR2 are maintained separately for each channel. Write and read registers 2 are linked with the overall operation of the MPSC and have different meaning when addressed through different channels.

When initializing the MPSC, write register 2A (and 2B if desired) should be programmed first to establish the MPSC processor/bus interface mode. Each channel may then be programmed to being used separately, beginning with write register 4 to set the protocol mode for that channel. The remaining registers may then be programmed in any order.

Command/Status Description

The following command and status bytes are used during initialization and execution phases of operation. All command/status operations on the two channels are identical and independent, unless otherwise noted.

Detailed Register Description

Write Register 0 (WR0)

D7	D6	D5	D4	D3	D2	D1	D0
CRC Control Command		Command			Register Pointer		

D2,D1,D0 Register pointer

The register pointer determines which write register the next byte is to be written into, or which read register the next byte is to be read from. After a hardware or software reset the register pointer is set to zero. Therefore, the first control byte goes to write register 0. When the register pointer is set to a value other than zero the next control or status ($C/\overline{D} = 1$) access is to the specified register, afterwards the pointer is reset to zero. Other commands can freely be combined in write register 0 by setting the register pointer.

D5, D4, D3 Commands

Commands commonly used during the operation of the MPSC are grouped in write register 0. They include the following:

000 **Null**: This command has no effect and is used only to set the register pointer or issue a CRC command.

001 **Send abort**: When operating in the HDLC/SDLC mode this command causes the MPSC to transmit the HDLC/SDLC abort code, issuing 8 to 13 consecutive ones. Any data currently in the transmitter or transmitter buffer is destroyed. After sending the abort the transmitter reverts to the idle phase (flags). When using the Tx byte count-mode enable (D6 of WR1) and an underrun condition occurs, the SAB 7201A will automatically issue the 'send abort' command.

010 **Reset external/status interrupts**: When the external/status change flag is set, the conditions of bits D7 to D3 of read register 0 are latched to allow the capture of the short pulses that may occur. The "reset external/status interrupts" command reenables the latches so that new interrupts may be sensed.

011 **Channel reset**: This command has the same effect on a single channel as an external reset at pin 2. A 'channel reset' command to channel A resets the internal interrupt prioritization logic. This does not occur when a channel reset command is issued to channel B. All control registers associated with the channel to be reset must be reinitialized. After a channel reset, wait at least four system clock cycles before writing new commands or controls to that channel.

100 **Enable interrupt on next character**: When operating the MPSC in an interrupt-on-first-received-character mode this command may be issued at any time. It must be issued at the end of a message to reenable the interrupt logic for the next character received (the first character of the next message).

101 **Reset pending transmitter interrupt/DMA request**: A pending transmitter-buffer-becoming-empty interrupt or DMA request can be reset without sending another character by issuing this command (typically at the end of a message). A new transmitter-buffer-becoming-empty interrupt or DMA request is not performed until another character has been loaded and transferred to the transmitter shift register or when, if operating in the synchronous or HDLC/SDLC modes, the first CRC character has been sent.

110 **Error reset**: This command resets a special receive condition interrupt. It also reenables the parity and overrun error latches that allow errors at the end of a message to be checked.

111 **End of interrupt (channel A only)**: Once an interrupt request has been issued by the MPSC all lower priority internal and external interrupts in the daisy chain are held back to permit the current interrupt to be serviced while allowing higher priority interrupts to occur. At some point in the interrupt service routine (generally at the end), the 'end of interrupt' command must be issued to channel A to reenable the daisy chain and allow occurring of any pending lower priority internal interrupt requests. The EOI command must be sent to channel A for interrupts that occurred on either channel.

D7, D6 **CRC control commands**: The following commands control the operation of the CRC generator/checker logic.

00 **Null**: This command has no effect and is used when issuing other commands or setting the register pointer.

01 **Reset receiver CRC checker**: This command resets the CRC checker to zero when the channel is in a synchronous mode, and resets to all ones when in an HDLC/SDLC mode.

10 **Reset transmitter CRC generator**: This command resets the CRC generator to zero when the channel is in synchronous mode, and resets to all ones when in an HDLC/SDLC mode.

11 **Reset Tx underrun/EOM latch**: This command resets the Tx underrun/EOM latch, so when a transmitter underrun condition occurs (that means the transmitter has no more characters to send) the transmitter enters the CRC phase of operation and begins to send the 16-bit CRC character calculated up to that point. The latch is then set, so if the underrun condition persists, idle characters are sent following the CRC. After a hardware or software reset the latch is in the set state. This latch is automatically reset after the first character has been loaded into the Tx buffer in the HDLC/SDLC mode.

Write Register 1 (WR1)

D7	D6	D5	D4	D3	D2	D1	D0
Wait Function Enable	Tx Byte Count Mode Enable	Wait on Receiver/ Transmitter	Receiver Interrupt Mode		Condition Affects Vector	Transmitter Interrupt Enable	Ext./Status INT Enable

Tx Length Register (high and low)

D7	D6	D5	D4	D3	D2	D1	D0
Tx Length Register (low byte)							

D7	D6	D5	D4	D3	D2	D1	D0
Tx Length Register (high byte)							

D0 **External/status interrupt enable**: When this bit is set to one the MPSC issues an interrupt whenever any of the following conditions occurs:
- transition on the $\overline{DCD}$ input pin
- transition on the $\overline{CTS}$ input pin
- transition on the $\overline{SYNC}$ input pin
- entering or leaving synchronous hunt phase, break detection or termination
- HDLC/SDLC abort detection or termination
- idle/CRC latch becoming set (CRC being sent)
- after ending flag is sent in the HDLC/SDLC mode

D1 **Transmitter interrupt/DMA enable**: When this bit is set to one the MPSC issues an interrupt when:
1) The character currently in the transmitter buffer is transferred to the shift register (transmitter buffer becoming empty) or,
2) the transmitter enters the idle phase and begins transmitting sync or flag characters, or
3) the Tx byte count mode enable bit is set (WR1–D6=1). The SAB 7201A will automatically issue a Tx interrupt or DMA request when the transmitter becomes enabled (WR5–D3=1).

D2 **Status affects vector (programmed in channel B for both channels):** When this bit is set to zero the fixed vector programmed in WR2B during MPSC initialization is returned in an interrupt acknowledge sequence. When this bit is set to one the vector is modified to reflect the condition that caused the interrupt.

D4, D3 **Receiver interrupt mode:** This field controls how the MPSC's interrupt/DMA logic handles the "character received" condition.

00 **Receiver interrupts/DMA request disabled:** The MPSC does not issue an interrupt or a DMA request when a character has been received.

01 **Interrupt on first received character only:** In this mode the MPSC issues an interrupt only for the first character received after an "enable interrupt on next character" command (WR0) has been given. If the channel is in a DMA mode, a DMA request is issued for each character received including the first one. This mode generally is used whenever the MPSC is in a DMA or block transfer mode. This will signal the processor that the beginning of an incoming message has been received.

10 **Interrupt (and issue a DMA request) on all received characters:** In this mode an interrupt (and DMA request if the DMA mode is selected) is issued whenever there is a character present in the receiver buffer. A parity error is considered a special receive condition.

11 **Interrupt (and issue a DMA request) on all received characters:** This mode is the same as the one above except that a parity error is not considered a special receive condition. The following are considered special receive conditions:
- receiver overrun factor
- asynchronous framing error
- parity error (if specified)
- HDLC/SDLC end of message (final flag received)

D5 **Wait on receiver/transmitter:** If the wait function is enabled for block transfers, setting this bit to zero causes the MPSC to issue a wait ($\overline{\text{WAIT}}$ output goes low) when the processor attempts to write a character to the transmitter while the transmitter buffer is full. Setting this bit to one causes the MPSC to issue a wait when the processor attempts to read a character from the receiver while the receiver buffer is empty.

D6 **Tx byte count mode enable:** Each channel has a 16-bit Tx length register used for automatic transmit termination. When this bit is set to one the next two consecutive command cycle writes will be to the Tx length register. The first byte is loaded into the lower 8 bits and the second to the upper 8 bits of the Tx length register. The Tx length register holds the number of transfers to be performed by the transmitter. The Tx byte counter (RR3, RR4) is incremented each time a transfer is performed until the value of the Tx byte counter is equal to the value in the Tx length register. When equal, interrupts or DMA requests will be stopped until the Tx byte count enable bit is issued and a new byte count is loaded into the Tx length register. If a transmit underrun occurs in the HDLC/SDLC mode and the Tx byte counter is not equal to the Tx length register contents, the abort sequence will be sent automatically. Also, when using the Tx byte count mode, a transmit interrupt or DMA request will automatically become active after issuing the "Tx enable" command to WR5.
The Tx byte count mode can be cleared by either a channel reset command or a hardware reset.

D7 **Wait function enable:** Setting this bit to one enables the wait function which is described in WR1.

Write Register 2, Channel A (WR2A)

D7	D6	D5	D4	D3	D2	D1	D0
Pin 10 $\overline{\text{SYNCB}}$/ RTSB	RxINT Mask	Interrupt Vector Mode			Priority	DMA Mode Select	

D1, D0 **DMA mode select:** Setting this field determines whether channel A or B is used in a DMA mode (i.e. data transfers are performed by a DMA controller) or in a non-DMA mode where transfers are performed by the processor in either a polled, interrupt, or block transfer mode. The functions of some MPSC pins are also controlled by this field.

D2 **Priority:** This bit selects the relative priorities of the various interrupt and DMA conditions according to the application requirements.

D2 D1 D0	INT/DMA Mode Channel A	INT/DMA Mode Channel B	Pin Function $\overline{\text{WAITA}}$/DRQRxA $\overline{\text{WAITB}}$/DRQTxA		Pin Function $\overline{\text{PRI}}$/DRQRxB $\overline{\text{PRO}}$/DRQTxB		Pin Function $\overline{\text{DTRB}}$/$\overline{\text{HAI}}$ $\overline{\text{DTRA}}$/$\overline{\text{HAO}}$		Priority High ... Low
0 0 0	INT	INT	$\overline{\text{WAITA}}$	$\overline{\text{WAITB}}$	$\overline{\text{PRI}}$	$\overline{\text{PRO}}$	$\overline{\text{DTRB}}$	$\overline{\text{DTRA}}$	RxA TxA RxB TxB E/SA E/SB
1 0 0	INT	INT							RxA RxB TxA TxB E/SA E/SB
X 0 1	DMA		DRQRxA	DRQTxA	$\overline{\text{PRI}}$	$\overline{\text{PRO}}$	$\overline{\text{HAI}}$	$\overline{\text{HAO}}$	RxA TxA
		INT							RxA* RxB TxB E/SA* E/SB
0 1 0	DMA	DMA	DRQRxA	DRQTxA	DRQRxB	DRQTxB	$\overline{\text{HAI}}$	$\overline{\text{HAO}}$	RxA TxA RxB TxB
									RxA* RxB* E/SA* E/SB*
1 1 0	DMA	DMA							RxA RxB TxA TxB
									RxA* RxB* E/SA* E/SB*
X 1 1	DMA	DMA					$\overline{\text{DTRB}}$	$\overline{\text{DTRA}}$	No Priority
									RxA* RxB* E/SA* E/SB*

*) The E/S interrupt and Rx interrupt may occur in DMA.

D5 to D3 **Interrupt vector mode:** This field determines how the MPSC responds to an interrupt acknowledge sequence from the processor.

Interrupt Acknowledge Sequence Response

	Mode	Read Register 2B and Interrupt Vector Bits Affected when Condition-Affects-Vector Is Enabled
000	Nonvectored	D4 D3 D2
001	Nonvectored	D4 D3 D2
010	Nonvectored	D2 D1 D0
011	Illegal	–
100	8085 Master	D4 D3 D2
101	8085 Slave	D4 D3 D2
110	8086	D2 D1 D0
111	8085/8259A Slave	D4 D3 D2

D6 **RxINT mask:** This option is generally used in the DMA modes. Enabling this bit inhibits the interrupt from occurring when mode "interrupt/DMA request on first received character" is selected. In other words, only a DMA request will be generated when the first character is received.

D7 **Pin 10 $\overline{\text{SYNCB}}$/$\overline{\text{RTSB}}$ select:** Programming a zero into this bit selects $\overline{\text{RTSB}}$ as the function of pin 10. A one selects $\overline{\text{SYNCB}}$.

Write Register 2, Channel B (WR2B)

D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Vector							

D7 to D0 **Interrupt vector:** When the MPSC is used in the vectored interrupt mode the contents of this register is put on the bus during the appropriate portion of the interrupt acknowledge sequence. Its value is modified if status-affects-vector is enabled. The value of RR2B can be read at any time. This feature is particularly useful for determining the cause of an interrupt when the MPSC is used in a nonvectored interrupt mode.

Write Register 3 (WR3)

D7	D6	D5	D4	D3	D2	D1	D0
Number of Received Bits per Character		Auto-Enable	Enter Hunt Phase	Receiver CRC Enable	Address Search Mode	Sync Character Load Inhibit	Receiver Enable

D0 **Receiver enable:** After the channel has been completely initialized, setting this bit to one allows the receiver to begin operation. This bit may be set to zero at any time to disable the receiver.

D1 **Sync character load inhibit:** In the character synchronous modes, this bit inhibits the transfer of sync characters to the receiver buffer thus performing a "sync-stripping" operation. When using the MPSC's CRC checking ability this feature should be used only to strip leading sync characters preceding a message, since the load inhibit does not exclude sync characters embedded in the message from the CRC calculation. Synchronous protocols using other types of block checking such as checksum or LRC are free to strip embedded sync characters with this bit.

D2 **Address search mode:** In the HDLC/SDLC mode, setting this bit places the MPSC in an address search mode. Character assembly does not begin until the 8-bit character (secondary address field) following the starting flag of a message matches either the address programmed into WR6 or the global adress 1111 1111.

D3 **Receiver CRC enable:** This bit enables (=1) and disables (=0) the CRC checker in the COP mode, allowing characters from the CRC calculation to be selectively included or excluded. The MPSC features a one-character delay between the receiver shift register and the CRC checker so that the enabling or disabling takes place at the same time the last character is transferred from the shift register to the receiver buffer. Therefore, there is one full character time in which to read the character and decide whether or not it should be included in the CRC calculation. In the HDLC/SDLC mode, there is no 8-bit delay.

D4 **Enter hunt phase:** Although the MPSC receiver automatically enters the sync hunt phase after a reset, there are times when reentry may be desired, such as when it has been determined that synchronization has been lost or – in an HDLC/SDLC mode – to ignore the current incoming message. Writing a one into this bit at any time after initialization causes the MPSC to reenter the hunt phase.

D5 **Auto-enable:** Setting this bit to one causes the DCD and CTS inputs to act as enable inputs to the receiver and transmitter, respectively.

D7, D6 **Number of received bits per character:** This field specifies the number of data bits assembled to form each character. The value may be changed on the fly while a character is being assembled and, if the change is made before reaching the new number of bits, it will affect that character. Otherwise the new specifications have effect on the next character received.

Received bits per character

00	Receive 5 data bits/character
01	Receive 7 data bits/character
10	Receive 6 data bits/character
11	Receive 8 data bits/character

Write Register 4 (WR4)

D7	D6	D5	D4	D3	D2	D1	D0
Clock Rate		Sync Mode		Number of Stop Bits per Sync Mode		Parity Even/Odd	Parity Enable

D0 **Parity enable:** Setting this bit to one adds an extra data bit containing parity information to each transmitted character. Each received character is expected to contain this extra bit and the receiver parity checker is enabled.

D1 **Parity even/odd:** Programming a zero into this bit when parity is enabled causes the transmitted parity bit to take on the value required for odd parity. The received character is checked for odd parity. Conversely, a one in this bit signifies even parity generation and checking.

D3, D2 **Number of stop bits per sync mode:** This field specifies whether the channel is used in a synchronous (HDLC/SDLC) or an asynchronous mode. In an asynchronous mode this field also specifies the number of bit times used as the stop bit length by the transmitter. The receiver always checks for one stop bit.

Stop bits

00 Synchronous modes
01 Asynchronous 1-bit time (1 stop bit)
10 Asynchronous 1½ bit time (1½ stop bits)
11 Asynchronous 2-bit time (2 stop bits)

D5, D4 **Sync mode:** When the stop bits/sync mode field is programmed for synchronous modes (D2, D3 = 00), this field specifies the particular synchronous format to be used. This field is ignored in an asynchronous mode.

Synchronous formats

00 8-bit internal synchronization character (monosync)
01 16-bit internal synchronization character (bisync)
10 HDLC/SDLC
11 External synchronization (SYNC pin becomes an input)

D7, D6 **Clock rate:** This field specifies the relationship between the transmitter and receiver clock inputs ($\overline{TxC}$, $\overline{RxC}$) and the actual data rates at TxD and RxD. When operating in a synchronous mode a 1x clock rate must be specified. In asynchronous modes any of the rates may be specified, however, with a 1x clock rate the receiver cannot determine the center of the start bit. In this mode, the sampling (rising) edge of $\overline{RxC}$ must be externally synchronized with the data.

Clock rates

00 Clock rate = 1x data rate
01 Clock rate = 16x data rate
10 Clock rate = 32x data rate
11 Clock rate = 64x data rate

Write Register 5 (WR5)

D7	D6	D5	D4	D3	D2	D1	D0
DTR	Number of Bits Transmitted per Character		Send Break	Transmitter Enable	CRC Polynomial Select	$\overline{RTS}$	Transmitter CRC Enable

D0 **Transmitter CRC enable:** A one or a zero enables or disables respectively, the CRC generator calculation. The enable or disable does not take place until the next character is transferred from the transmitter buffer to the shift register, thus allowing specific characters to be included or excluded from the CRC calculation. By setting or resetting this bit just before loading the next character, this and subsequent characters are included or excluded from the calculation. If this bit is zero when the transmitter becomes empty, the MPSC goes to the idle phase regardless of the state of the idle/CRC latch.

D1 $\overline{RTS}$: In synchronous and HDLC/SDLC modes setting this bit to one causes the $\overline{RTS}$ pin to go low while a zero causes it to go high. In an asynchronous mode setting this bit to zero does not cause $\overline{RTS}$ to go high until the transmitter is completely empty. This feature facilitates programming the MPSC for use with asynchronous modems.

D2 **CRC polynomial select:** This bit selects the polynomial used by the transmitter and receiver for CRC generation and checking. A one selects the CRC 16 polynomial ($x^{16}+x^{15}+x^2+1$). A zero selects the CRC CCITT polynomial ($x^{16}+x^{12}+x^5+1$). In HDLC/SDLC mode, CRC CCITT must be selected. Either polynomial may be used in other synchronous modes.

D3 **Transmitter enable:** After a reset the transmitted data output (TxD) is held high (marking) and the transmitter is disabled until this bit is set. In an asynchronous mode TxD remains high until data is loaded for transmission. In synchronous and HDLC/SDLC modes the MPSC automatically enters the idle phase and sends the programmed sync or flag characters.

When the transmitter is disabled in an asynchronous mode any character currently being sent is completed before TxD returns to the marking state.
If the transmitter is disabled during the data phase in a synchronous mode the current character is sent. TxD then goes high (marking). In HDLC/SDLC mode the current character is sent, but the marking line following is zero-inserted. That is, the line goes low for one bit time out of every five.
The transmitter should never be disabled during the HDLC/SDLC data phase unless a reset is to follow immediately. In either case, any character in the buffer register is held.
Disabling the transmitter during the CRC phase causes the remainder of the CRC character to be bit-substituted with the sync (or flag). The total number of bits transmitted is correct and TxD goes high after they are sent.
If the transmitter is disabled during the idle phase the remainder of the sync (flag) character is sent. TxD then goes high.

D4 **Send break:** Setting this bit to one immediately forces the transmitter output (TxD) low (spacing). This function overrides the normal transmitter output and destroys any data being transmitted although the transmitter is still in operation. Resetting this bit releases the transmitter output.

D6, D5 **Transmitted bits per character:** This field controls the number of data bits transmitted in each character. The number of bits per character may be changed by rewriting this field just before the first character is loaded to use the new specification.

Transmitted Bits per Character

Transmitted Bits per Character 1	Transmitted Bits per Character	
D6	D5	Bits per Character
0	0	5 or Less (see below)
0	1	7
1	0	6
1	1	8

Normally each character is sent to the MPSC right-justified and the unused bits are ignored. However, when sending five bits or less the data should be formatted as shown below to inform the MPSC about the precise number of bits to be sent.

Transmitted Bits per Character for 5 Bits or Less

D7	D6	D5	D4	D3	D2	D1	D0	Number of Bits per Character
1	1	1	1	0	0	0	D0	1
1	1	1	0	0	0	D1	D0	2
1	1	0	0	0	D2	D1	D0	3
1	0	0	0	D3	D2	D1	D0	4
0	0	0	D4	D3	D2	D1	D0	5

D7 **$\overline{\text{DTR}}$ (data terminal ready):** When this bit is one the $\overline{\text{DTR}}$ output is low (active). Conversely, when this bit is zero DTR is high.

Write Register 6 (WR6)

D7	D6	D5	D4	D3	D2	D1	D0
Sync Byte 1							

D7 to D0 Sync byte 1

Sync byte 1 is used in the following modes:

Monosync 8-bit sync character transmitted during the idle phase.
Bisync Least significant (first) 8 bits of the 16-bit transmit and receive sync character.
External sync Sync character transmitted during the idle phase.
HDLC/SDLC Secondary address value matched to secondary address field of the HDLC/SDLC frame when the MPSC is in the address search mode.

Write Register 7 (WR7)

D7	D6	D5	D4	D3	D2	D1	D0
Sync Byte 2							

D7 to D0 Sync byte 2

Sync byte 2 is used in the following modes:

Monosync 8-bit sync character matched by the receiver.
Bisync Most significant (second) 8 bits of the 16-bit transmit and receive sync characters.
HDLC/SDLC The flag character, 0111 1110, must be programmed into control register 7 for flag matching by the MPSC receiver.

Read Register 0 (RR0)

D7	D6	D5	D4	D3	D2	D1	D0
Break/ Abort	Tx Underrun /EOM	CTS	Sync Status	DCD	Transmitter Buffer Empty	Interrupt Pending	Received Character Available

D0 **Received character available:** When this bit is set it indicates that one or more characters in the receiver buffer are available for the processor to read. Once all the available characters have been read the MPSC resets this bit until a new character is received.

D1 **Interrupt pending (channel A only):** The interrupt pending bit is used with the interrupt vector register (read register 2) to make it easier to determine the MPSC's interrupt status, particularly in a nonvectored interrupt mode where the processor must poll each device to determine the interrupt source. In this mode interrupt pending is set when read register is read, the $\overline{PRI}$ input is active (low), and the MPSC is requesting interrupt service.
The status registers of both channels need not be analyzed to determine if an interrupt is pending. If the status-affects-vector is enabled and the interrupt pending is set, the vector read from RR2 contains valid condition information.

In a vectored interrupt mode, interrupt pending is set during the interrupt acknowledge cycle (on the leading edge of the second $\overline{INTA}$ pulse) when the MPSC is the highest priority device requesting interrupt service ($\overline{PRI}$ is active). In either mode, if there are no other pending interrupt requests, interrupt pending is reset when the end of the interrupt command is issued.

D2 **Transmitter buffer empty:** This bit is set whenever the transmitter buffer is empty except during the transmission of CRC. (The MPSC uses the buffer to facilitate this function.) After a reset the buffer is considered empty and transmit buffer empty is set.

D7 to D3 **External/status flags:** The following status bits reflect the state of the various conditions that cause an external/status interrupt. The MPSC latches all external/status bits whenever a change occurs that would cause an external/status interrupt (regardless of whether this interrupt is enabled). This allows transient status changes on these lines to be captured with relaxed software timing requirements.
When the MPSC is operated in an interrupt-driven mode for external/status interrupts, read register 0 should be read when this interrupt occurs and a "reset external/status interrupt" command issued to reenable the interrupt and the latches. To poll these bits without interrupts, the "reset external/status interrupt" command can be issued to first update the status to reflect the current values.

D3 $\overline{DCD}$: This bit reflects the inverted state of the $\overline{DCD}$ input. When $\overline{DCD}$ is low the DCD status bit is high. Any transition on this bit causes an external/status interrupt request.

D4 **Sync status:** The meaning of this bit depends on the operating mode of the MPSC.

Asynchronous mode: Sync status reflects the inverted state of the $\overline{SYNC}$ input. When $\overline{SYNC}$ is low, sync status is high. Any transition on this bit causes an external/status interrupt request.

External synchronization mode: Sync status operates in the same manner as in asynchronous mode. The MPSC's receiver synchronization logic is also tied to the sync status bit in external synchronization mode and a low-to-high transition ($\overline{SYNC}$ input going low) informs the receiver that synchronization has been achieved and character assembly begins.
A low-to-high transition on the $\overline{SYNC}$ input indicates that synchronization has been lost and is reflected both in the sync status becoming zero and the generation of an external/status interrupt. The receiver remains in the receive data phase until the enter hunt phase bit in write register 3 is set.

Monosync, bisync, HDLC/SDLC modes: In these modes, sync status indicates whether the MPSC receiver is in the sync hunt or receive data phase of operation. A zero indicates that the MPSC is in the receive data phase and a one indicates that the MPSC is in the sync hunt phase (as after a reset or a setting of the enter sync hunt phase bit). Like in the other modes a transition on this bit causes an external/status interrupt to be issued. It should be noted that entering a sync hunt phase after either a reset or when programmed causes an external/status interrupt request which may be cleared immediately with a "reset external/ status interrupt" command.

D5 **CTS:** This bit reflects the inverted state of the $\overline{CTS}$ input. When $\overline{CTS}$ is low, the CTS status bit is high. Any transition on this bit causes an external/status interrupt request.

D6 **Tx underrun/EOM:** This bit indicates the state of the Tx underrun/EOM latch used in the synchronous and HDLC/SDLC modes. After a hardware reset this bit is set to one, indicating that the transmitter is completely empty. When the MPSC enters idle phase it automatically transmits sync or flag characters. In the HDLC/SDLC mode the MPSC automatically resets this latch after the first byte of a frame is written to the Tx buffer. When the transmitter is completely empty, the MPSC sends the 16-bit CRC character and sets the latch again. An external/status interrupt is issued when the latch is set, indicating that CRC is being sent. No interrupt is issued when the latch is reset.

Break/abort: In the asynchronous mode this bit indicates the detection of a break sequence (a null character plus framing error that occurs when the RxD input is held low, spacing, for more than one character time). Break/abort is reset when RxD returns high (marking).
In the HDLC/SDLC mode, break/abort indicates the detection of an abort sequence when seven or more ones are received in sequence. It is reset when a zero is received.
Any transition of the break/abort bit causes an external/status interrupt.

Read Register 1 (RR1)

D7	D6	D5	D4	D3	D2	D1	D0
End of HDLC/ SDLC Frame	CRC Framing Error	Overrun Error	Parity Error	HDLC/SDLC Residue Code			All Sent

D0 **All sent:** This bit is set when the transmitter is empty and reset when a character is present in the transmitter buffer or shift register. This feature simplifies the modem control software routines. In the bit-synchronous mode, this bit will be set when the ending flag pattern is sent.

D3 to D1 **HDLC/SDLC residue code:** Since the data portion of an HDLC/SDLC message can consist of any number of bits and not necessarily an integral number of characters, the MPSC features special logic to determine and report when the end of frame flag has been received, the boundary between the data field and the CRC character in the last few data characters that were just read.

When the end of frame condition is indicated, that is, read register 1D7 = 1 and special receive condition interrupt (if enabled), the last bits of the CRC character are in the receiver buffer. The residue code for the frame is valid in the read register 1 byte associated with that data character (RR1 tracks the received data in its own buffer).
The meaning of the residue code depends upon the number of bits per character specified for the receiver. The previous character refers to the last character read before the end of frame, and so forth.

Residue Codes

8 Bits per Character

D_3	D_2	D_1	Previous Character	2nd Previous Character	
1	0	0	C C C C C C C C	C C C C C D D D	
0	1	0	C C C C C C C C	C C C C D D D D	
1	1	0	C C C C C C C C	C C C D D D D D	
0	0	1	C C C C C C C C	C C D D D D D D	
1	0	1	C C C C C C C C	C D D D D D D D	
0	1	1	C C C C C C C C	D D D D D D D D	(no residue)
1	1	1	C C C C C C C D	D D D D D D D D	
0	0	0	C C C C C C D D	D D D D D D D D	

7 Bits per Character

D_3	D_2	D_1	Previous Character	2nd Previous Character	
1	0	0	C C C C C C C	C C C C C D D	
0	1	0	C C C C C C C	C C C C D D D	
1	1	0	C C C C C C C	C C C D D D D	
0	0	1	C C C C C C C	C C D D D D D	
1	0	1	C C C C C C C	C D D D D D D	
0	1	1	C C C C C C C	D D D D D D D	(no residue)
0	0	0	C C C C C C D	D D D D D D D	

6 Bits per Character

D_3	D_2	D_1	Previous Character	2nd Previous Character	
1	0	0	C C C C C C	C C C C C D	
0	1	0	C C C C C C	C C C C D D	
1	1	0	C C C C C C	C C C D D D	
0	0	1	C C C C C C	C C D D D D	
1	0	1	C C C C C C	C D D D D D	
0	0	0	C C C C C C	D D D D D D	(no residue)

5 Bits per Character

D_3	D_2	D_1	2nd Previous Character	3rd Previous Character	
1	0	0	C C C C C	D D D D D	(no residue)
0	1	0	C C C C D	D D D D D	
1	1	0	C C C D D	D D D D D	
0	0	1	C C D D D	D D D D D	
0	0	0	C D D D D	D D D D D	

Special receive condition flags

The status bits described in the following – parity error (if parity as a special receive condition is enabled), receiver overrun error CRC/framing error, and end of HDLC/SDLC frame – all represent special receive conditions.

When any of these conditions occur and interrupts are enabled, the MPSC issues an interrupt request. In addition, if a condition-affects-vector mode is enabled, the vector generated (and the contents of RR2B for nonvectored interrupts) is different from that of a received-character-available condition. Thus, it is not necessary to analyze RR1 with each character to determine if an error has occurred.

As a further convenience, the parity error and receiver overrun error flags are latched. That is, once one of these errors occurs, the flag remains set for all subsequent characters until reset by the error reset command. With this facility RR1 need only be read at the end of a message to determine if either of these errors occurred anywhere in the message. The other flags are not latched and follow each character available in the receiver buffer.

D4 **Parity error**: This bit is set and latched when parity is enabled and the received parity bit does not match the sense (odd or even) calculated from the data bits.

D5 **Receiver overrun error**: This error occurs and is latched when the receiver buffer already contains three characters and a fourth character is completely received, overwriting the last character in the buffer.

D6 **CRC/framing error**: In the asynchronous mode a framing error is flagged (but not latched) when no stop bit is detected at the end of a character (i.e. RxD is low one bit time after the center of the last data or parity bit). When this condition occurs, the MPSC waits an additional one-half bit time before sampling again so that the framing error is not interpreted as a new start bit.
In the synchronous and HDLC/SDLC modes this bit indicates the result of the comparison between the current CRC result and the appropriate check value and is usually set to one since a message rarely indicates a correct CRC result until correctly completed with the CRC check character. Note that a CRC error does not result in a special receive condition interrupt.

D7 **End of HDLC/SDLC frame (EOF)**: This status bit is used only in the bit synchronous mode to indicate that the end of frame flag has been received and that the CRC error flag and residue code are valid. This flag can be reset at any time by issuing an error reset command. The MPSC also automatically resets this bit when the first character of the next message frame is sent.

Read Register 2B (RR2B)

D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Vector							

D7 to D0 **Interrupt vector (channel B only)**: Reading read register 2B returns the interrupt vector that is programmed into write register 2B. If a condition-affects-vector mode is enabled the value of the vector is modified as shown in the following table.

Status-Affects-Vector Modifications

Interrupt Pending (RR0, D1 Channel A)	8085 Modes / 8086 Modes	D4 / D2	D3 / D1	D2 / D0	Condition
0		1	1	1	No Interrupt Pending
1		0	0	0	Channel B Transmitter Buffer Empty
1		0	0	1	Channel B External/Status Change
1		0	1	0	Channel B Received Character Available
1		0	1	1	Channel B Special Receive Condition
1		1	0	0	Channel A Transmitter Buffer Empty
1		1	0	1	Channel A External/Status Change
1		1	1	0	Channel A Received Character Available
1		1	1	1	Channel A Special Receive Condition

As can be seen code 111 can mean either channel A special receive condition or no interrupt pending. They can be easily distinguished by examining the interrupt pending bit (D1) of read register 0, channel A. In a nonvectored interrupt mode the vector register must be read first for the interrupt pending to be valid.

Read Registers 3 and 4 (RR3, RR4)
Tx Byte Counter (low byte RR3, high byte RR4)

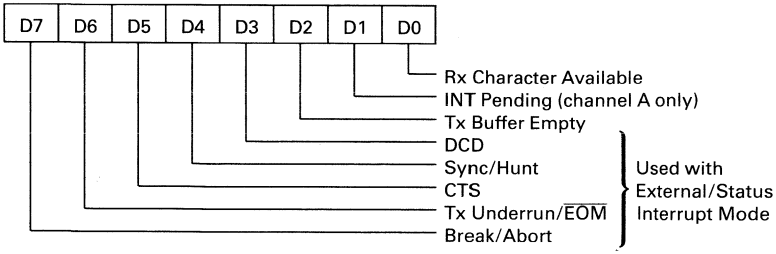
D7	D6	D5	D4	D3	D2	D1	D0
Tx Byte Counter (low byte)							

D7	D6	D5	D4	D3	D2	D1	D0
Tx Byte Counter (high byte)							

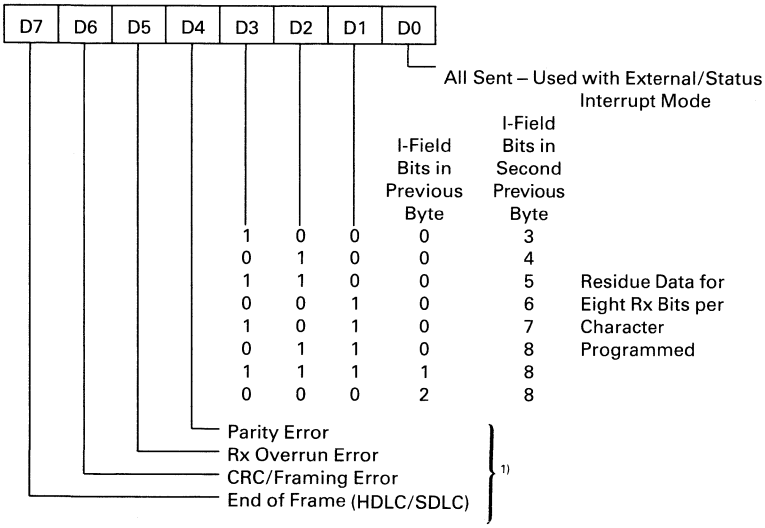
These two registers are used to count the number of transmit data. They can be used when data transmission is performed in the Tx byte count enable mode (i.e., when bit D6 of WR1 is 1). The values of the counters are cleared when the system is reset, when the contents of the Tx length registers (addressed via WR1) coincide with those of RR3, RR4 or when Tx length registers are set by setting bit D6 of the WR1 to 1.

Read Register Bit Functions

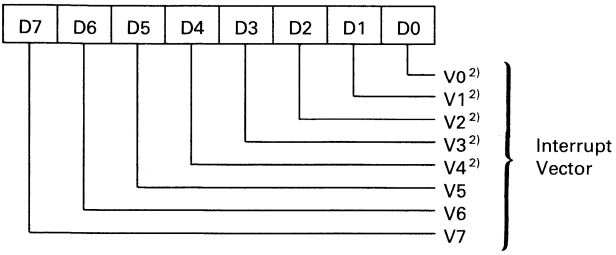
Read register 0



Read register 1

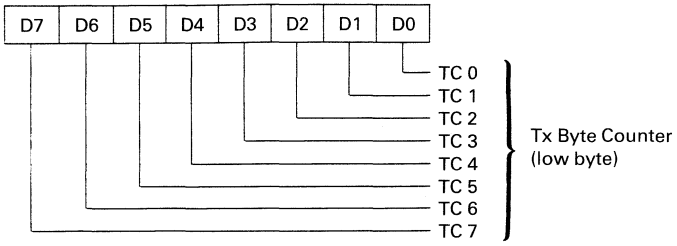


Read register 2 (channel B only)

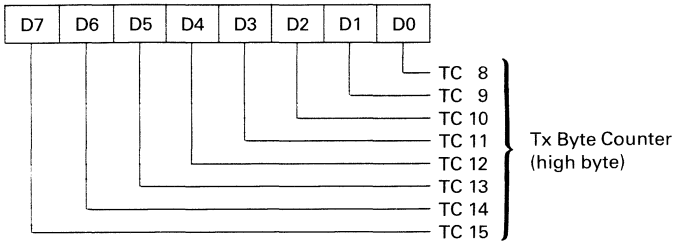


1) Used with special receive condition mode.
2) Variable if status-affects-vector is programmed.

Read register 3



Read register 4

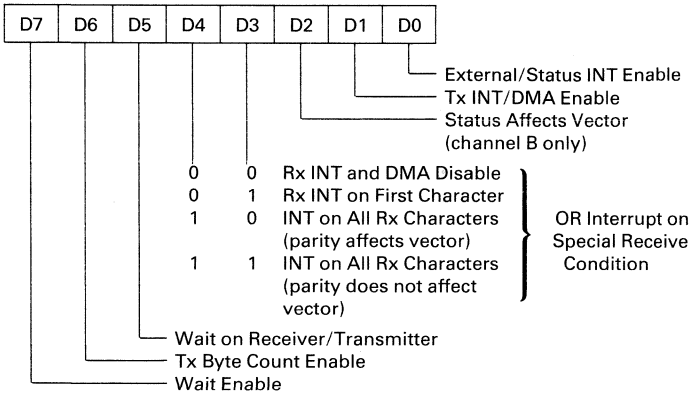


Write Register Bit Functions

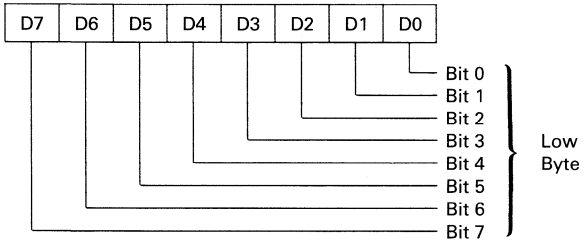
Write register 0

D7	D6	D5	D4	D3	D2	D1	D0		
					0	0	0	Register 0	Pointer for the Selection of a Read/Write Register
					0	0	1	Register 1	
					0	1	0	Register 2	
					0	1	1	Register 3	
					1	0	0	Register 4	
					1	0	1	Register 5	
					1	1	0	Register 6	
					1	1	1	Register 7	
		0	0	0	Null Code				
		0	0	1	Send Abort (HDLC/SDLC)				
		0	1	0	Reset External/Status INT				
		0	1	1	Channel Reset				
		1	0	0	Enable INT on Next Rx Character				
		1	0	1	Reset Tx INT/DMA Pending				
		1	1	0	Error Reset				
		1	1	1	End of Interrupt (EOI – channel A only)				
0	0	Null Code							
0	1	Reset Rx CRC Checker							
1	0	Reset Tx CRC Generator							
1	1	Reset Tx Underrun/EOM Latch							

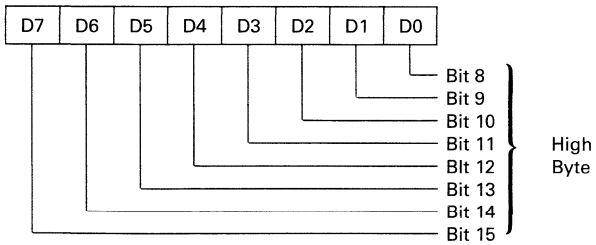
Write register 1



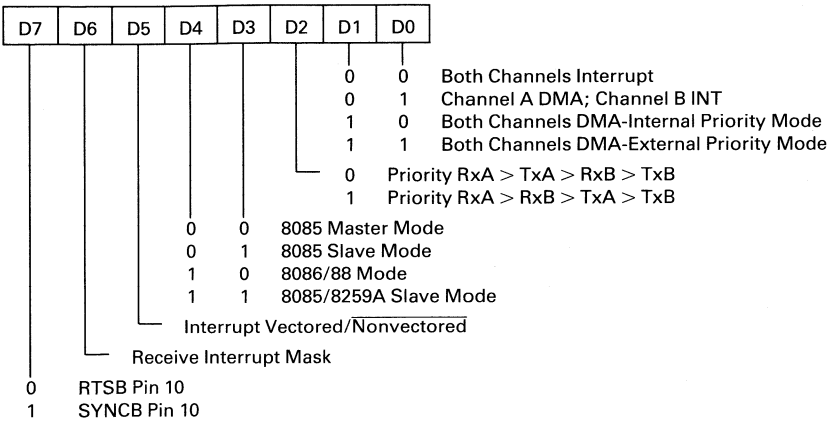
Tx length register



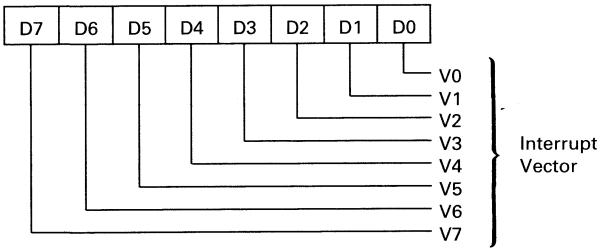
Tx length register



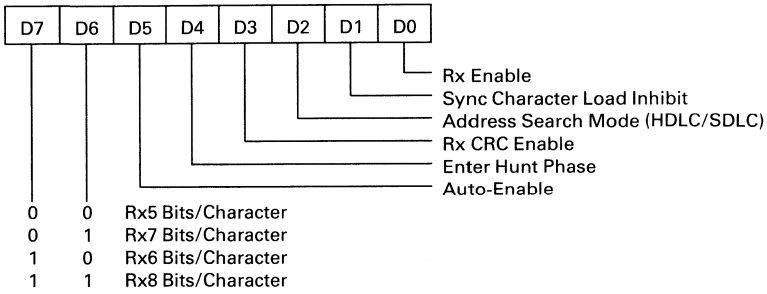
Write register 2 (channel A)



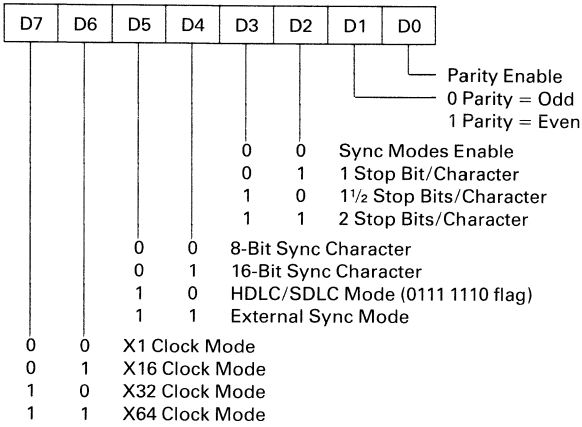
Write register 2 (channel B)



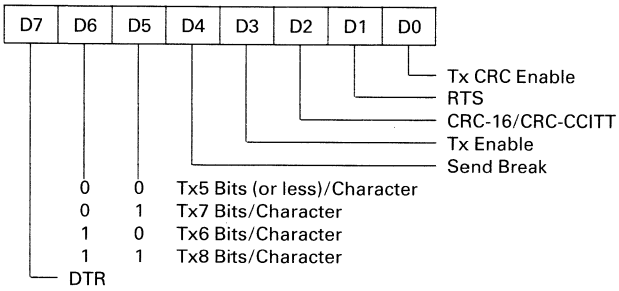
Write register 3



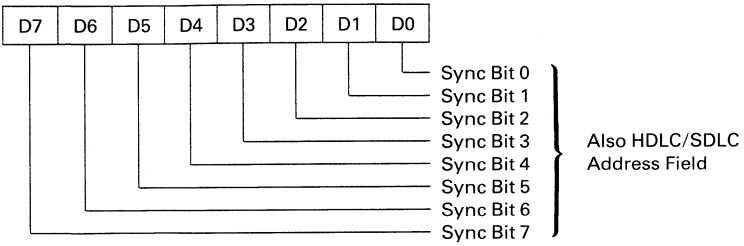
Write register 4



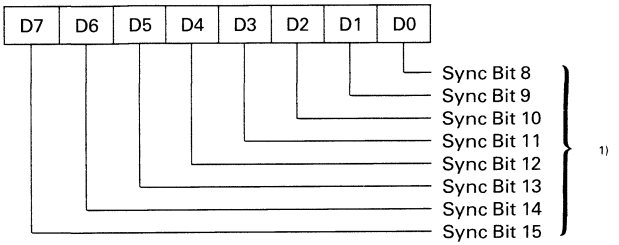
Write register 5



Write register 6



Write register 7



[1] For HDLC/SDLC it must be programmed to 0111 1110 for flag recognition.

Absolute Maximum Ratings [1)]

Temperature under bias	0 to + 70°C
Storage temperature	−65 to +150°C
All output and supply voltages	−0.5 to + 7V
All input voltages	−0.5 to + 7V
Power dissipation	1.0W

DC Characteristics

(TA = 0 to 70°C, VCC = 5V ±10%)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
VIL	Input low voltage	−0.5	0.8	V	–
VIH	Input high voltage	2.0	VCC+0.5V	V	–
VOL	Output low voltage	–	0.45	V	IOL = 2.0 mA
VOH	Output high voltage	2.4	–	V	IOH = −200 µA
IIL	Input load current	–	±10	µA	VIN = VCC to 0V
IOFL	Output float leakage	–	±10	µA	VOUT = VCC to 0V
ICC	VCC supply current	–	200	mA	–

Capacitance

(TA = 25°C, VCC = GND = 0V)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
CIN	Input capacitance	–	10	pF	fc = 1 MHz
COUT	Output capacitance	–	15	pF	Unmeasured pins returned to GND
CIO	I/O capacitance	–	20	pF	

[1)] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

(TA = 0 to 70°C, VCC = +5V ±10%)

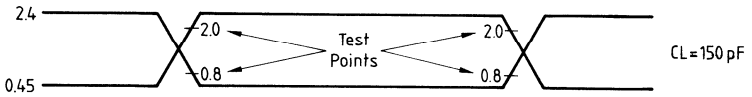
Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCY	Clock cycle	200	4000	ns	–
TCH	Clock pulse width high	70	2000	ns	–
TCL	Clock pulse width low	70	2000	ns	–
TR	Clock rise time	0	30	ns	–
TF	Clock fall time	0	30	ns	–
TAR	Address setup time to $\overline{RD}$	0	–	ns	–
TRA	Address hold time from $\overline{RD}$	0	–	ns	–
TRR	$\overline{RD}$ pulse width	200	–	ns	–
TAD	Data output delay from address	–	200	ns	–
TRD	Data output delay from $\overline{RD}$	–	200	ns	–
TDF	Data float delay from $\overline{RD}$	10	100	ns	–
TAW	Address setup time to $\overline{WR}$	0	–	ns	–
TWA	Address hold time from $\overline{WR}$	0	–	ns	–
TWW	$\overline{WR}$ pulse width	200	–	ns	–
TDW	Data setup time to $\overline{WR}$	130	–	ns	–
TWD	Data hold time from $\overline{WR}$	0	–	ns	–
TPIPO	$\overline{PRO}$ delay time from $\overline{PRI}$	–	100	ns	–
TIAPO	$\overline{PRO}$ delay time from $\overline{INTA}$	–	200	ns	–
TPIIA	$\overline{PRI}$ setup time to $\overline{INTA}$	0	–	ns	–
TIAPI	$\overline{PRI}$ hold time from $\overline{INTA}$	20	–	ns	–
TIAIA	$\overline{INTA}$ pulse width	200	–	ns	–
TIAD	Data output delay from $\overline{INTA}$	–	200	ns	–
TDF	Data float delay from $\overline{INTA}$	10	100	ns	–
TCQ	DRQ hold time from $\overline{RD}$, $\overline{WR}$	–	150	ns	–
THIC	$\overline{HAI}$ setup time to $\overline{RD}$, $\overline{WR}$	300	–	ns	–
TCHI	$\overline{HAI}$ hold time from $\overline{RD}$, $\overline{WR}$	0	–	ns	–
THIHO	$\overline{HAO}$ delay time from $\overline{HAI}$	–	100	ns	–
TDCY	Data clock cycle	400	–	ns	$\overline{RxC}$, $\overline{TxC}$
TDCH	Data clock pulse width high	180	–	ns	$\overline{RxC}$, $\overline{TxC}$
TDCL	Data clock pulse width low	180	–	ns	$\overline{RxC}$, $\overline{TxC}$

AC Characteristics (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TTCTD	Tx data delay time from TxC	–	300	ns	x1 mode
		–	1000	ns	x16, x32, x64 mode
TRDRC	Rx data setup time to $\overline{RxC}$	0	–	ns	–
TRCRD	Rx data hold time from $\overline{RxC}$	140	–	ns	–
TTDI	$\overline{INT}$ delay time from Tx data	–	4–6	TCY	–
TRCI	$\overline{INT}$ delay time from $\overline{RxC}$	–	7–11	TCY	–
TMH	$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse width high	200	–	ns	–
TML	$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse width low	200	–	ns	–
TMI	$\overline{INT}$ delay from $\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$	–	500	ns	–
TRV	Recovery time for $\overline{RD}$, $\overline{WR}$	300	–	ns	–
TAWT	$\overline{WAIT}$ delay time from address	–	120	ns	–
TRCS	$\overline{SYNC}$ setup time to $\overline{RxC}$	–	100	ns	–

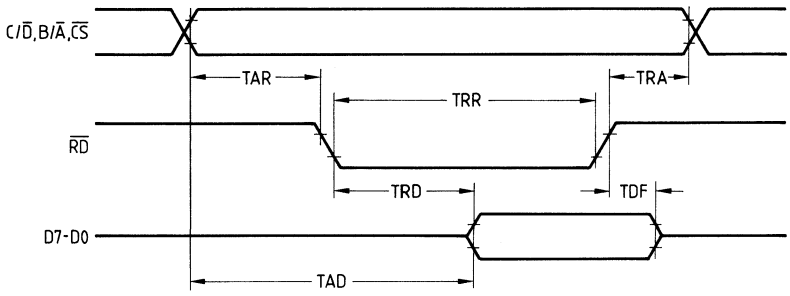
Note
$\overline{RESET}$ must be active for a minimum of one complete CLK cycle.
In all modes, system clock rate must be 4.5 times data rate.

AC Testing Input/Output Waveform

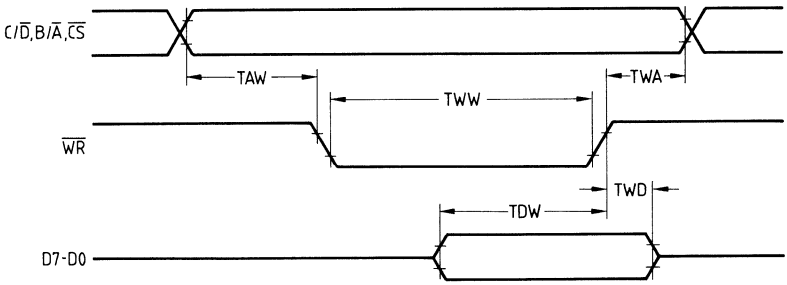


Waveforms

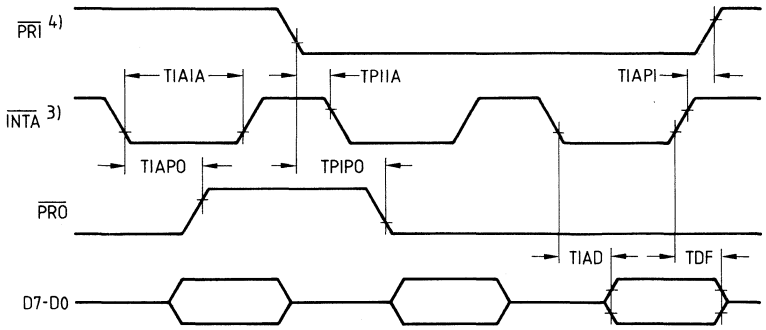
Read Cycle Timing



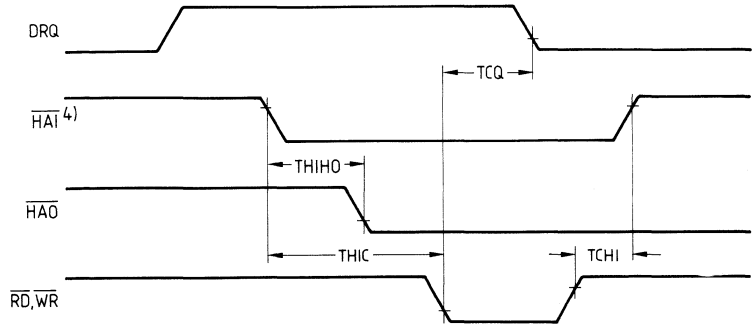
Write Cycle Timing



$\overline{\text{INTA}}$ Cycle Timing

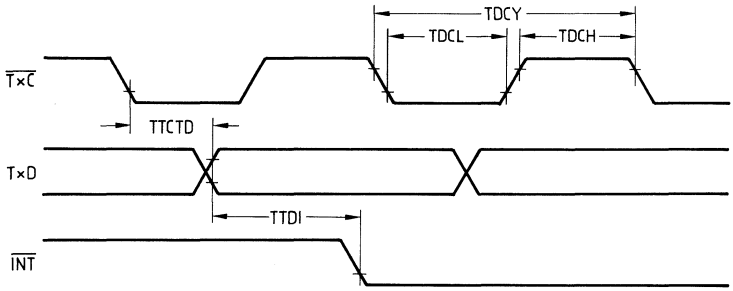


DMA Cycle Timing

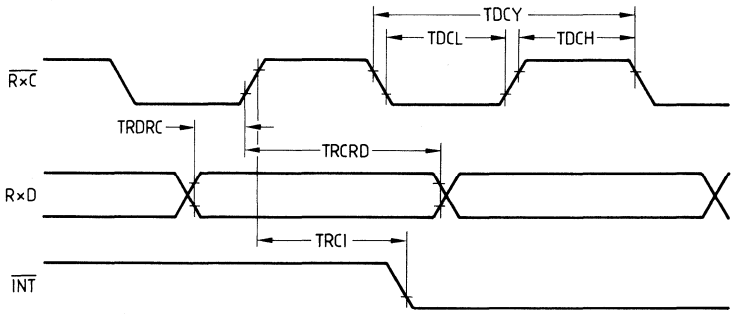


Note
3) $\overline{\text{INTA}}$ signal acts as $\overline{\text{RD}}$ signal.
4) $\overline{\text{PRI}}$ and $\overline{\text{HAI}}$ signals act as $\overline{\text{CS}}$ signal.

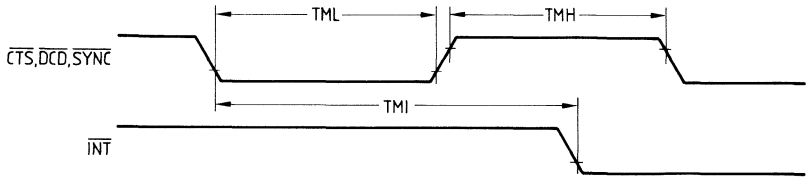
Transmit Cycle Timing



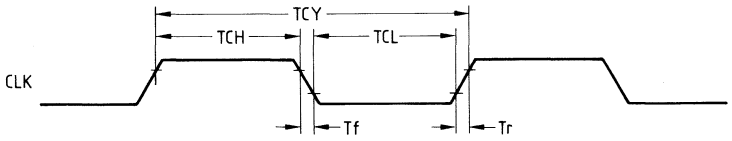
Receive Cycle Timing



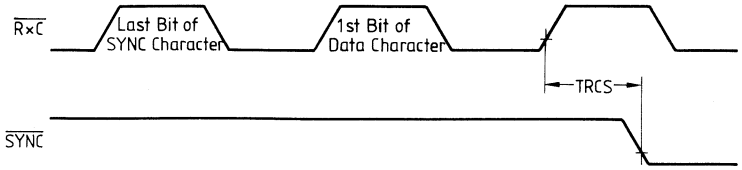
External/Status Timing



Clock Timing

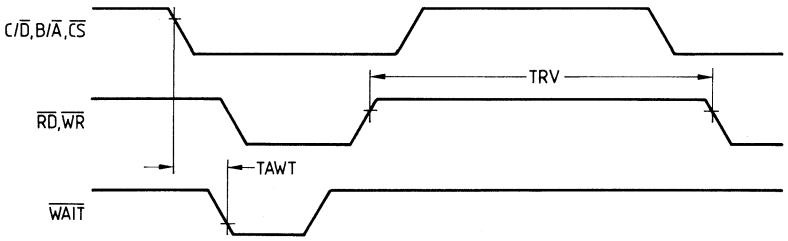


$\overline{\text{SYNC}}$ Input Timing (external sync mode)



$\overline{\text{SYNC}}$ input should become 0 (low level) at rising edge of $\overline{\text{RxC}}$ after two clock cycles from the last bit of SYNC character.

Read/Write Cycle Timing (software block transfer mode)



Ordering Information

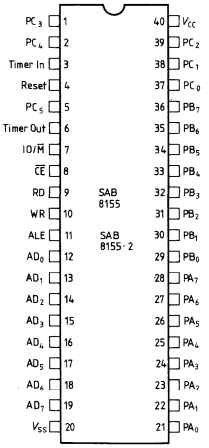
Type	Description	Ordering code
SAB 7201A-P	Multi-protocol serial communication controller MPSC	Q67120-P143

SIEMENS

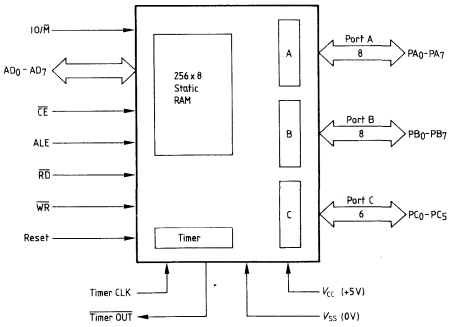
SAB 8155, SAB 8155-2 2048 Bit Static MOS RAM with I/O Ports and Timer

- 256 Word × 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8-Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with SAB 8085A and SAB 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

Pin Configuration



Block Diagram



The SAB 8155 is a RAM and I/O chip to be used in the SAB 8085A and SAB 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256×8. They have a maximum access time of 400ns to permit use with no wait states in SAB 8085A CPU. The SAB 8155-2 has a maximum access time of 330ns for use with the SAB 8085A-2 and the full speed 5MHz SAB 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
PCØ–PC5	1, 2, 5, 37–39	I/O	PORT C – These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PCØ-PC5 are used as control signals, they will provide the following: PCØ – A INTR (Port A Interrupt) PC1 – ABF (Port A Buffer Full) PC2 – $\overline{\text{A STB}}$ (Port A Strobe) PC3 – B INTR (Port B Interrupt) PC4 – B BF (Port B Buffer Full) PC5 – $\overline{\text{B STB}}$ (Port B Strobe)
TIMER IN	3	I	TIMER INPUT – Input to the counter/timer.
RESET	4	I	RESET – Pulse provided by the SAB 8085A to initialize the system (connect to SAB 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two SAB 8085A clock cycle times.
$\overline{\text{TIMER OUT}}$	6	O	TIMER OUTPUT – This output can be either a square wave or a pulse, depending on the timer mode.
IO/$\overline{\text{M}}$	7	I	I/O MEMORY – Selects memory if low and I/O and command/status registers if high.
$\overline{\text{CE}}$	8	I	CHIP ENABLE – On this SAB 8155, this pin is $\overline{\text{CE}}$ and is ACTIVE LOW.
$\overline{\text{RD}}$	9	I	READ CONTROL – Input low on this line with the Chip Enable active enables and ADØ–AD7 buffers. If IO/$\overline{\text{M}}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{\text{WR}}$	10	I	WRITE CONTROL – Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{\text{M}}$.
ALE	11	I	ADDRESS LATCH ENABLE – This control signal latches both the address on the ADØ–AD7 lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.
ADØ–AD7	12–19	I/O	ADDRESS/DATA – 3-state Address/Data lines that interface with the CPU lower 8-bit Address-Data Bus. The 8-bit address is latched into the address latch inside the SAB 8155 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{\text{M}}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{\text{WR}}$ or $\overline{\text{RD}}$ input signal.

Symbol	Number	Input (I) Output (O)	Function
PAØ–PA7	21–28	I/O	PORT A – These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PBØ–PB7	29–36	I/O	PORT B – These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
V_{CC}	40		POWER SUPPLY (+5V)
V_{SS}	20		GROUND (0 V)

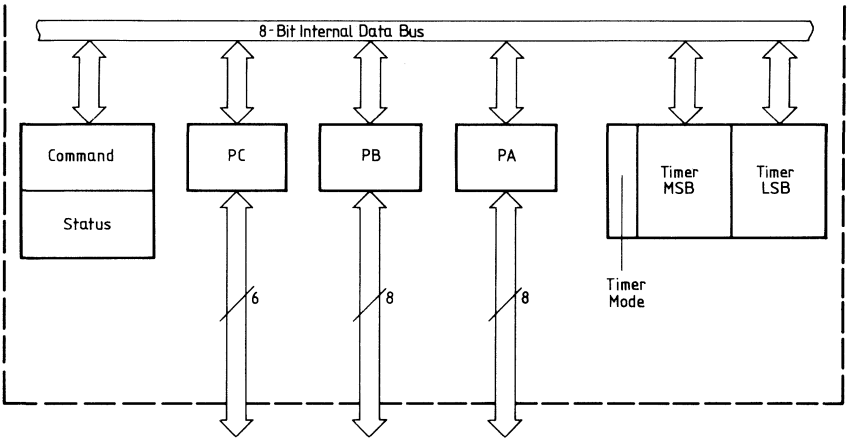
Functional Description

The SAB 8155 contains the following:

- 2Kbit Static RAM organized as 256×8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA0–PA7, PB0–PB7, PC0–PC5) or the memory (RAM) portion.

SAB 8155 Internal Registers



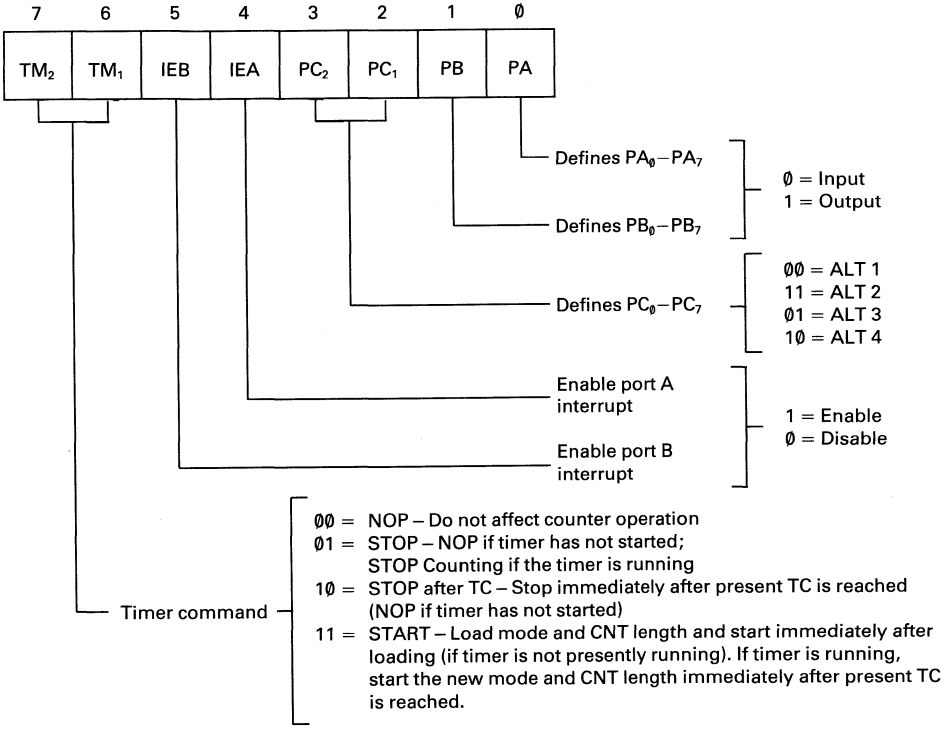
The 8-bit address on the Address/Data lines, Chip Enable input $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

Programming of the Command Register

The command register consists of eight latches. Four bits (Ø–3) define the mode of the ports, two bits (4–5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6–7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXXØØØ during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in the following figure. The contents of the command register may never be read.

Command Register Bit Assignment

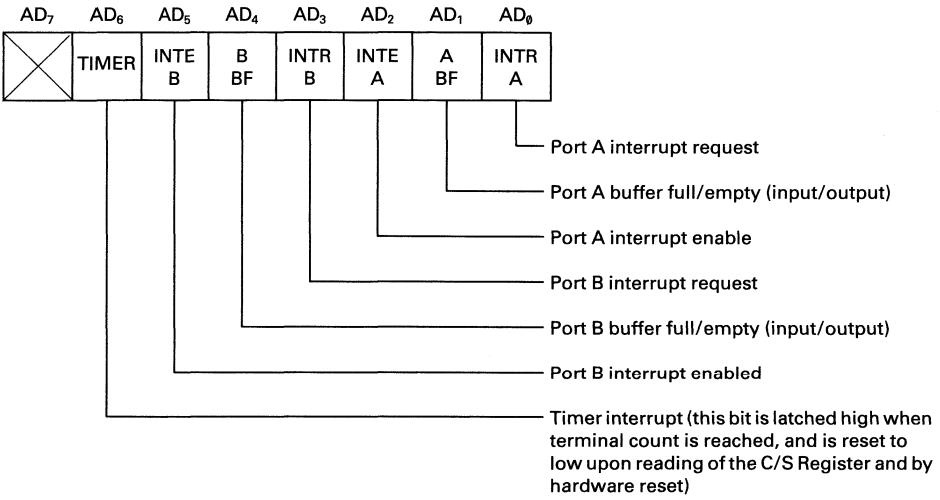


Reading the Status Register

The status register consists of seven latches, one for each bit; six (Ø–5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polles by reading the Status Register (Address XXXXXØØØ). Status word format is shown in the following figure. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

Status Register Bit Assignment



Input/Output Section

The I/O section of the SAB 8155 consists of five registers (see following figure):

- **Command/Status Register (C/S)** – Both registers are assigned the address XXXXXØØØ. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are **not** accessible through the pins.

  When the C/S (XXXXXØØØ) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the ADØ–AD7 lines.

- **PA Register** – This register can be programmed to be either input or – output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (see timing diagram). The I/O pins assigned in relation to this register are PAØ–PA7. The address of this register is XXXXXØØ1.

- **PB Register** – This register functions the same as PA Register. The I/O pins assigned are PBØ–PB7. The address of this register is XXXXXØ1Ø.

- **PC Register** – This register has the address XXXXXØ11 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA und PB by properly programming the AD2 and AD3 bits of the C/S register.

  When PCØ–PC5 is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the SAB 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode (see table Port Control Assignment).

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

Control	Input Mode	Output Mode
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

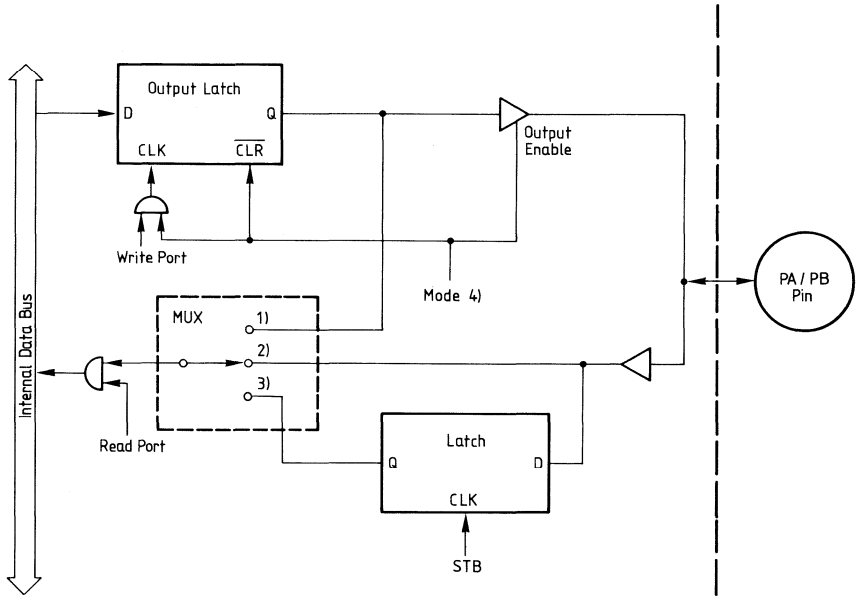
I/O Port and Timer Addressing Scheme

I/O Address *								Selection
A7	A6	A5	A4	A3	A2	A1	AØ	
X	X	X	X	X	Ø	Ø	Ø	Interval Command/Status Register
X	X	X	X	X	Ø	Ø	1	General Purpose I/O Port A
X	X	X	X	X	Ø	1	Ø	General Purpose I/O Port B
X	X	X	X	X	Ø	1	1	Port C – General Purpose I/O or Control
X	X	X	X	X	1	Ø	Ø	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	Ø	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care.
*: I/O Address must be qualified by $\overline{CE}$ = Ø and IO/$\overline{M}$ = 1 in order to select the appropriate register.

The following figure shows how I/O PORTS A and B are structured within the SAB 8155:

SAB 8155 Port Functions



Notes:

1) Output Mode
2) Simple Input } Multiplexer Control
3) Strobed Input

4) = 1 for Output Mode
= Ø for Input Mode

Read Port = (IO/$\overline{M}$ = 1) × ($\overline{RD}$ = Ø) × (CE Active) × (Port Address selected)
Write Port = (IO/$\overline{M}$ = 1) × ($\overline{WR}$ = Ø) × (CE Active) × (Port Address selected)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the SAB 8155 are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the SAB 8155 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

Port Control Assignment

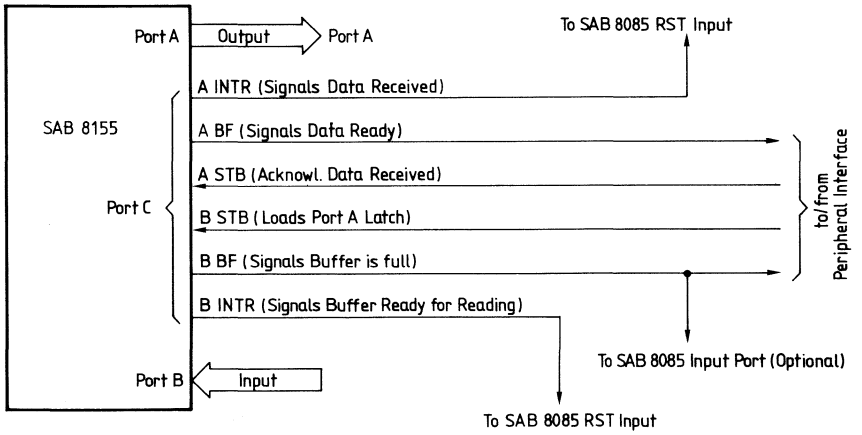
Pin	ALT 1	ALT 2	ALT 3	ALT 4
PCØ	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{\text{STB}}$ (Port A Strobe)	A $\overline{\text{STB}}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{\text{STB}}$ (Port B Strobe)

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Next figure shows how the SAB 8155 I/O ports might be configured in a typical SAB 8085 system.

Example: Command Register = ØØ111ØØ1



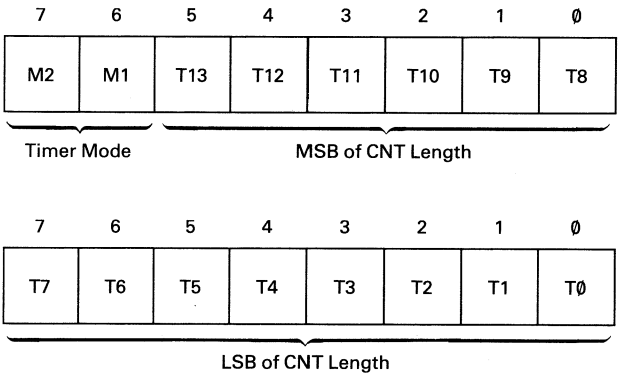
Timer Section

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX1ØØ for the low order byte of the register and the I/O address XXXXX1Ø1 for the high order byte of the register (see figure I/O Port and Timer Addressing Scheme).

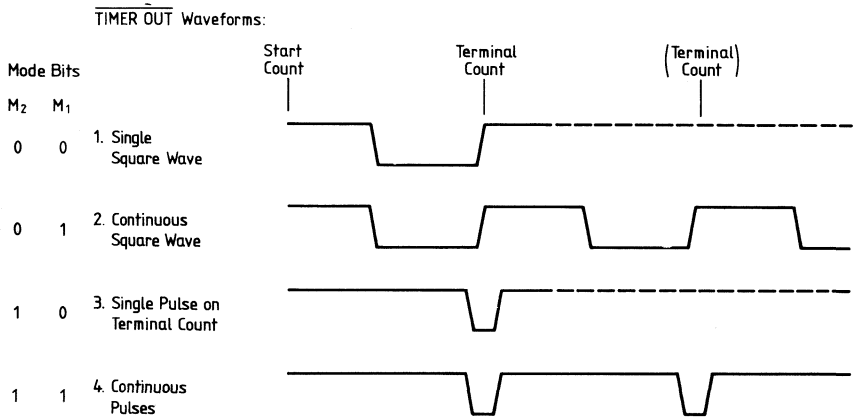
To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits Ø–13 of the high order count register will specify the length of the next count and bits 14–15 of the high order register will specify the timer output mode (see next figure). The value loaded into the count length register can have any value from 2H through 3FFH in Bits Ø–13.

Timer Format



There are four modes to choose from: M2 and M1 define the timer mode, as shown in following figure.

Timer Modes



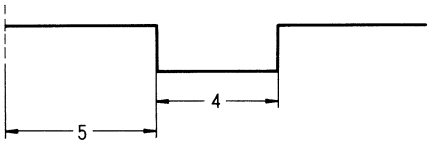
Bits 6–7 (TM2 and TM1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM2	TM1	Function
Ø	Ø	NOP – Do not affect counter operation
Ø	1	STOP – NOP if timer has not startet; stop counting if the timer is running
1	Ø	STOP AFTER TC – Stop immediately after present TC is reached (NOP if timer has not startet)
1	1	START – Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you **must** issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in next figure.

Asymmetrical Square-Wave Output Resulting from Count of 9



Note: 5 and 4 refer to the number of clocks in that time period

The counter in the SAB 8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the SAB 8155 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the SAB 8085A be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To abtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set. add ½ of the full original count (½ full count – 1 if full count is odd)

Note:
If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts have occured. Regardless of this, the SAB 8155 always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

Absolute maximum ratings *)

Temperature Under Bias	0 to +70°C
Storage Temperature	−65 to +150°C
Voltage on any Pin with Respect to Ground	−0.5 to +7 V
Power Dissipation	1.5 Watt

D.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±5%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5		
V_{OL}	Output Low Voltage	–	0.45		I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH} = −400 µA
I_{IL}	Input Leakage	–	±10	µA	V_{IN} = V_{CC} to 0 V
I_{LO}	Output Leakage				0.45 V ≦ V_{OUT} ≦ V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	–
I_{IL} (CE)	Chip Enable Leakage		+100	µA	V_{IN} = V_{CC} to 0 V

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

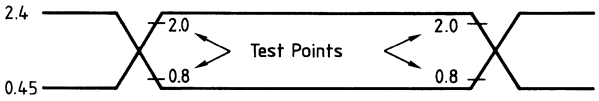
A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 5%

Symbol	Parameter	Limit Values				Units
		SAB 8155		SAB 8155-2		
		Min.	Max.	Min.	Max.	
t_{AL}	Address to Latch Set Up Time	50				
t_{LA}	Address Hold Time after Latch	80	–	30	–	
t_{LC}	Latch to READ/WRITE Control	100		40		
t_{RD}	Valid Data Out Delay from READ Control	–	170	–	140	
t_{AD}	Address Stable to Data Out Valid		400		330	
t_{LL}	Latch Enable Width	100	–	70	–	
t_{RDF}	Data Bus Float After READ	0	100	0	80	
t_{CL}	READ/WRITE Control to Latch Enable	20		10		
t_{CC}	READ/WRITE Control Width	250		200		
t_{DW}	Data In to WRITE Set Up Time	150	–	100	–	
t_{WD}	Data In Hold Time After WRITE	0		0		
t_{RV}	Recovery Time Between Controls	300		200		
t_{WP}	WRITE to Port Output	–	400	–	300	ns
t_{PR}	Port Input Setup Time	70	–	50	–	
t_{RP}	Port Input Hold Time	50	–	10	–	
t_{SBF}	Strobe to Buffer Full	–	400	–	300	
t_{SS}	Strobe Width	200	–	150	–	
t_{RBE}	READ to Buffer Empty					
t_{SI}	Strobe to INTR ON	–	400	–	300	
t_{RDI}	READ to INTR Off					
t_{PSS}	Port Setup Time to Strobe Strobe	50	–	0	–	
t_{PHS}	Port Hold Time After Strobe	120		100		
t_{SBE}	Strobe to Buffer Empty					
t_{WBF}	WRITE to Buffer Full					
t_{WI}	WRITE to INTR Off	–	400	–	300	
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low					
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High					
t_{RDE}	Data Bus Enable from READ Control	10		10		
t_1	TIMER-IN Low Time	80	–	40	–	
t_2	TIMER-IN High Time	120		70		

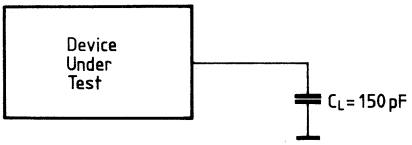
A.C. Testing

Input/Output Waveform



A.C. Testing: Input are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0".
Timing Measurements are made at 2.0 V for Both a Logic "1" and 0.8 V for a Logic "0".

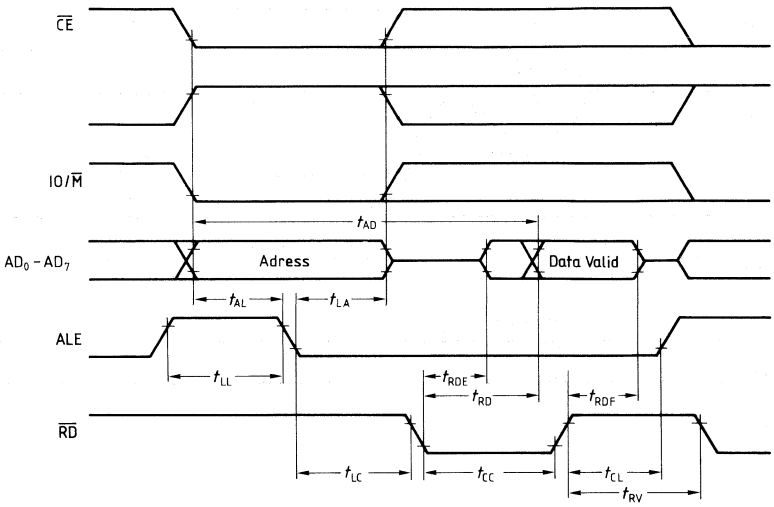
Load Circuit



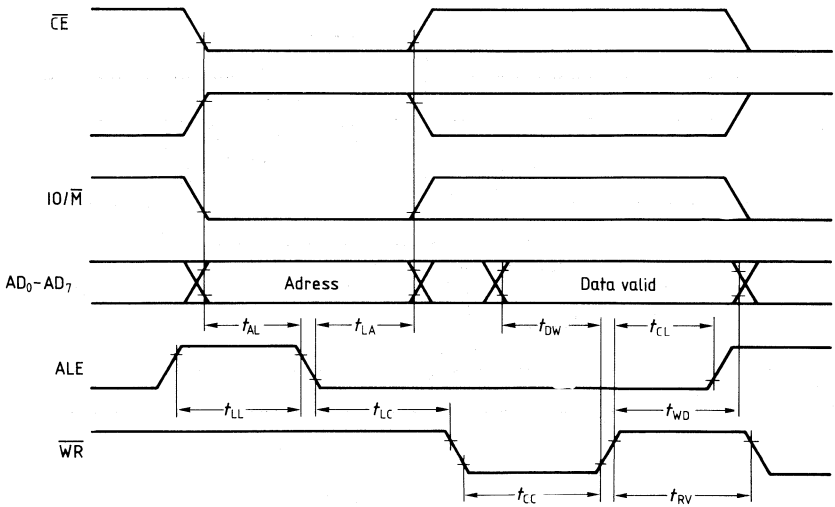
C_L = 150 pF
C_L = Includes JIG Capacitance

Waveforms

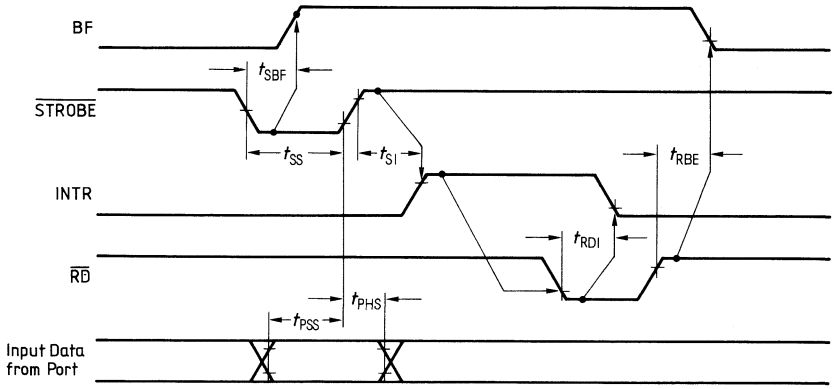
Read Cycle



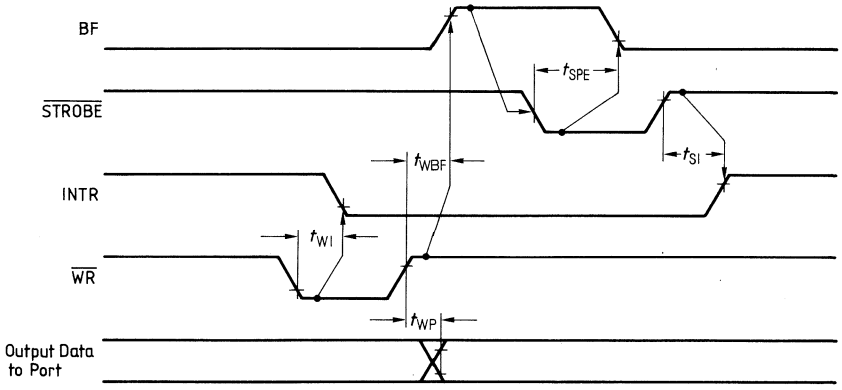
Write Cycle



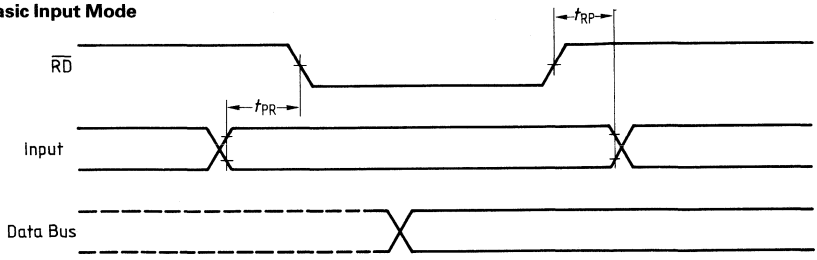
Strobed Input Mode



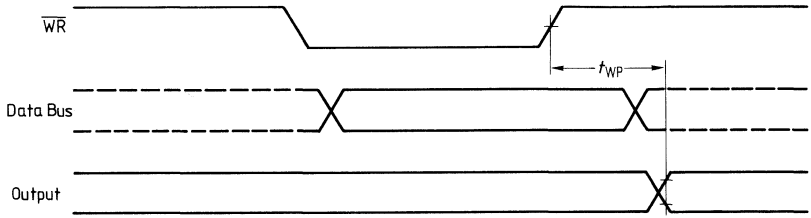
Strobed Output Mode



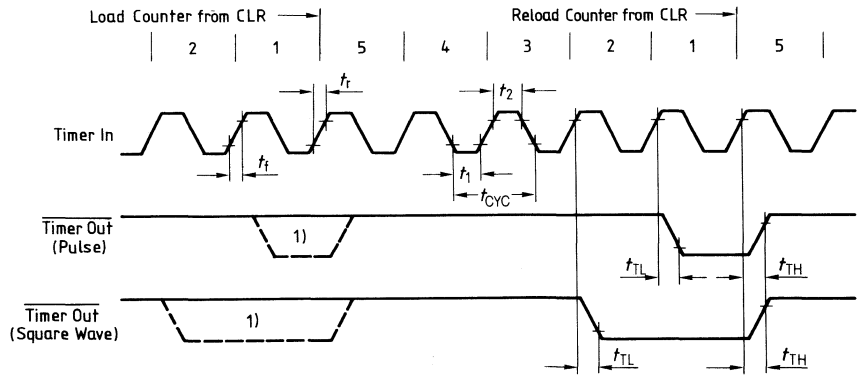
Basic Input Mode



Basic Output Mode



Timer Output Countdown from 5 to 1



1) The Timer Output is periodic if an automatic reload Mode (M1 Mode Bit = 1)

Ordering Description

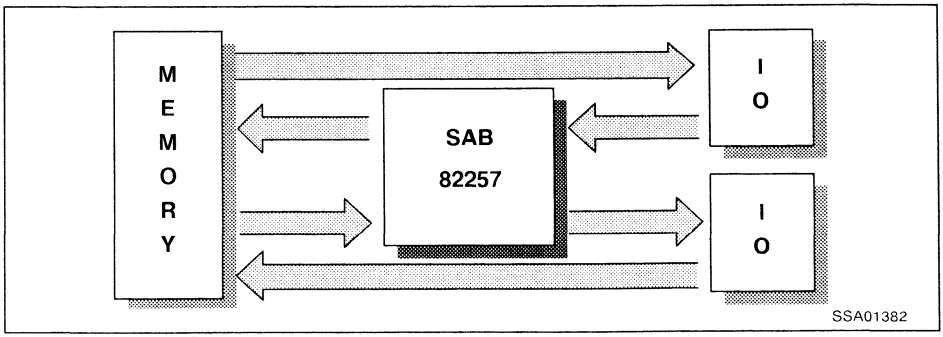
Type	Description	Ordering Number
	RAM with I/O Port and Timer	
SAB 8155-C	Ceramic	Q 67120–Q 43
SAB 8155-P	Plastic	Q 67120–Q 42
SAB 8155-2-C	Ceramic	Q 67120–Q 85
SAB 8155-2-P	Plastic	Q 67120–Q 86

SIEMENS

Advanced DMA Controller SAB 82257
for 8-/16-Bit Microcomputer Systems

Preliminary **8 MHz**

- High-performance 16-bit DMA controller for 16-bit family processors SAB 80286, SAB 80186/188, SAB 8086/88
- 4 independent high-speed DMA channels
- Adaptive on-chip bus interface for direct connection to 16/8-bit processors
- Standalone operation for modular systems
- Programmable bus loading
- Transfer rates up to 8 Mbytes/s (8 MHz system)
- 16 Mbytes addressing range
- 16 Mbytes maximum block size
- Command chaining for automatic processing
- Automatic data chaining (scattering/ gathering) for flexible data structures
- Single and double cycle transfers
- Automatic assembly/disassembly of data
- Memory-based communication scheme with CPU



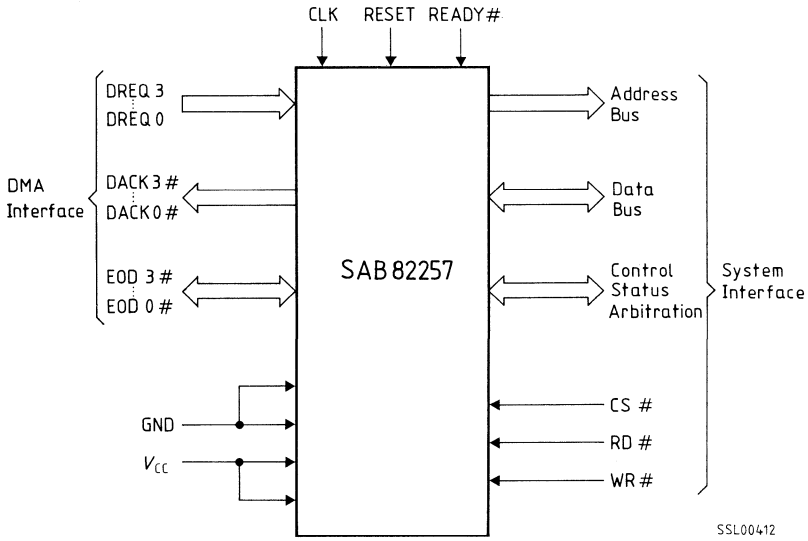
The SAB 82257 is an advanced DMA (direct memory access) controller especially designed for the 16-bit microprocessors SAB 80286 and SAB 8086/186/88/188. In addition the operation with other processors is supported by the remote mode. The SAB 82257 has 4 independent DMA channels which can transfer data at rates up to 8 Mbytes/ s at 8 MHz clock frequency in an SAB 80286 system or up to 4 Mbytes/ s at 8 MHz in an SAB 8086/80186 system. This great bandwidth allows the user to handle very fast data transfers or a large number of concurrent peripherals.

The device is fabricated in advanced +5 V N-channel Siemens MYMOS technology and comes in a 68-pin plastic leaded chip carrier (PL-CC-68).

Ordering Information

Type	Ordering code	Package	Function
SAB 82257-N	Q67120-P176	PL-CC-68	Advanced DMA controller, 8 MHz

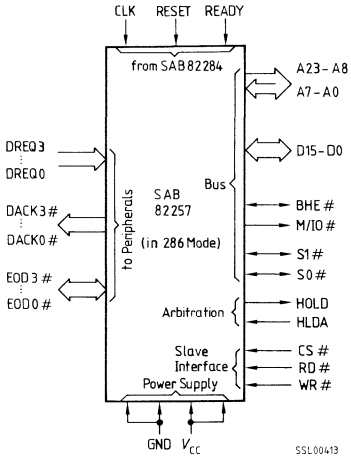
Logic Symbol



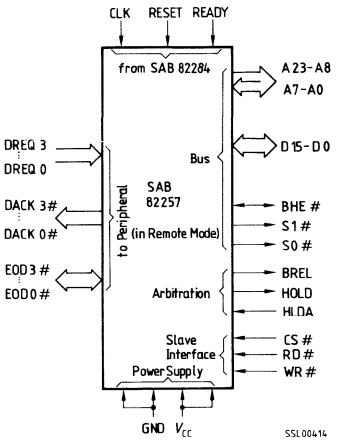
Modes of Operation, Adaptive Bus Interface

Like the advanced DMA controller SAB 82258A, the SAB 82257 has been defined to work with all 16-bit processors linke SAB 80286, SAB 80186/188 and SAB 8086/88 without additional support and interface logic. Hence the local buses of the above processors are different in signals, functions and timings, the SAB 82257 has an adaptive bus interface to meet the different requirements of these local buses.

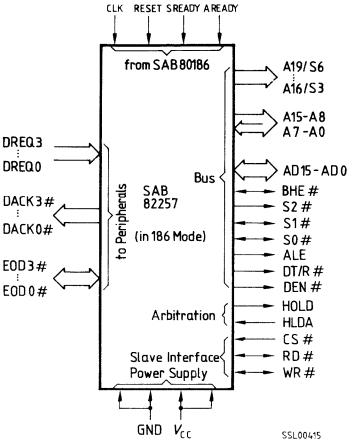
Logic Symbol in 286 Mode



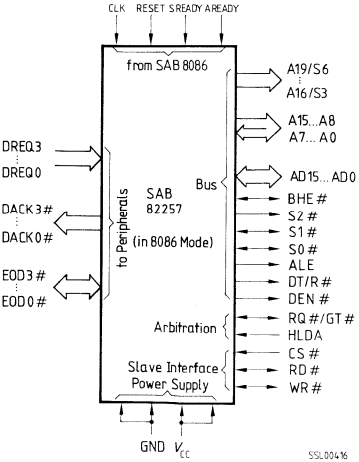
Logic Symbol in Remote Mode



Logic Symbol in 186 Mode



Logic Symbol in 8086 Mode

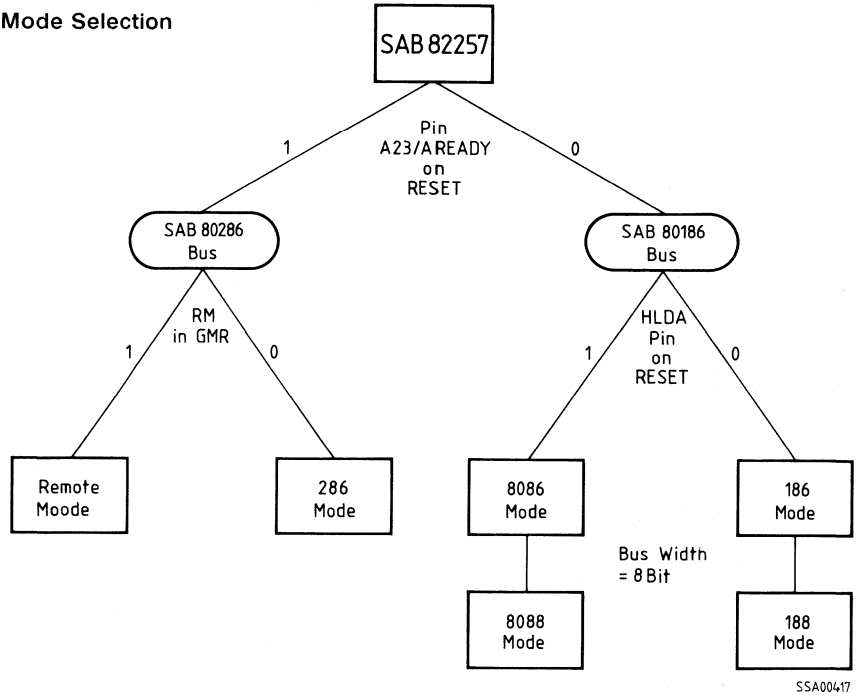


As a result of this, a bus compatibility with identical timing is attained with the processors SAB 80286, SAB 80186 and SAB 8086. A compatibility with the 8-bit bus versions of these processors, SAB 8088 and SAB 80188, is also guaranteed by defining the physical bus width of the SAB 82257 (per software) as 8 bits. The only difference in operation with SAB 8086 or SAB 80186 is that for SAB 8086 the HOLD pin functions as RQ#/GT# line (if HLDA is held high on reset).

The SAB 82257 can also be operated in remote or standalone mode, in which case it is not coupled directly to a processor. In remote mode, the SAB 82257 can be operated as sole bus master in a multimaster environment. The SAB 82257 is programmed to a specific mode of operation by applying defined logic levels to certain pins during reset and by setting the status of several control bits (see figure below).

Note: *Pin 57 (A21/DT/R# of the SAB 82257) must be high during reset in order to enable proper operation. This is provided, if pin A21 is connected to the SAB 80286's address bus. An internal pullup resistor supports applications where pin 57 is left open.*

Mode Selection

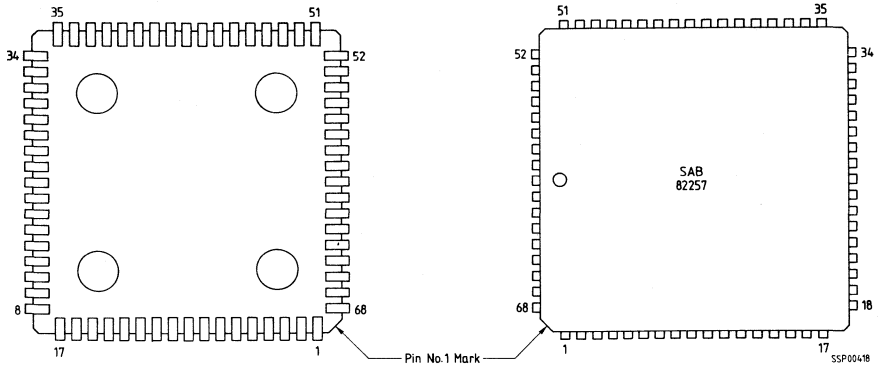


Pin 57 (A21 or DT/R#) must be high during Reset to enter the desired operating mode. An internal pullup pulls this pin high, if nothing is driving it.

Pin Configuration

PL-CC-68
Bottom view

PL-CC-68
Top view



Pin Definitions and Functions

Some pins of the SAB 82257 serve for different purposes according to the different modes of bus operation. The table below summarizes the pinouts of the SAB 82257 in the various modes. A detailed description of the general pin functions as well as the mode-specific pin functions is given in the following sections.

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
16	HOLD	O	HOLD	O	HOLD or RQ#/GT#	O (186) I/O (8086)
17	HLDA	I	HLDA	I	HLDA	I
1	BHE#	I/O	BHE#	I/O	BHE#	I/O
14	M/IO#	O	BREL	O	S2#	O
11	S1#	I/O	S1#	O	S1#	I/O
13	S0#	I/O	S0#	O	S0#	I/O
8	CS#	I	CS#	I	CS#	I
2	RD#	I	RD#	I	RD#	I/O
3	WR#	I	WR#	I	WR#	I/O
10	READY#	I	READY#	I	SREADY	I
59	A23	O	A23	O	AREADY	I
59	A23	O	A23	O	AREADY	I
58	A22	O	A22	O	ALE	O
57	A21	O	A21	O	DT/R#	O
56	A20	O	A20	O	DEN#	O
55	A19	O	A19	O	A19/S6	O
54	A18	O	A18	O	A18/S5	O
53	A17	O	A17	O	A17/S4	O
52	A16	O	A16	O	A16/S3	O
51	A15	O	A15	O	A15	O
50	A14	O	A14	O	A14	O
49	A13	O	A13	O	A13	O
48	A12	O	A12	O	A12	O
47	A11	O	A11	O	A11	O
46	A10	O	A10	O	A10	O
45	A9	O	A9	O	A9	O
44	A8	O	A8	O	A8	O
42	A7	I/O	A7	I/O	A7	I/O
41	A6	I/O	A6	I/O	A6	I/O
40	A5	I/O	A5	I/O	A5	I/O
39	A4	I/O	A4	I/O	A4	I/O

Pin Definitions and Functions (cont'd)

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
38	A3	I/O	A3	I/O	A3	I/O
37	A2	I/O	A2	I/O	A2	I/O
36	A1	I/O	A1	I/O	A1	I/O
35	A0	I/O	A0	I/O	AO	I/O
18	D15	I/O	D15	I/O	AD15	I/O
20	D14	I/O	D14	I/O	AD14	I/O
22	D13	I/O	D13	I/O	AD13	I/O
24	D12	I/O	D12	I/O	AD12	I/O
27	D11	I/O	D11	I/O	AD11	I/O
29	D10	I/O	D10	I/O	AD10	I/O
31	D9	I/O	D9	I/O	AD9	I/O
33	D8	I/O	D8	I/O	AD8	I/O
19	D7	I/O	D7	I/O	AD7	I/O
21	D6	I/O	D6	I/O	AD6	I/O
23	D5	I/O	D5	I/O	AD5	I/O
25	D4	I/O	D4	I/O	AD4	I/O
28	D3	I/O	D3	I/O	AD3	I/O
30	D2	I/O	D2	I/O	AD2	I/O
32	D1	I/O	D1	I/O	AD1	I/O
34	D0	I/O	D0	I/O	AD0	I/O
7	DREQ0	I	DREQ0	I	DREQ0	I
6	DREQ1	I	DREQ1	I	DREQ1	I
5	DREQ2	I	DREQ2	I	DREQ2	I
4	DREQ3	I	DREQ3	I	DREQ3	I
61	DACK0#	O	DACK0#	O	DACK0#	O
62	DACK1#	O	DACK1#	O	DACK1#	O
63	DACK2#	O	DACK2#	O	DACK2#	O
64	DACK3#	O	DACK3#	O	DACK3#	O
65	EOD0#	I/O	EOD0#	I/O	EOD0#	I/O
66	EOD1#	I/O	EOD1#	I/O	EOD1#	I/O
67	EOD2#	I/O	EOD2#	I/O	EOD2#	I/O
68	EOD3#	I/O	EOD3#	I/O	EOD3#	I/O
15	RESET	I	RESET	I	RESET	I
12	CLK	I	CLK	I	CLK	I
9,43	GND	–	GND	–	GND	–
26,60	V_{CC}	–	V_{CC}	–	V_{CC}	–

Pin Definitions for All Operating Modes

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>BHE#</td><td>1</td><td>I/O</td><td>BUS HIGH ENABLE
This active low input indicates transfer of data on the upper byte of the data bus, D15 to D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use BHE# to condition chip select functions. BHE# floats to tristate off when the SAB 82257 does not own the bus.
BHE# and A0 encodings
<table>
<tr><th>BHE#</th><th>A0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer (D15-D8)</td></tr>
<tr><td>0</td><td>1</td><td>Byte transfer on upper half of data bus (D15-D8)</td></tr>
<tr><td>1</td><td>0</td><td>Byte transfer on lower half of data bus (D7-D0)</td></tr>
<tr><td>1</td><td>1</td><td>Odd-addressed byte on 8-bit bus (D7-D0)</td></tr>
</table></td></tr>
<tr><td>RD#</td><td>2</td><td>I</td><td>READ
This active low input in conjunction with chip select enables reading the SAB 82257 register which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82257 clock.</td></tr>
<tr><td>WR#</td><td>3</td><td>I</td><td>WRITE
This active low input in conjunction with chip select enables writing into the SAB 82257 registers which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82257 clock.</td></tr>
<tr><td>DREQ0-
DREQ3</td><td>4-7</td><td>I</td><td>DMA REQUEST (0 TO 3)
These active high inputs are used for synchronized DMA transfers. DREQ3 has the meaning of I/O request (IOREQ) if channel 3 is a multiplexer channel. These signals can be asynchronous to the SAB 82257 clock.</td></tr>
</table>

Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CS#	8	I	**CHIP SELECT** This active low input enables the access of a processor to SAB 82257 registers. This access is additionally controlled either by bus status signals or by the read or write command signals. Chip select can be asynchronous to the SAB 82257 clock.
CLK	12	I	**CLOCK** This input provides the fundamental timing. In 286 mode and remote mode it must be two times the system clock. It can be directly connected to the SAB 82284 CLK output. It is divided by two to generate the SAB 82257 internal clock. The on-chip divide-by-two circuitry can be synchronized to the external clock generator by a low-to-high transition on the RESET input, or by the first high-to-low transition on the status inputs S0# or S1# after reset. In 186/8086 mode no internal prescaling is done.
S0#, S1#	11, 13	I/O	**BUS STATUS LINES (0, 1)** These signals control the support circuits. The beginning of a bus cycle is indicated by S1# or S0# or both going active. The termination of a bus cycle is indicated by all status signals going inactive in 186 mode or bus ready signal (READY#) going active in 286 mode. The type of bus cycle is indicated by S0#, S1# and S2# (in 186 mode) or M/IO# (in 286 mode). S2# and M/IO# have the same meaning but in 186 mode the S2# signal can be active only when at least one of S1# or S0# is active, whereas in 286 mode the M/IO# signal is valid with the address on the address lines. The SAB 82257 can generate the following bus cycles by activating the status signals (and M/IO# in 286 mode):

Pin Definitions for All Operating Modes (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>S0#,S1#
(cont'd)</td><td>11, 13</td><td>I/O</td><td>
<table>
<tr><th>M/IO#
or S2#</th><th>S1#</th><th>S0#</th><th>Cycle Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Read I/O-vector
(for multiplexer channel)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from I/O space</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into I/O space</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle, does not
occur in 186 mode</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read from memory space</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write into memory space</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No bus cycle</td></tr>
</table>
When the SAB 82257 is not the master of the local bus the status signals are used as inputs for detection of synchronous accesses to the SAB 82257. The following table shows the bus status and CS# signals and their interpretation by the SAB 82258.
<table>
<tr><th>CS#</th><th>S1#</th><th>S0#</th><th>Description</th></tr>
<tr><td>1</td><td>X</td><td>X</td><td>SAB 82257 is not
selected (no action)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No SAB 82257
access (no action)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from an
SAB 82257 register</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into an
SAB 82257 register</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle[1)]</td></tr>
</table>
</td></tr>
</table>

1) SAB 82257 is selected but no synchronous access is activated. In this case the SAB 82257 monitors RD# and WR# signals for detection of an asynchronous access.

Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
RESET	15	I	**SYSTEM RESET** An activation of the reset signal forces the SAB 82257 to the initial state. The reset signal must be synchronous to CLK.
DACK0#- DACK3#	61-64	O	**DMA ACKNOWLEDGE (0 TO 3)** These active low inputs acknowledge the requests on the related DREQn signals. They are activated when the requested transfer(s) is (are) performed. If the channel 3 is a multiplexer channel the signal DACK3# has the meaning of I/O acknowledge (IOACK#).
EOD0#- EOD3#	65-68	I/O	**END OF DMA (0 TO 3)** These lines are implemented as open drain output drivers with a high impedance pullup resistor and thus can be used as bidirectional lines. As **outputs** the lines are activated for two system clock cycles at the end of the DMA transfer of the corresponding channel (if enabled) or they are activated under program control (EOD output or interrupt output). If the lines are held internally high but forced to low by external circuitry, they act as "End of DMA" **inputs.** The current transfer is aborted and the SAB 82257 continues with the next command. Additionally, a special function is possible with the EOD2# pin: this pin can also be used as common interrupt signal for all 4 channels. In this mode this line is not an open drain output but a pushpull output (output only). The other EOD# pins may be used as EOD# outputs/inputs as described above.
V_{CC}	26, 60		**POWER SUPPLY** (+5 V)
GND	9, 43		**GROUND** (0 V)

Pin Definitions for 286 Mode and Remote Mode

In 286 mode the SAB 82257 bus signals and bus timings are the same as for the SAB 80286 processor. Additional features of the SAB 82257 require a slight change in pin definitions. The processor can access internal registers of the SAB 82257. Therefore the bus signals must support these accesses. This means that some of the bus control signals must be bidirectional and some additional bus control signals are necessary. All additional pins and their functions are listed below.

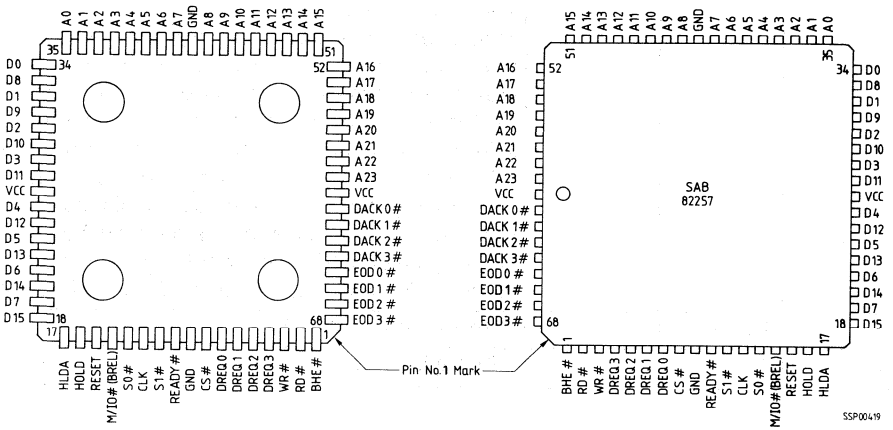
In **remote mode** most of the bus signals are the same as in 286 mode. Pin 14 (M/IO#) serves as BREL output. The HOLD/HLDA arbitration in remote mode is used only for system bus accesses, the resident bus is accessed directly.

The CS# input additionally requests access to the local bus of the SAB 82257. These accesses are enabled through the BREL output after the SAB 82257 has released the bus.

Pin Configuration in 286 Mode and Remote Mode

Component Pad View – As viewed from underside of component when mounted on the board

PC Board View – As viewed from the component side of the pc board



Pin Definitions for 286 Mode and Remote Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
READY#	10	I	**BUS READY** This active low input terminates a bus cycle. Bus cycles are extended without limit until terminated by READY# low. READY# is a synchronous input requiring setup and hold times relative to the system clock to be met for correct operation.
M/IO#	14 (286 mode)	O	**Memory / I/O SELECT** In 286 mode, pin 14 is used to distinguish between memory and I/O space addresses.
BREL	14 (remote mode)	O	**BUS RELEASE** In remote mode pin 14 is used to indicate when the SAB 82257 has released the control of the local bus.
HOLD	16	O	**BUS HOLD REQUEST** This active high output indicates a request for control of the local bus (286 mode) or the system bus (remote mode). When the SAB 82257 relinquishes the bus it drops the HOLD output. HOLD is connected to the bus arbiter in remote mode.
HLDA	17	I	**BUS HOLD ACKNOWLEDGE** This active high input indicates that the SAB 82257 can acquire the control of the bus. When it goes low SAB 82257 must relinquish the bus at the end of its current cycle. HLDA can be asynchronous to the SAB 82257 clock. HLDA is connected to the bus arbiter in remote mode.
D0-D15	18-25, 27-34	I/O	**DATA BUS (0 TO 15)** This is the bidirectional 16-bit data bus. For use with an 8-bit bus, only the lower 8 data lines D7-D0 are relevant.
A0-A7	35-42	I/O	**ADDRESS BUS (0 TO 7)** The lower 8 address lines for DMA transfers. They are also used to input the register address when the processor accesses an SAB 82257 register.
A8-A23	44-59	O	**ADDRESS BUS (8 TO 23)** Higher address outputs.

Pin Definitions for 186 Mode and 8086 Mode

In 186 mode and 8086 mode the SAB 82257 multiplexes the address with data and additional status lines.

Pins A0 to A15 retain their original function while pins A20 to A23 serve for different purposes (not used for address in 186/8086 mode).

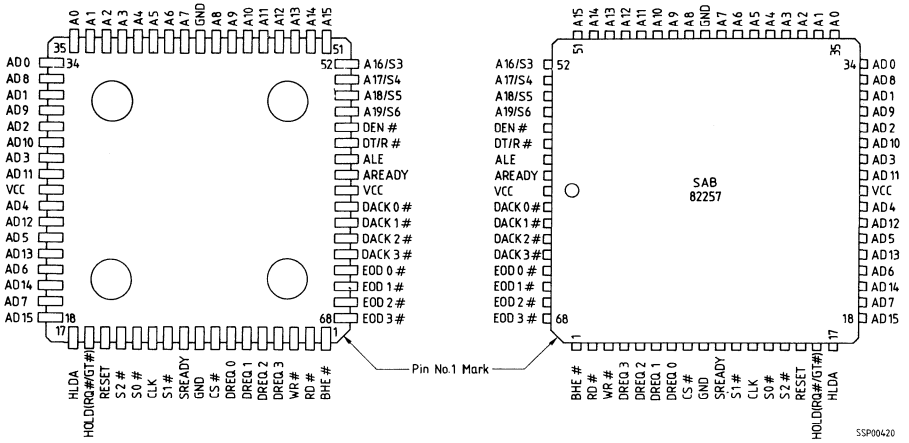
The RD# and WR# lines are additionally used as outputs in 186/8086 mode to support minimum mode systems.

Note that the HLDA input can be used to force the SAB 82257 off the bus in 8086 mode, even though the arbitration is done via the RQ#/GT# line!

Pin Configuration in 186 Mode and 8086 Mode

Component Pad View – As viewed from underside of component when mounted on the board

PC Board View – As viewed from the component side of the pc board



Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ALE	58	O	**ADDRESS LATCH ENABLE** This active high output provides a strobe signal to separate the address information on the multiplexed AD lines.
DEN#	56	O	**DATA ENABLE** This active low output enables the data transceivers.
DT/R#	57	O	**DATA TRANSMIT/RECEIVE** This signal controls the direction of the data transceivers. When low, data is transferred to the SAB 82257, when high, the SAB 82257 places data onto the data bus.
S2#	14	O	**STATUS LINE 2** Signal as for SAB 186/8086/88 processors (see also S1#, S0# description in 286 mode).
AREADY	59	I	**ASYNCHRONOUS READY** The rising edge of this signal is internally synchronized, the falling edge must be synchronous to CLK. During reset this signal must be low to enter 186 mode.
SREADY	10	I	**SYNCHRONOUS READY** This signal must be synchronized externally. The use of this pin permits a relaxed system-timing specification by eliminating the clock phase which is required for resolving the signal level when using the AREADY input.
AD0-AD15	18-25 27-34	I/O	**ADDRESS/DATA BUS (0 to 15)** Lower address and data information is multiplexed on pin AD0 to AD15.
A0-A7 A8-A15	35-42 44-51	I/O O	**ADDRESS BUS (0 to 15)** Additionally the demultiplexed address information is available on address pin A0 to A15.

Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A16/S3-A19/S6	52–55	O	**ADDRESS BUS (16 TO 19)/ STATUS LINES (3 TO 6)** The higher address bits are multiplexed with additional status information.
HLDA	17	I	**BUS HOLD ACKNOWLEDGE** This active high input indicates that the SAB 82257 can acquire the control of the bus. When it goes low the SAB 82257 must relinquish the bus at the end of its current bus cycle. HLDA can be asynchronous to the SAB 82257 clock. In 8086 mode, HLDA can be used to force the SAB 82257 off the bus.
HOLD	16 (186 mode)	O	**BUS HOLD REQUEST** This active high output indicates a request for control of the bus. When the SAB 82257 relinquishes the bus, it drops the HOLD output.
RQ#/GT#	16 (8086 mode)	I/O	**REQUEST/GRANT** In 8086 mode the HOLD output acts as RQ#/GT# line. The RQ#/GT# protocol implements a one-line communication dialog required to arbitrate the use of the system bus normally done via HOLD/HLDA. The RQ#/GT# signal is active low and has an internal pullup resistor.

Functional Description

General

The SAB 82257 is an advanced general-purpose DMA controller especially designed for efficient highspeed data transfers on an SAB 80286 bus as well as on an SAB 80186/188 or SAB 8086/88 bus.

It supports two basic operating modes:

- local mode (tightly coupled to a processor) and
- remote mode (loosely coupled to a processor).

In the first case the SAB 82257 is directly coupled to the CPU and uses the same system support/control devices as the CPU (see figure below). This mode is possible with the above-mentioned processors.

As a second basic operating mode remote (standalone) mode is supported (see figure below). Here the SAB 82257 has its own sets of bus interface circuits and thus can utilize its own local bus. This allows the DMA controller to work in parallel with the main CPU and therefore overall system performance can be increased. Besides, this mode is very useful for the design of modular systems and allows connecting the SAB 82257 to any other processor via the system bus independent of the processor's local bus.

The SAB 82257 has four independent DMA channels that can transfer up to 8 Mbytes/s in single cycle mode (2 clocks/transfer). In 2-cycle transfer mode the maximum rate is 4 Mbytes/s. Switching between channels induces no time penalty. Thus the overall maximum transfer rate of 8 Mbytes/s is also valid for multiple channel operation.

This fast operation is possible because of the pipelined architecture of the SAB 82257 which allows the different functional units to work in parallel.

The SAB 82257 supports two address spaces, memory space and I/O space, each with a maximum address range of 16 Mbytes. In addition, the maximum block length (byte count) is also 16 Mbytes to support applications where large blocks of data have to be transferred (e.g. graphics).

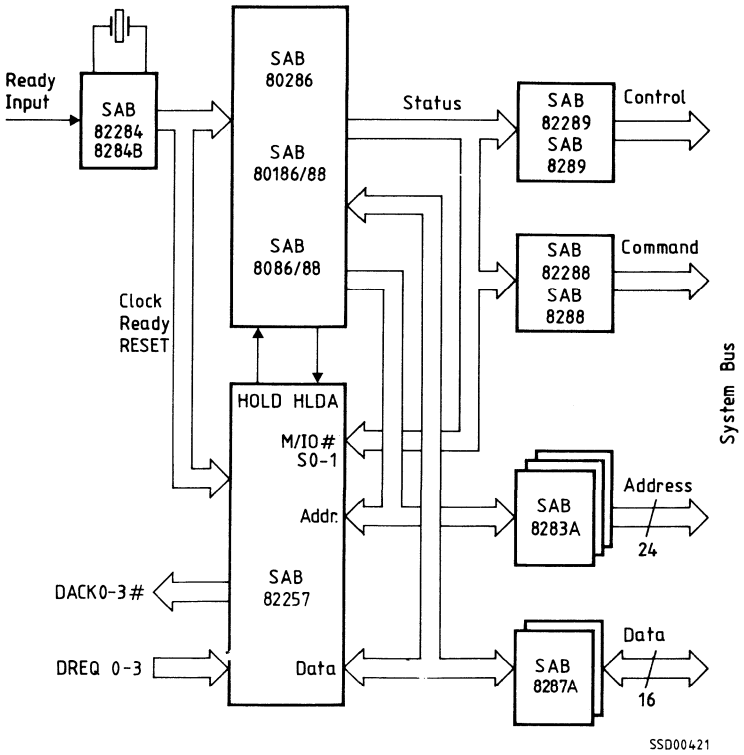
As source or as destination, four parameters can be selected independently:

- address space (memory or I/O)
- physical bus width (8 bits or 16 bits)
- logical bus width (same as physical bus width or 8 bits on a 16-bit physical bus) and
- transfer direction (increasing, decreasing, fixed pointer or constant value).

If the physical bus width of source or destination differs from the logical bus width, an automatic byte/word assembly (word/byte disassembly) takes place. The same is true, if the logical bus widths of source and destination are not identical.

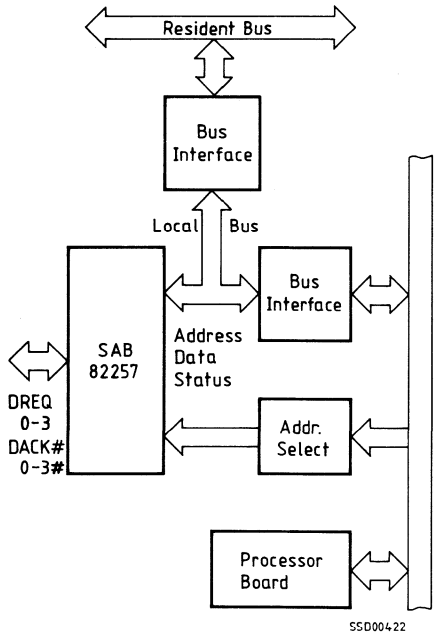
Basic SAB 82257 Operating Modes

a) Local Mode



Basic SAB 82257 Operating Modes

b) Remote Mode

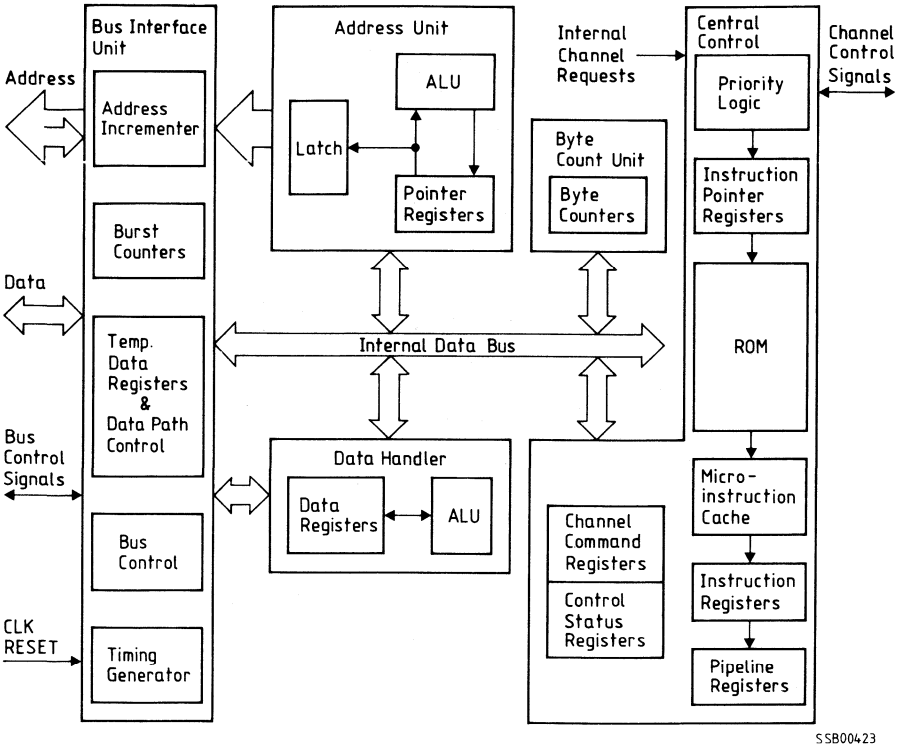


Transfers between different address spaces can be performed within one or two cycles, transfers within one address space can be performed only in two cycles.

The transfers can be executed free running or externally synchronized via DREQ where source or destination synchronization is possible.

In summary, this very symmetrical operation of the SAB 82257 gives the user a great amount of design flexibility.

Block Diagram of the SAB 82257



Adaptive Bus Interface

As shown in the figure on page 4, the SAB 82257 bus interface has two basic timing modes: the 286 mode and the 186 mode. In 286 mode the SAB 82257 is directly coupled to an SAB 80286, in 186 mode to an SAB 80186 or SAB 80188. For each of these two modes a slightly different variation exists:

- For the 286 mode the variation is the remote mode, where the SAB 82257 operates as a bus master on the system bus without being directly coupled to a processor. In this mode the SAB 82257 can utilize its own local bus and the communication with the main processor is done via the system bus. To enable access to SAB 82257 registers by the main processor, the SAB 82257 must release its local bus. This "local bus arbitration" in remote mode is done via the CS# and BREL lines.
- For the 186 mode the variation is the 8086 mode, where the SAB 82257 supports the RQ#/GT# protocol and thus can be directly coupled to an SAB 8086 or SAB 8088.

Memory-Based Communication

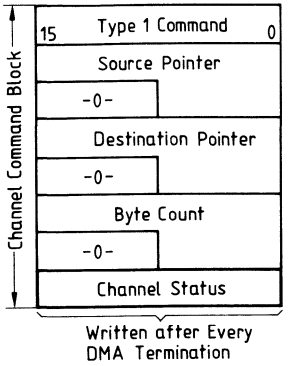
The normal communication between the SAB 82257 and the processor is memory-based. This means that all necessary data for a transfer is contained in a command block in memory accessible for CPU and SAB 82257 (see figure below). To start the transfer the CPU loads one of the command pointer registers of the SAB 82257 with the address of the command block and then issues a "start channel command". Getting the command the SAB 82257 loads the entire command block from memory into its on-chip channel registers and executes it. On completing the operation, channel status information is written back by the SAB 82257 into the channel status word contained in the command block in memory.
The command block structure of the SAB 82257 is identical with the structure of the SAB 82258A short command blocks. This allows to portate SAB 82257 software to the SAB 82258A and vice versa (in thise case with restrictions).

Command Chaining

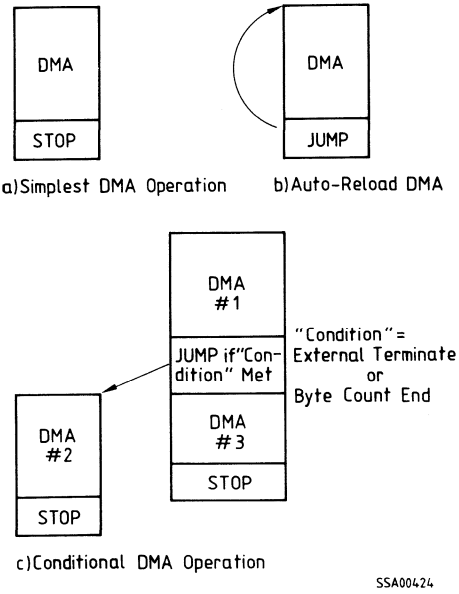
Command blocks for any channel can be chained for sequential execution (see figure). When the SAB 82257 has completed the execution of a command, it automatically increments the command pointer and starts to fetch and execute the next command block until a stop command is found. As a result a chain of command blocks can be executed by the SAB 82257 without any CPU intervention. Due to conditional and unconditional STOP and JUMP commands, quite complex sequences of DMA can be executed by the SAB 82257.

Memory-Based Communication and Command Chaining

Memory-Based Communication



Command Chaining



Data Chaining

Data chaining allows an automatic, dynamic linking of data blocks scattered in memory. There are two types: list and linked-list data chaining.

If for a DMA the source blocks are to be dynamically linked during DMA, it is called source chaining and the effect is that of gathering data blocks and sending them out effectively as one block.

If one source block is dynamically broken up into multiple destination blocks, it is called destination chaining. This results in scattering of a block.

This dynamic linking and unlinking of data blocks makes the logical sequencing of data independent of its physical sequencing in memory.
In the case of linked list chaining (see figure a) each data block has a descriptor containing information on position of the data block in memory, length of the data block and a pointer to the next descriptor.

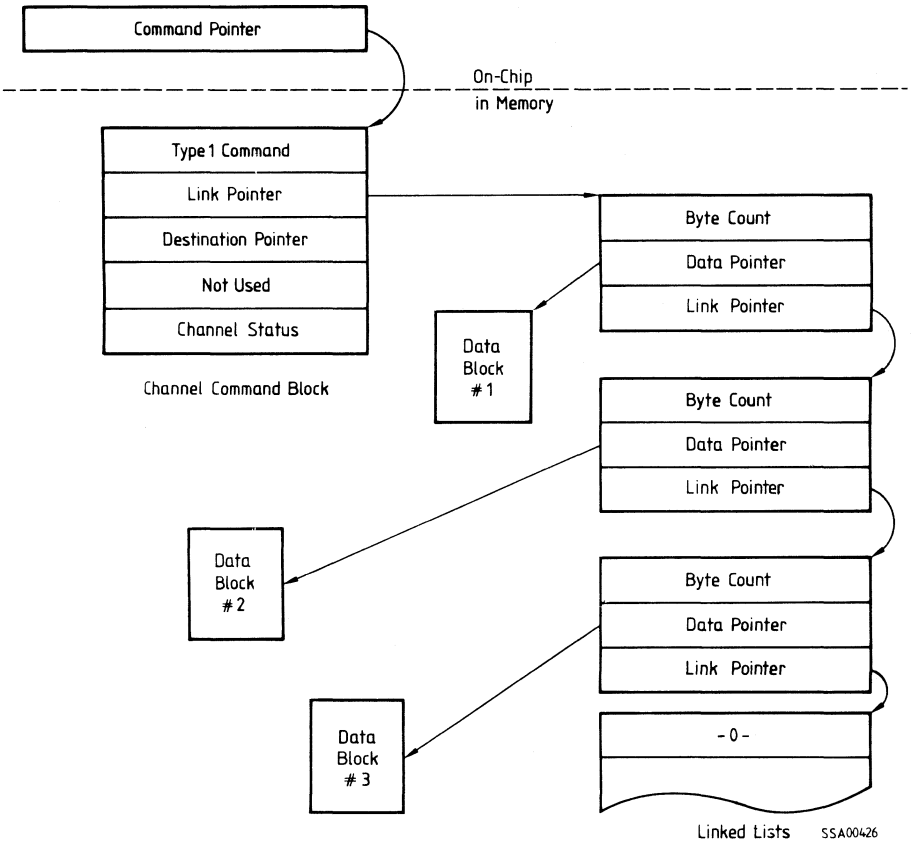
During data transfer the data block 1 is sent out first, then 2 and so on till a "0" is encountered in the byte count field.

The second type of data chaining is list chaining (see figure b).

Unlike linked list chaining, here the data block descriptors are continuous in a block and thus determine the sequence of data blocks. The flexibility lost in terms of predefined sequence is gained in terms of linking time.

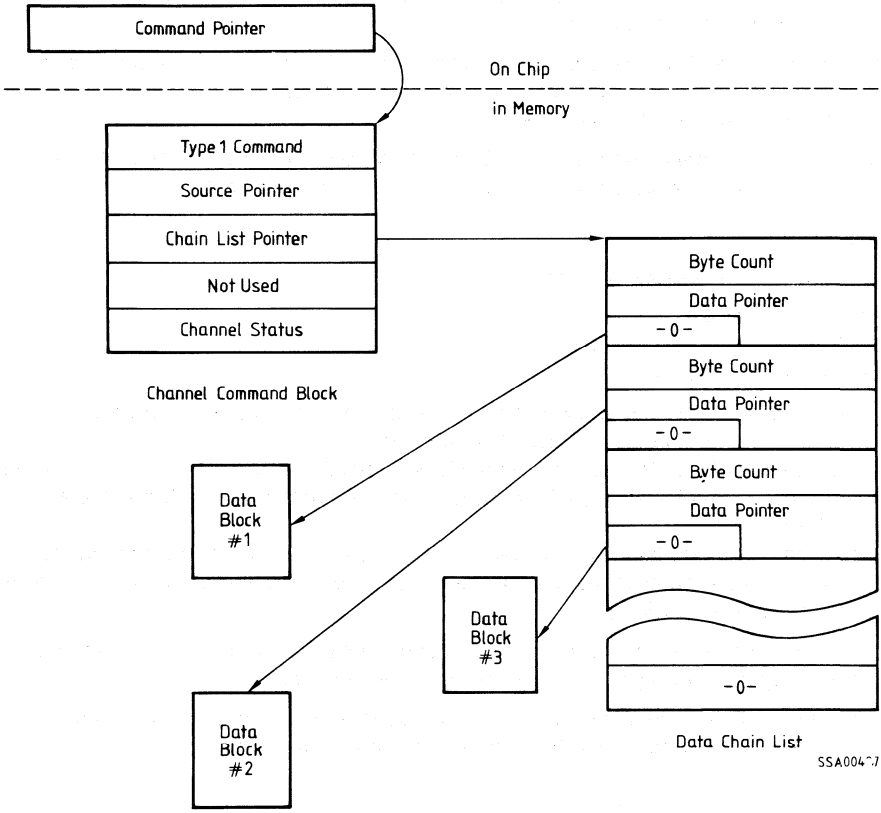
Data Chaining

a) Linked List Chaining



Data Chaining

b) List Chaining



Operating the SAB 82257

Reset

When activating the reset input, the SAB 82257 is forced into its initial state. All channels and bus activities are stopped, tristate lines are tristated and the others enter the inactive state. While the reset input is active, pin 57 must be held high and lines A23/AREADY and HLDA must be forced to the appropriate levels to select the desired bus interface mode (see figures on page 4, 41 and 52).
After deactivating reset the inactive state is maintained, in addition the state of the SAB 82257 registers is as follows:

- general mode register, general burst register, general delay register, general status register and the four channel status registers are set to zero,
- all other registers and bits are undefined.

Note: The general mode register (GMR) should be loaded first to select the mode of operation before any other activity is started on the SAB 82257.

DMA Interface

The DMA interface consists of three lines:

- DREQ – DMA request
- DACK# – DMA acknowledge and
- EOD# – End of DMA

The first two lines work as request and acknowledge lines to control synchronized DMA transfers as known from conventional DMA controllers.
A special feature of the SAB 82257 are the bidirectional EOD# lines . Firstly they can be used as inputs to receive an asynchronous external terminate signal to terminate a running DMA.
Secondly, as an output, they can be used to send out a pulse which interrupts the CPU and/or signals to the peripheral a specific status (e.g. transfer aborted, or end of a block, or send/receive next block ...).

The EOD# output signal can be generated synchronously to a transfer (during the last transfer) or asynchronously to the transfers by a specific command.

In addition the EOD# output of channel 2 can be used as a collective interrupt output for all DMA channels while the other three retain their normal function.

Slave Interface

The slave interface is used to access the SAB 82257 internal registers. Although nearly all of the communication between CPU and SAB 82257 is done via memory-based data blocks, some direct accesses to SAB 82257 registers are necessary.
For example during the initialization phase the general mode register must be written, or to start a channel the command pointer register and the general command register must be loaded. Also during the debugging phase it is of great benefit to have access to all of the SAB 82257 internal registers.

The slave interface is enabled by the CS# input and consists of the following lines:

- S0#, S1# – status lines (inputs)
- RD#, WR# – control lines (inputs)
- A0-A7 – register address (inputs)
- D0-D15 – data lines (inputs/outputs) or
- AD0-AD15 – data lines (inputs/outputs) for synchronous access in 186 mode

Note that all of these lines are outputs, if the SAB 82257 is an active bus master.

In 186 mode and 286 mode two types of accesses are possible:

- Synchronous access by means of the status lines. Processor and SAB 82257 are directly coupled and must use the same clock.
- Asynchronous access by using the control lines RD# and WR# (processor and SAB 82257may have different clocks).

In all modes except the synchronous access in 186 mode the register address must be supplied on address pins A0 to A7. Using synchronous access in 186 mode the address information is expected at address/data lines AD0 to AD7.
In remote mode only the asynchronous access is possible because the SAB 82257 first has to release its local bus to enable the register access. On receiving an access request (activation of CS# input) the SAB 82257 releases its local bus as soon as possible and signals this by activating the BREL line. Now the CPU can accomplish its access.

Bus Arbitration

To arbitrate access to the bus between the SAB 82257 and the processor, the signals HOLD and HLDA serve for communication. Normally the SAB 82257 competes for the bus via HOLD, the processor grants access to the bus via HLDA. The HLDA signal can also be deactivated in order to force the SAB 82257 off the bus for a certain reason (kick off). After reactivation of HLDA, the SAB 82257 will again get control of the bus.
In 8086 mode this communication is done by pulses via a single RQ#/GT# line which uses the HOLD pin. In this case normally the HLDA input has no function. Nevertheless, even in 8086 mode the HLDA input can be used for kick-off. This provides some kind of additional bus arbitration.

Register Set

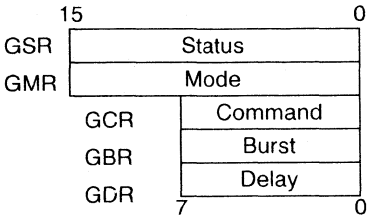
The following figure shows the user visible registers of the SAB 82257. A set of 5 registers, called the general registers, is used for all of the 4 channels. The mode register is being written to first after reset and it describes the SAB 82257 environment – bus widths, priorities, etc.

The general command register (GCR) is used to start and stop the DMA transfer on different channels. The general status register (GSR) shows the status of all of the 4 channels; if the channel is running, if interrupt is pending, etc. General burst register (GBR) and general delay register (GDR) are used to specify the bus load which is permissible for the SAB 82257.

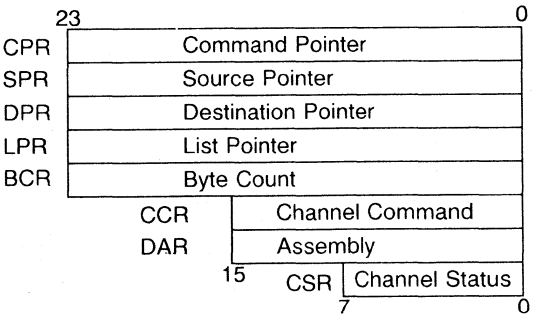
There is a set of channel registers for each of the 4 channels. Most channel registers serve as cache registers and need to be accessed only for debugging. During normal operation they are loaded automatically by the SAB 82257 (see next paragraph).
The layout of register addresses shown in the figure on the next page. All register addresses are even. Locations not designated in that figure are reserved and should not be used.

SAB 82257 Register Set

General Register



Channel Register (4 sets; 1 per channel)



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Register Address Arrangement

Address Bits 0-5	Address Bits 7, 6			
	00	01	10	11
0	GCR			
2				
4	GSR			
6				
8	GMR			
A	GBR			
C	GDR			
E				
10	CSR 0	CSR 1	CSR 2	CSR 3
12	DAR 0	DAR 1	DAR 2	DAR 3
14				
16				
18				
1A				
1C				
1E				
20	CPR L0	CPR L1	CPR L2	CPR L3
22	CPR H0	CPR H1	CPR H2	CPR H3
24	SPR L0	SPR L1	SPR L2	SPR L3
26	SPR H0	SPR H1	SPR H2	SPR H3
28	DPR L0	DPR L1	DPR L2	DPR L3
2A	DPR H0	DPR H1	DPR H2	DPR H3
2C				
2E				
30	LPR L0	LPR L1	LPR L2	LPR L3
32	LPR H0	LPR H1	LPR H2	LPR H3
34				
36				
38	BCR L0	BCR L1	BCR L2	BCR L3
3A	BCR H0	BCR H1	BCR H2	BCR H3
3C	CCR L0	CCR L1	CCR L2	CCR L3
3E	CCR H0	CCR H1	CCR H2	CCR H3

GCR = General Command Register
GSR = General Status Register
GMR = General Mode Register
GBR = General Burst Register
GDR = General Delay Register
CSR = Channel Status Register
DAR = Data Assembly Register

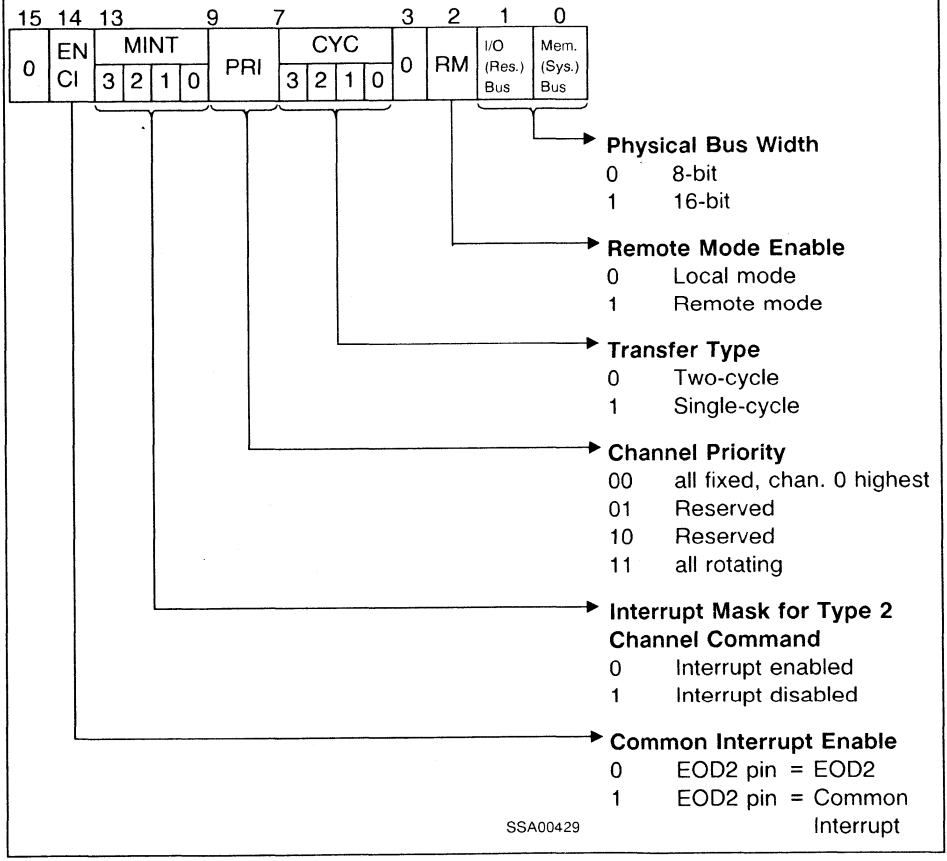
CPR = Command Pointer Register
SPR = Source Pointer Register
DPR = Destination Pointer Register
LPR = List Pointer Register
BCR = Byte Count Register
CCR = Channel Command Register

Register Description

General Mode Register

In the general mode register GMR (figure below) the system wide parameters are specified. This register should be programmed first after reset, with an 8-bit bus program low byte first.

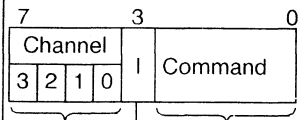
General Mode Register (GMR)



General Command Register

Individual channels are started and stopped by a command written to the general command register GCR (figure below). The GCR is directly loaded by the CPU.

General Command Register



Channel Command

000	NOP	
001	CONTINUE	Channel(s) after it has been stopped by the STOP command
010	START	Channel(s) = Command block at system/memory space
011	START	Channel(s) = Command block at resident I/O space
100	STOP	Channel(s)
101	---	Reserved
110	---	Reserved
111	HALT	Single-step channel(s): Start execution and stop before next command block will be loaded

Interrupt Command

0	NOP
1	Clear interrupt(s) of channel(s)

Channel Select

0	Channel not effected
1	Command refers to this channel

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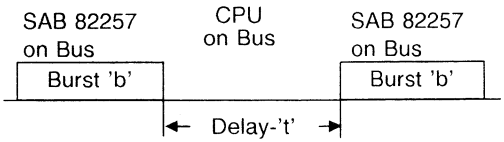
General Burst and Delay Register

It is possible to restrict the bus load generated by the SAB 82257 on the CPU bus by programming the burst and the delay register. The bus load is defined by the formula given in figure a) below. The factor b (burst) is programmed in the general burst register GBR, t (delay time) in the general delay register GDR (see figures b and c). Since the SAB 82257 can also execute locked bus cycles, the maximum burst length consists of b + 3 (8-bit bus) or b + 2 (16-bit bus) bus cycles. GBR and GDR must be directly loaded by the CPU. Loading GBR with 0 leads to no bus load limitations for the SAB 82257 (default after reset).

General Burst and Delay Register

a) Bus Loading

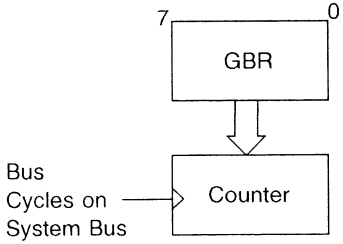


$$\text{Bus Load due to the SAB 82257} = \frac{b}{b+t}$$

b) General Burst Register (GBR) – to Program 'b'

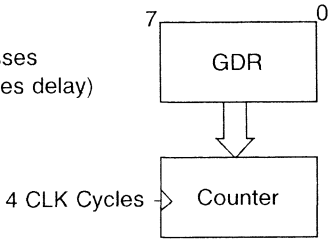
Determines max. number of contiguous bus cycles from the SAB 82257

If GBR = 0, No Limit



c) General Delay Register (GDR) – to Program 't'

Determines min. number of clock cycles between burst accesses (default after reset = 0,i.e. 4 T-states delay)



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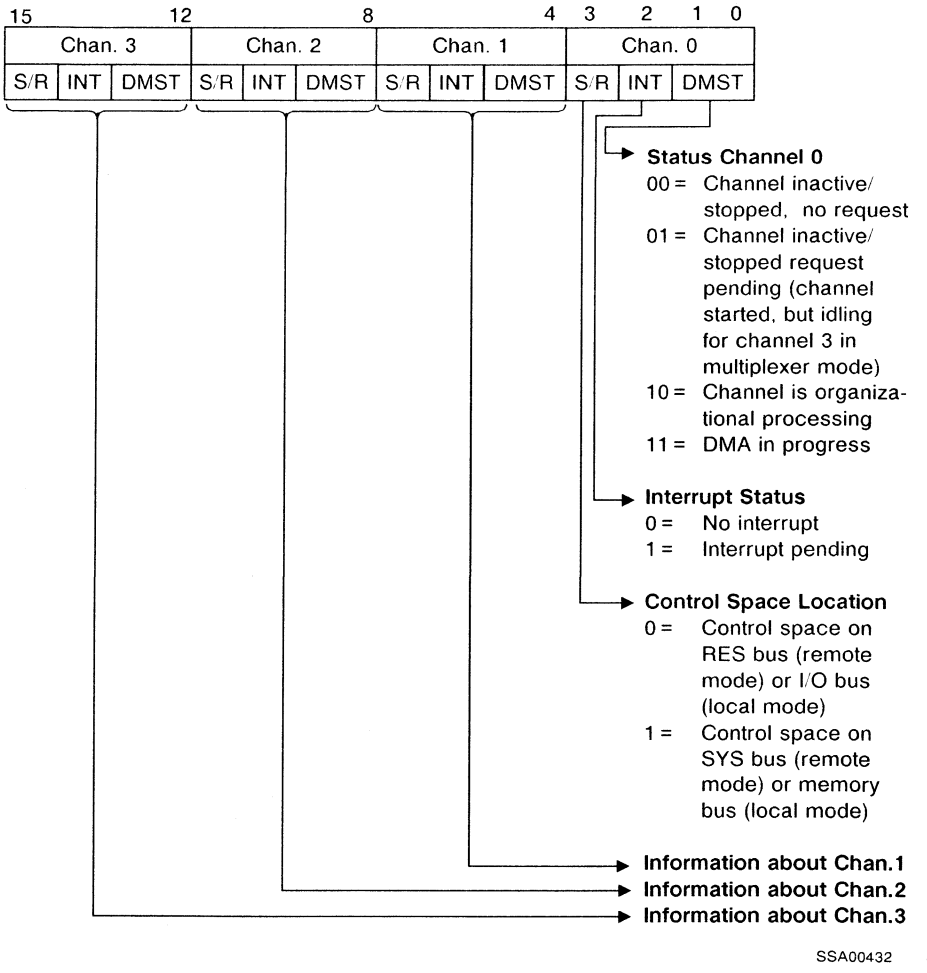
General Status Register

The general status register GSR (figure below) shows the current status of all the channels.

General Status Register (GSR)



Channel Commands

The channel commands are contained in the channel command block. 15 bits are used to specify the command. There are two types of channel commands:

- Type 1: for data movement
- Type 2: for command chaining control

The command block for a type 1 command is 16 bytes long (see figure „Memory based Communication").

The type 1 command fields (see figures below) contain information on:

a. Bus width of source and destination
b. If source and/or destination address should be incremented or decremented or kept constant during the transfer
c. If source/destination is in memory or I/O space (local mode) or in system or resident space (remote mode)
d. If data chaining (list or linked-list) is to be performed
e. If the data transfer is synchronized (source or destination)

Type 2 command blocks are 6 bytes long (see figure „Type 2 Command Block") of which the first 2 bytes form the command and the rest is either a relative displacement or an absolute address for the JUMP operation. There are two basic type 2 commands (see figure „Type 2 Command Block"):

a. JUMP – conditional and non-conditional
b. STOP – conditional and non-conditional

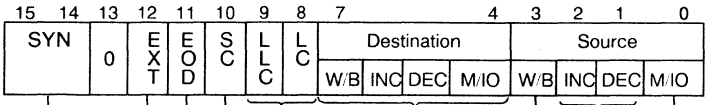
The conditional case tests for either of the 2 condition bits which are altered at the termination of any DMA operation:

- Termination due to byte count end
- Termination due to external terminate.

It is thus possible to JUMP or STOP further execution of commands based on any of these conditions and optionally generate an EOD# or interrupt signal.

The combination of type 1 and 2 commands gives the SAB 82257 a high degree of "programmability". It can thus execute quite complex algorithms with a fairly low demand for CPU service.

Type 1 (DMA) Channel Command



Source Description

Associated Space
0 I/O or resident
1 Memory or system

Source Pointer
00 Printer not modified
01 Decrement pointer
10 Increment pointer
11 No pointer (constant value)

Logical Bus Width
0 8-bit
1 16-bit

Destination Description
Same as source description

Data Chaining
LLC LC
0 0 No chaining
0 1 List chaining
1 0 Link list chaining
1 1 Not allowed

Select Chaining
0 Destination data chaining
1 Source data chaining

Enable EOD# Output

Enable External Terminate Input

Synchronization
00 Not valid(type 2 command)
01 Source synchronization
10 Destination synchronization
11 No synchronization (free running)

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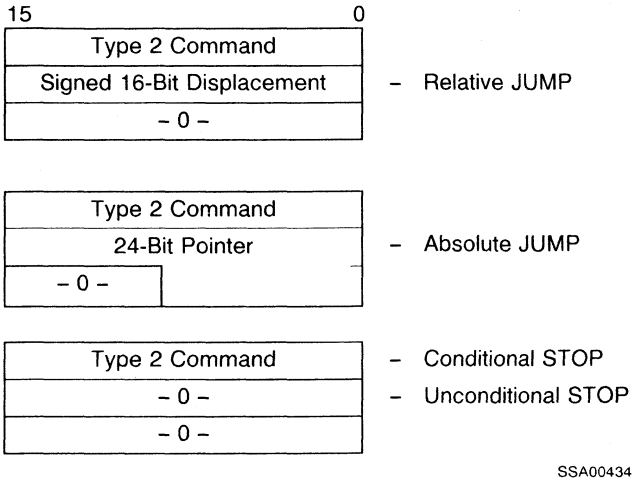
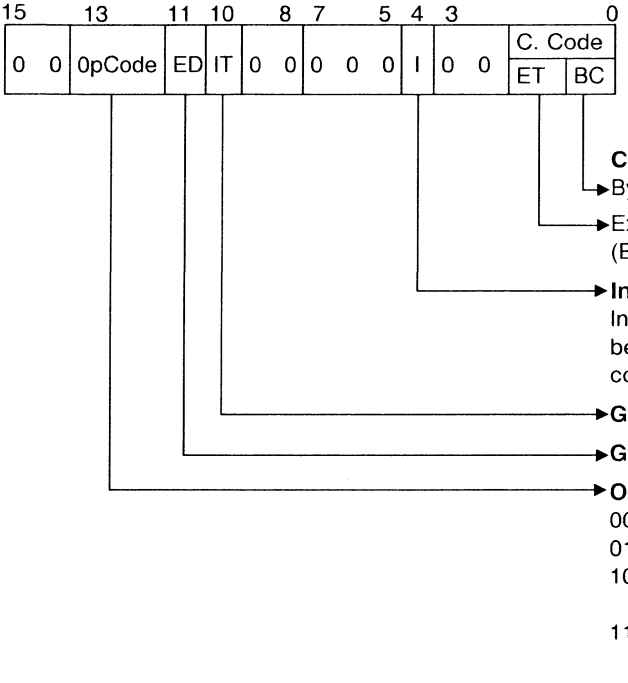
Type 2 Command Blocks (for command chaining control)



Type 2 Command Format



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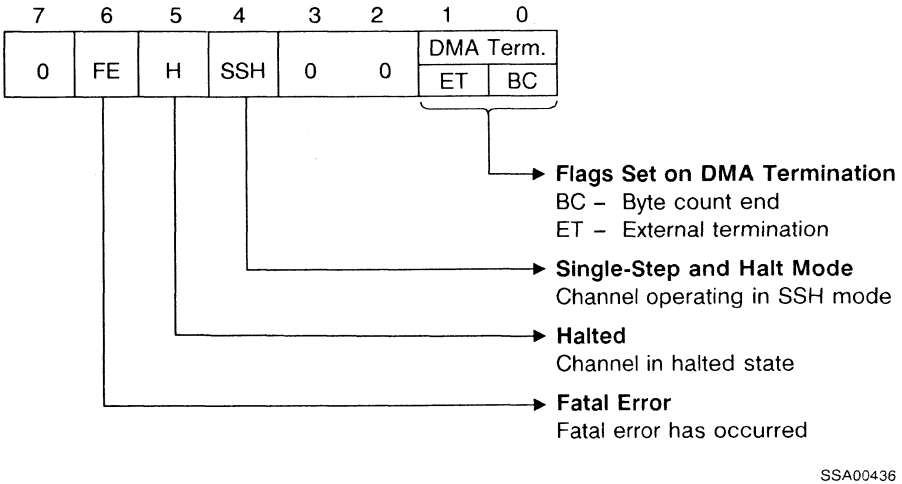
*) Unconditional JUMP when both condition code bits are set 1.

Channel Status Register

For each channel there is a channel status register (see figure below). This register shows the current state of the appropriate channel.

Channel Status Register



Timings

The bus timings in 286 and remote mode are identical to that for the SAB 80286, in 186 and 8086 mode the timings are identical to that for the SAB 80186. For exact timings see timing diagrams of AC Characteristics.

Asynchronous control inputs are specified with setup and hold times which are only important to determine whether the SAB 82257 responds to the signal in the current cycle or the next cycle.

The following pages hold two sections of AC characteristics and waveforms. The first section refers to 286 mode and remote mode, the second one to 186 mode and 8086 mode.

Absolute Maximum Ratings

Temperature under bias ..... 0 to 70°C
Storage temperature ..... – 65 to + 150°C
Voltage on any pin with respect to ground ..... – 0.5 to + 7 V
Power dissipation ..... 3.6 W

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics [1]

T_C = 0 to 100°C; V_{CC} = + 5 V ± 10%

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage (except CLK)	V_{IL}	– 0.5	+ 0.8	V	–
Input high voltage (except CLK)	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 3.0 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = – 400 µA
Power supply current	I_{CC}	– –	550 385	mA mA	T_C = 0°C, (turn on) T_C = 100°C (steady operation) all outputs open
Input leakage current	I_{LI}				
S0#, S1#, S2#, BHE#, RD#, WR#, M/IO#		–	– 200	µA	0 V ≤ V_{IN} ≤ V_{CC}
HOLD (RQ#/GT# mode), EOD#		–	–1.5	mA	0 V ≤ V_{IN} ≤ V_{CC}
A23 (AREADY), A21 [2]		–	–1.5	mA	0 V ≤ V_{IN} ≤ V_{CC}
other pins		–	± 10	µA	0 V ≤ V_{IN} ≤ V_{CC}
Output leakage current	I_{LO}	–	± 10	µA	0.45 V ≤ V_{OUT} ≤ V_{CC}
Clock input low voltage	V_{CL}	– 0.5	+ 0.6	V	–
Clock input high voltage	V_{CH}	3.8	V_{CC} + 1.0	V	–

1) Clock must be applied.
2) This specification is valid only during RESET.

Capacitance

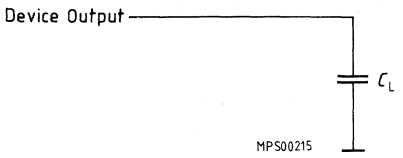
$T_C = 25°C$; V_{CC} = GND = 0 V, $f_c = 1$ MHz

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Capacitance of inputs (except CLK)	C_{IN}	–	10	pF	3)
Capacitance of I/O or outputs	C_{IO}	–	20	pF	3)
Capacitance of CLK input	C_{CLK}	–	12	pF	3)

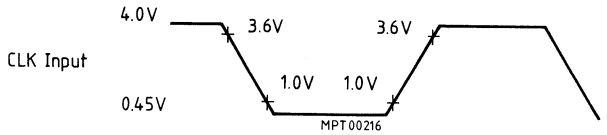
3) Not 100% tested, guaranteed by design characterization.

AC Testing Waveforms

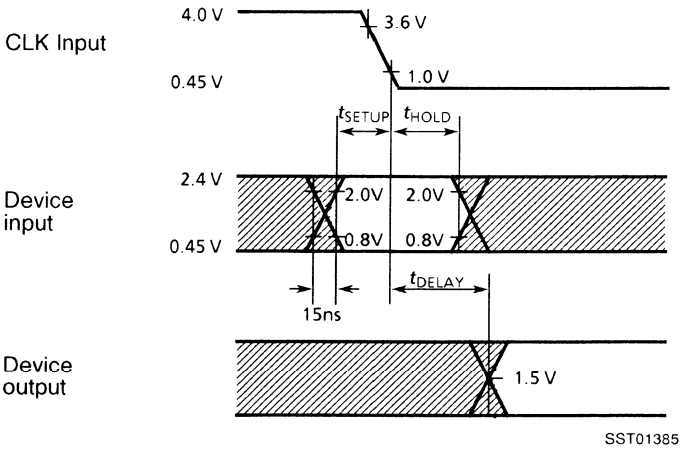
Test Loading on Outputs



Drive and Measurement Points – CLK Input



Setup, Hold and Delay Time Measurement – General



AC Characteristics SAB 82257 (286 mode)

T_C = 0 to 100°C; V_{CC} = +5 V ±10%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
CLK cycle period	t_1	62	250	ns	–
CLK low time	t_2	15	230	ns	at 1.0 V
CLK high time	t_3	20	235	ns	at 3.6 V
Address/control output delay	t_4	–	60	ns	C_L = 100 pF
Status output delay	t_5	–	40	ns	C_L = 100 pF
Sync data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync READY# setup time	t_8	38	–	ns	–
Sync READY# hold time	t_9	25	–	ns	–
Sync control input setup time	t_{10}	20	–	ns	–
Sync control/address input hold time	t_{11}	20	–	ns	–
Sync address setup time	t_{12}	2.5	–	ns	–
Data/control output delay	t_{13}	–	50	ns	C_L = 100 pF
Data/control float delay	t_{14}	–	50	ns	–
BHE# setup time	t_{15}	60	–	ns	–
Write command width	t_{16}	4CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	2CLK + t_6 + t_{44}	–	ns	–
Async address setup time	t_{18}	t_{43}	–	ns	–
Async data access time	t_{19}	–	5CLK + t_{43} + t_{13}	ns	–
Mode select setup time	t_{28}	2CLK + 20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Command recovery time	t_{33}	4CLK + t_{43} + t_{44}	–	ns	–

AC Characteristics SAB 82257 (286 mode) cont'd

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
CLK rise time	t_{34}	–	15	ns	1.0 to 3.6 V
CLK fall time	t_{35}	–	15	ns	3.6 to 1.0 V
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
CS# active response time	t_{37}	2CLK	20CLK + t_{43} + t_{44}	ns	1)
CS# active after BREL inactive	t_{39}	0	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async input setup time	t_{43}	20	–	ns	2)
Async input hold time	t_{44}	20	–	ns	2)
Async HLDA high time	t_{47}	2CLK + t_{43} + t_{44}	–	ns	3)
HOLD output low time	t_{49}	4CLK – t_{13}	–	ns	–
HLDA low to HOLD low delay	t_{50}	6CLK	20CLK + t_{43} + t_{13}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
CS# hold time	t_{56}	40	–	ns	–
DACK# output delay	t_{59}	–	50	ns	–

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- normal pointer transfer (3 bus cycles): 16 CLK
- splitted pointer transfer (4 bus cycles): 20 CLK

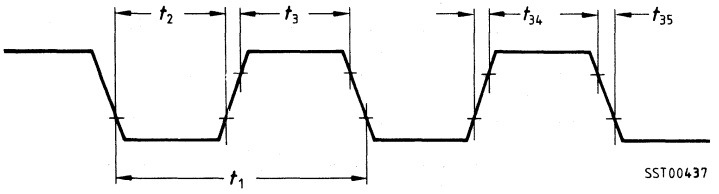
If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

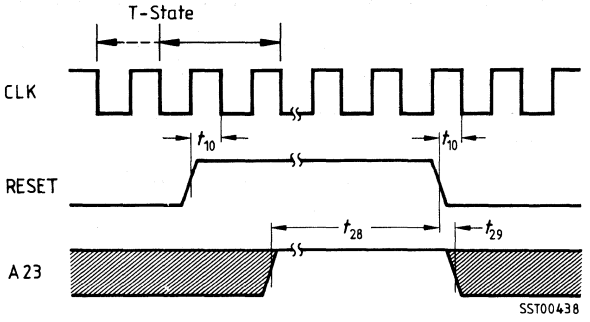
3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

Waveforms

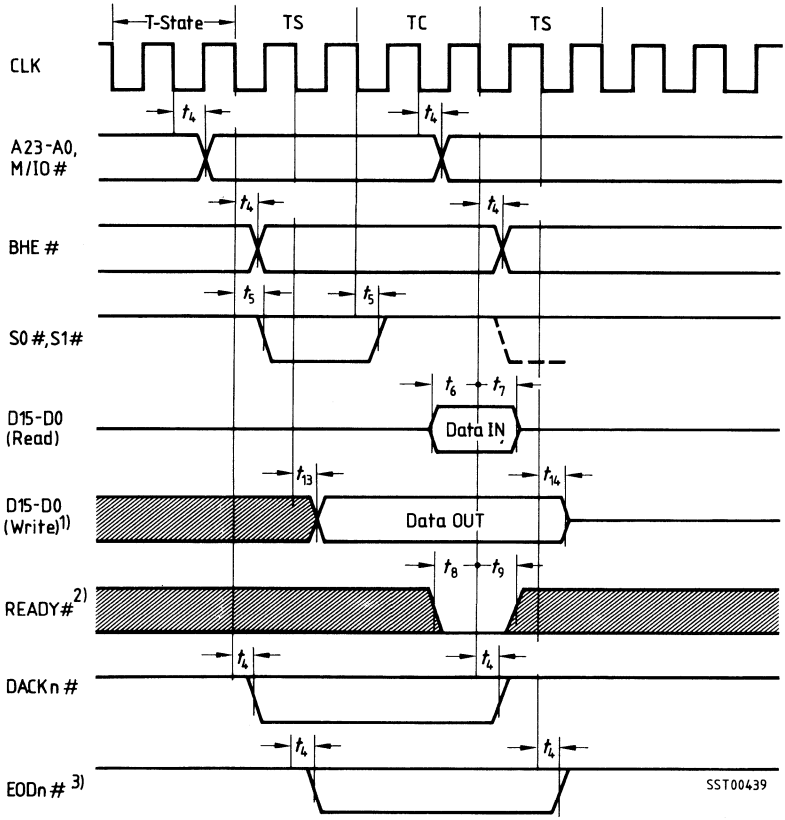
Clock Signal (286 mode)



Mode Selection on RESET (286 mode)

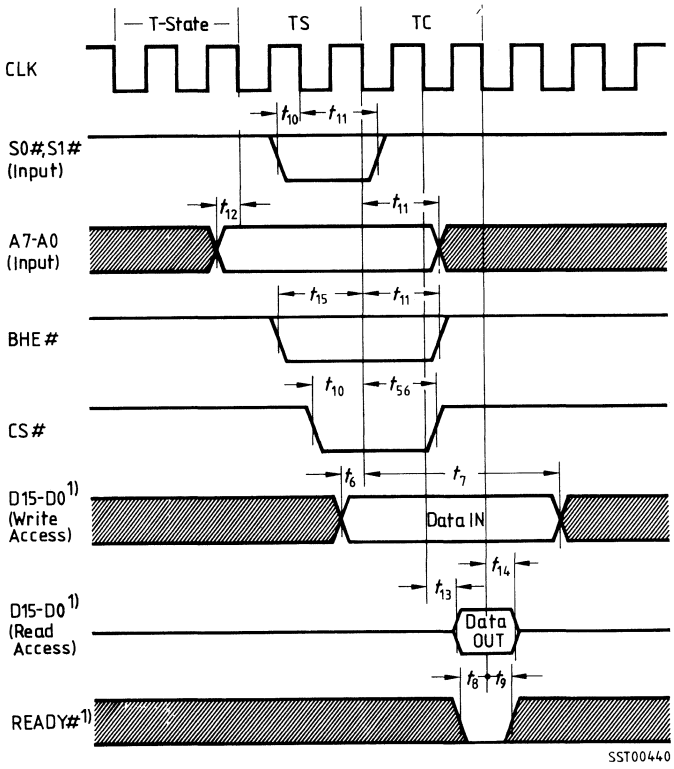


Major Timing for Active Bus Cycles (286 mode)



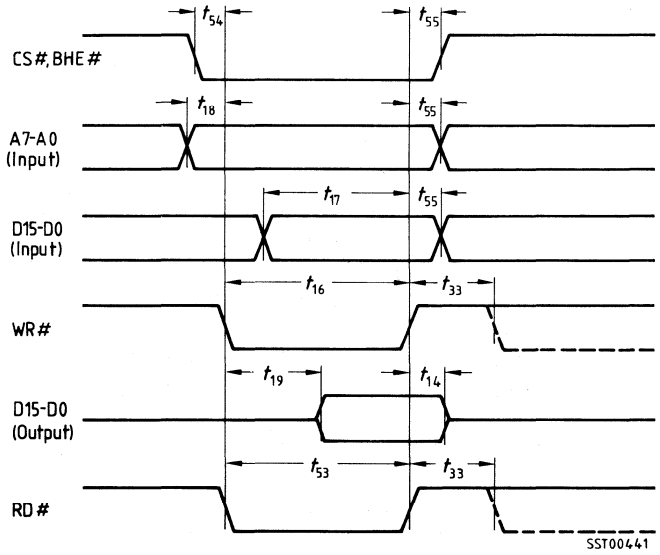
1) If executing a single cycle transfer, D15 to D0 float like during read cycles!
2) TC will be repeated, if READY# is inactive at the sampling point (end of current TC).
3) Initiated by terminal count.

Synchronous Access (286 mode)

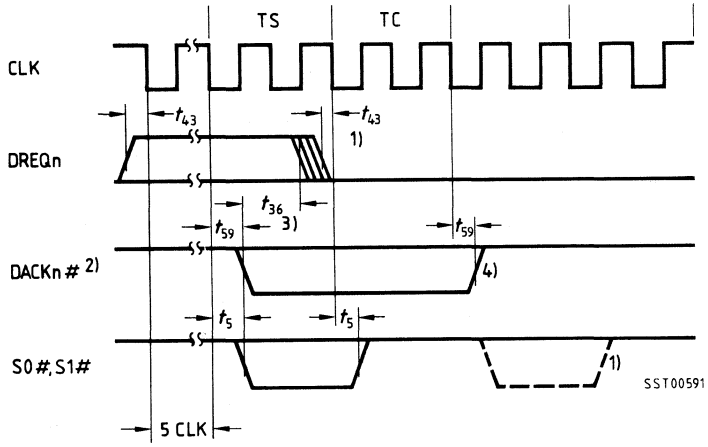


1) The processor will repeat TC, if READY# is not active at the sampling point (end of current TC). The SAB 82257 will output data until the end of the repeated TC (read access) or sample the data bus again at the beginning of the repeated TC (write access).

Asynchronous Access (286 mode)

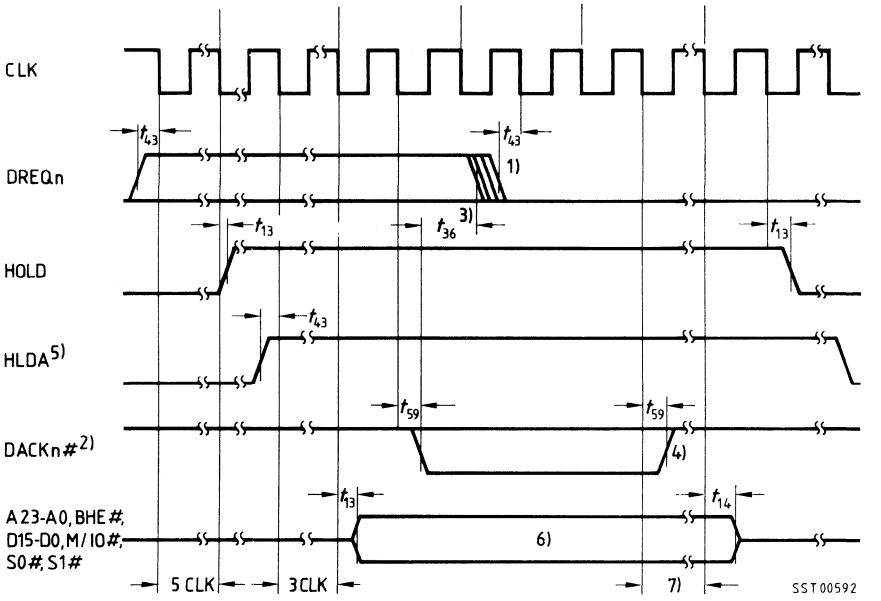


DMA Control Without Bus Arbitration (286 mode)



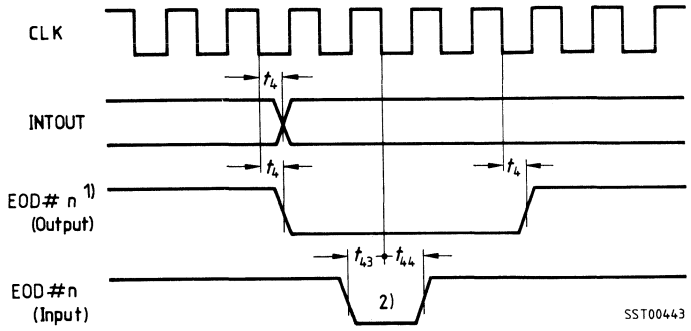
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) Minimum time to execute bus cycle.
4) If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

DMA Control With Bus Arbitration (286 mode)



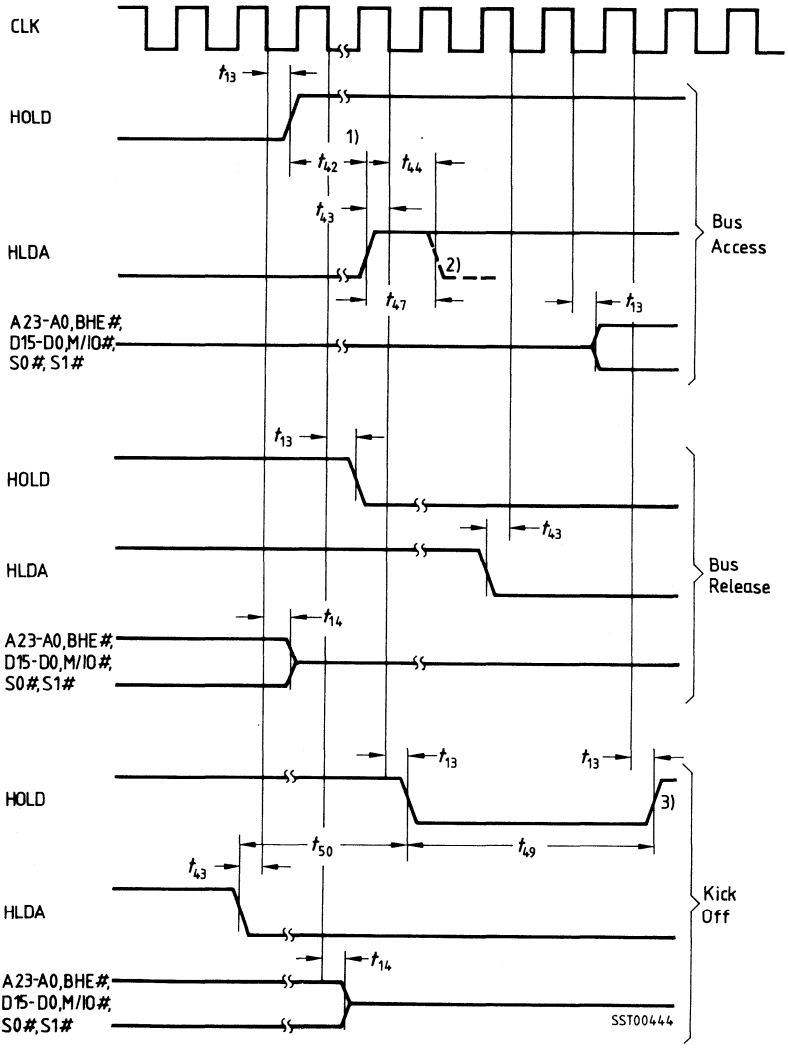
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) Minimum time to execute bus cycle.
4) If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.
5) The SAB 82257 can be forced off the bus by driving HLDA inactive (see "Bus Arbitration").
6) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycle".
7) The SAB 82257 may execute additional bus cycles, e.g. for command chaining.

EOD#/INTOUT Timing (286 mode)



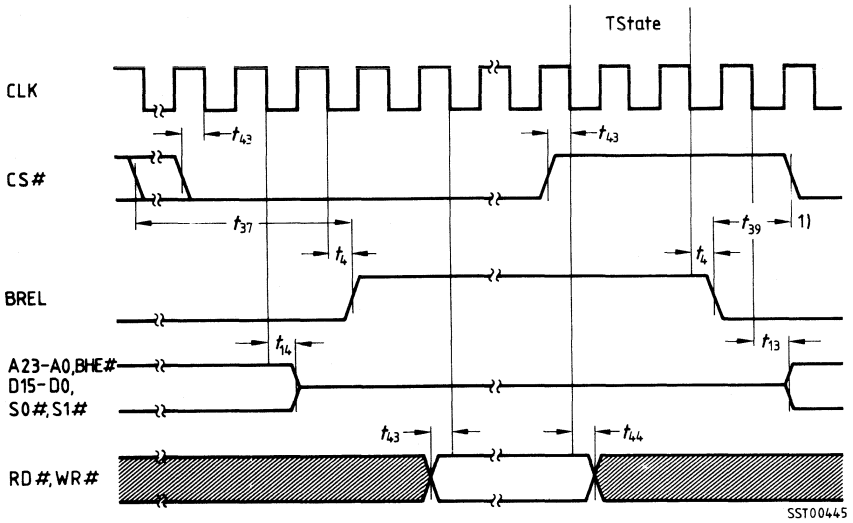
1) Initiated by type 2 command.
2) EOD# input minimum pulse width is 3 CLKs, if the signal is asynchronous.

Bus Arbitration (286 mode)



1) To avoid arbitration conflicts, HLDA should not become active before HOLD.
2) Minimum HLDA high time before kick-off to respond to HOLD signal.
3) Earliest possible reactivation of HOLD after deactivation of HLDA.

Access in Remote Mode



1) Required to avoid bus conflicts.

This diagram shows the times when the output signals are driven active and input signals are recognized, rather than the exact timing.

AC Characteristics SAB 82257 (186 mode)

T_C = 0 to 100°C; V_{CC} = +5 V ±10%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Control output delay	t_4	–	60	ns	–
Sync address/data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync control input setup time	t_{10}	20	–	ns	–
Sync control/address input hold time	t_{11}	20	–	ns	–
Data/control delay	t_{13}	–	50	ns	C_L = 100 pF
Data float delay	t_{14}	–	50	ns	–
Write command width	t_{16}	2CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	1CLK + 30	–	ns	–
Async address setup time	t_{18}	20	–	ns	–
Async data access time	t_{19}	–	2CLK + t_{22} + t_{43} + t_{13}	ns	–
CLK cycle period	t_{20}	125	500	ns	–
CLK low time	t_{21}	55	–	ns	at 1.5 V
CLK high time	t_{22}	55	–	ns	at 1.5 V
CLK rise time	t_{23}	–	15	ns	1.0 to 3.5 V
CLK fall time	t_{24}	–	15	ns	3.5 to 1.0 V
AREADY active setup time	t_{25}	20	–	ns	2)
AREADY hold time	t_{26}	15	–	ns	2)
AREADY inactive setup time	t_{27}	35	–	ns	–
Mode select setup time	t_{28}	2CLK + 20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Address/data output delay	t_{30}	10	50	ns	C_L = 20 to 200 pF
Status output delay	t_{31}	10	55	ns	–
Float delay	t_{32}	10	50	ns	–

AC Characteristics SAB 82257 (186 mode) cont'd

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Command recovery time	t_{33}	2CLK + t_{43} + t_{44}	–	ns	–
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
ALE output delay	t_{38}	–	40	ns	–
Address/control input hold time	t_{40}	10	–	ns	–
Address input setup time	t_{41}	20	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async control input setup time	t_{43}	20	–	ns	2)
Async control input hold time	t_{44}	20	–	ns	2)
HLDA hold time	t_{45}	10	–	ns	–
Async HLDA high time	t_{46}	1CLK + t_{43} + t_{45}	–	ns	3)
HOLD output delay	t_{48}	5	70	ns	–
HLDA output low time	t_{51}	2CLK – t_{48max}	–	ns	–
HLDA low to HOLD low delay	t_{52}	3CLK	16CLK + t_{43} + t_{48}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
SREADY hold time	t_{57}	15	–	ns	–
Status setup time	t_{58}	35	–	ns	–
DACK# output delay	t_{60}	–	60	ns	–
Status hold time	t_{61}	10			

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- normal pointer transfer (3 bus cycles): 12 CLK
- splitted pointer transfer (4 bus cycles): 16 CLK

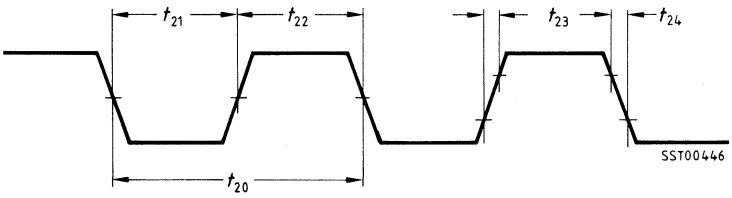
If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

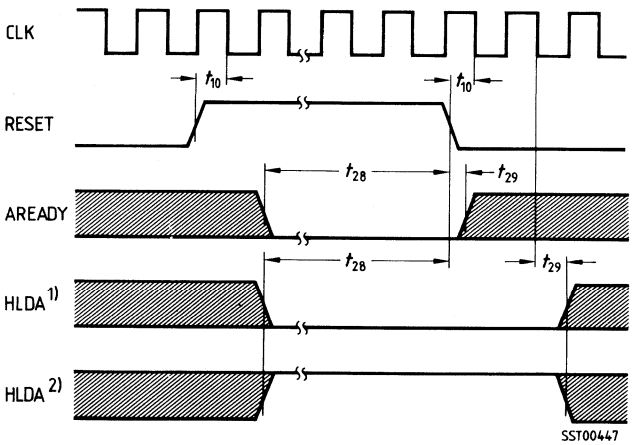
3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

Waveforms

Clock Signal (186 mode)

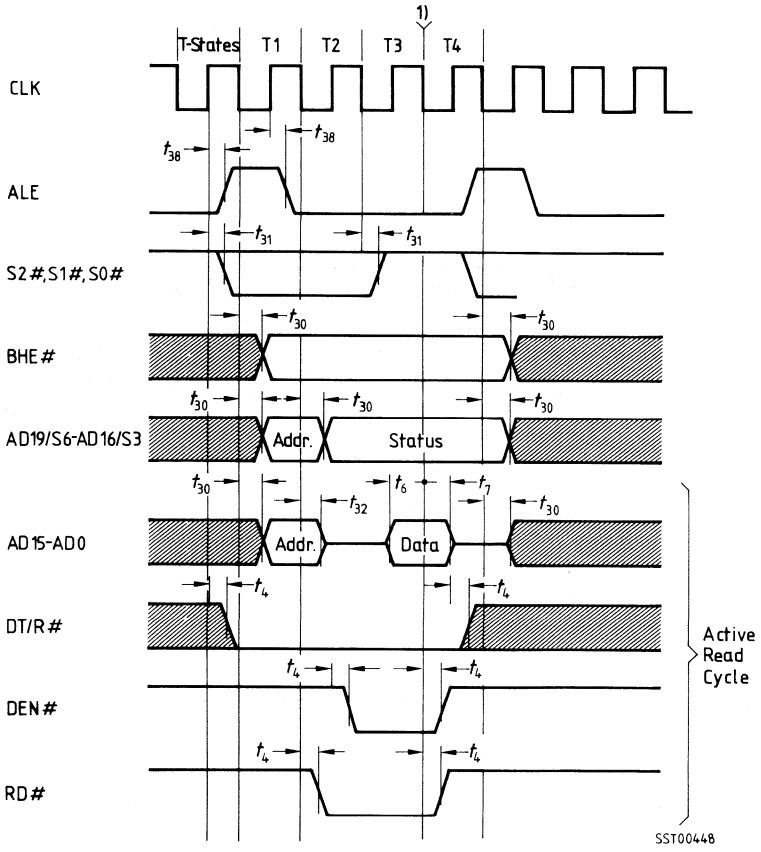


Mode Selection on RESET (186 mode)



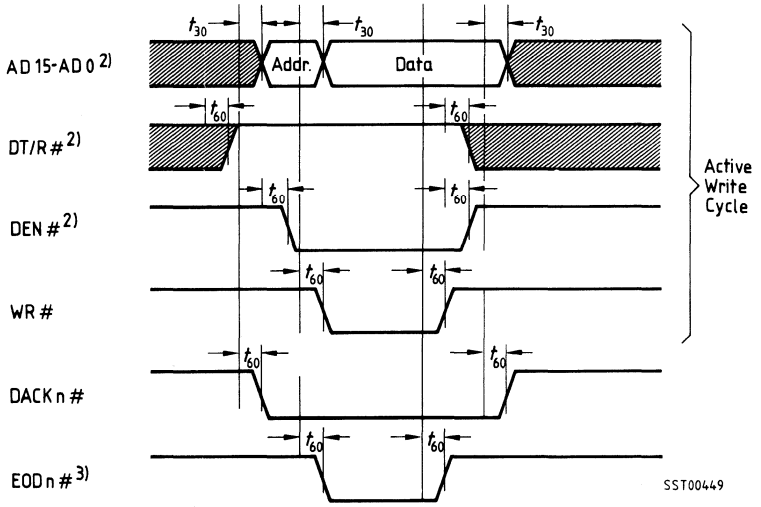
1) To operate in 186 mode with HOLD/HLDA protocol.
2) To operate in 8086 mode with RQ#/GT# protocol.

Major Timing for Active Bus Cycle (186 mode) a)



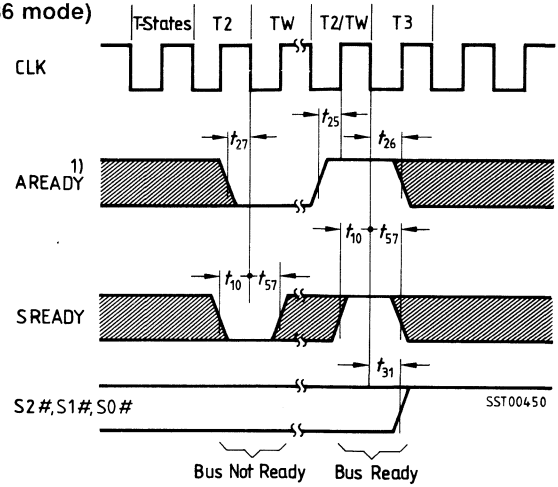
1) A wait state is inserted after T3 or TW, whenever the bus is not ready at the beginning of T3 or TW (see "Bus Cycle Termination"). The status must be valid just prior to T4.

Major Timing for Active Bus Cycle (186 mode) b)



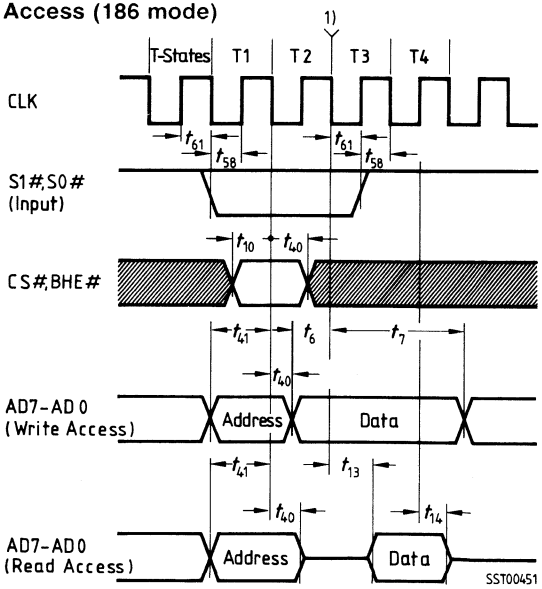
2) For a single-cycle transfer the timing of AD15-AD0,DT/R# and DEN# is identical to a read cycle. AD15-AD0 will float as during a read cycle.
3) Initiated by terminal count.

Bus Cycle Termination (186 mode)



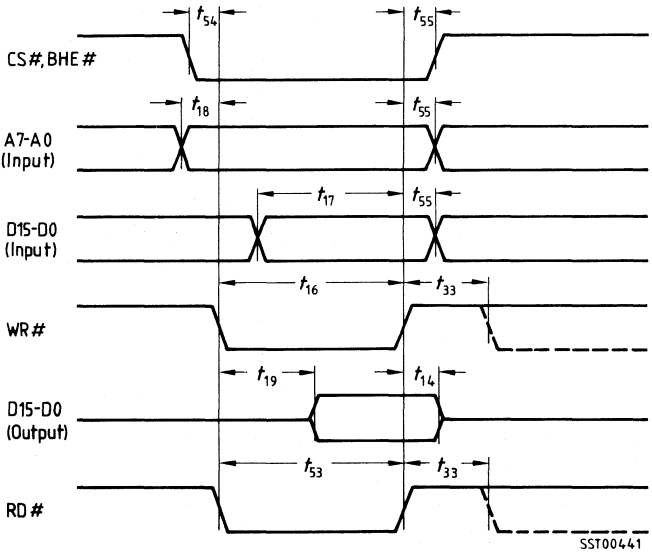
1) Only the rising edge of AREADY is synchronized internally to CLK. The falling edge must be synchronized externally.

Synchronous Access (186 mode)

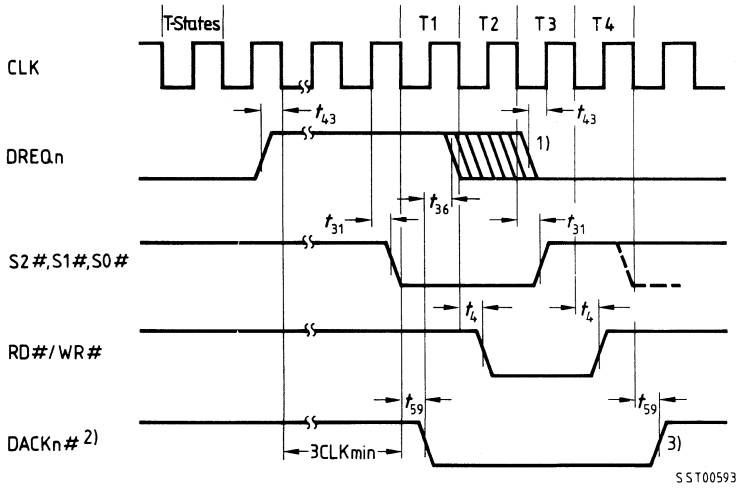


1) Additional wait cycles may be inserted. Status must be valid just prior to T4.

Asynchronous Access (186 mode)

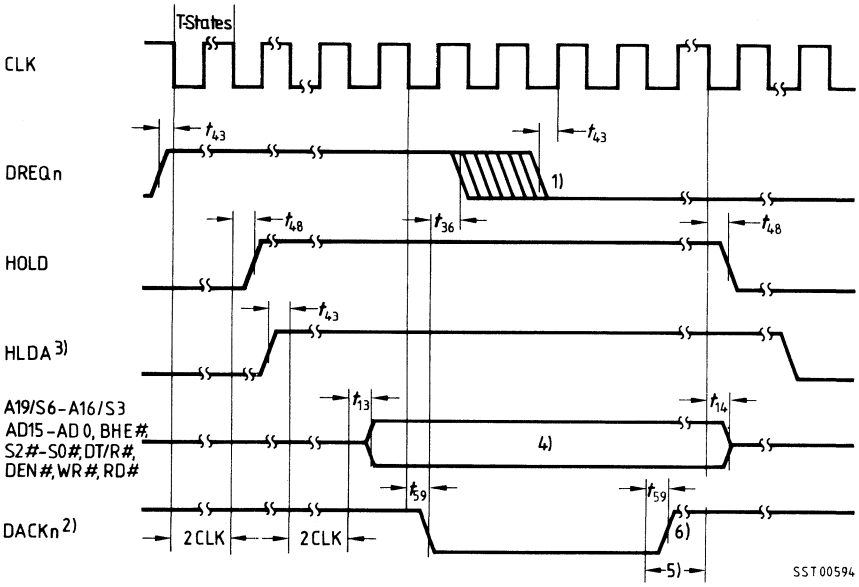


DMA Control Without Bus Arbitration (186 mode)



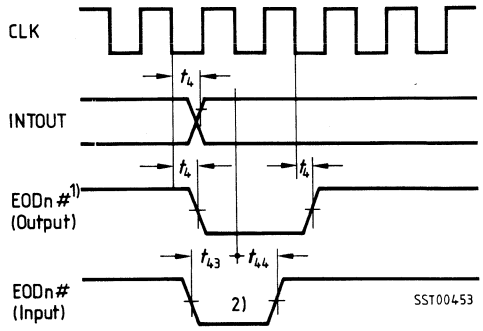
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

DMA Control With Bus Arbitration (186 mode)



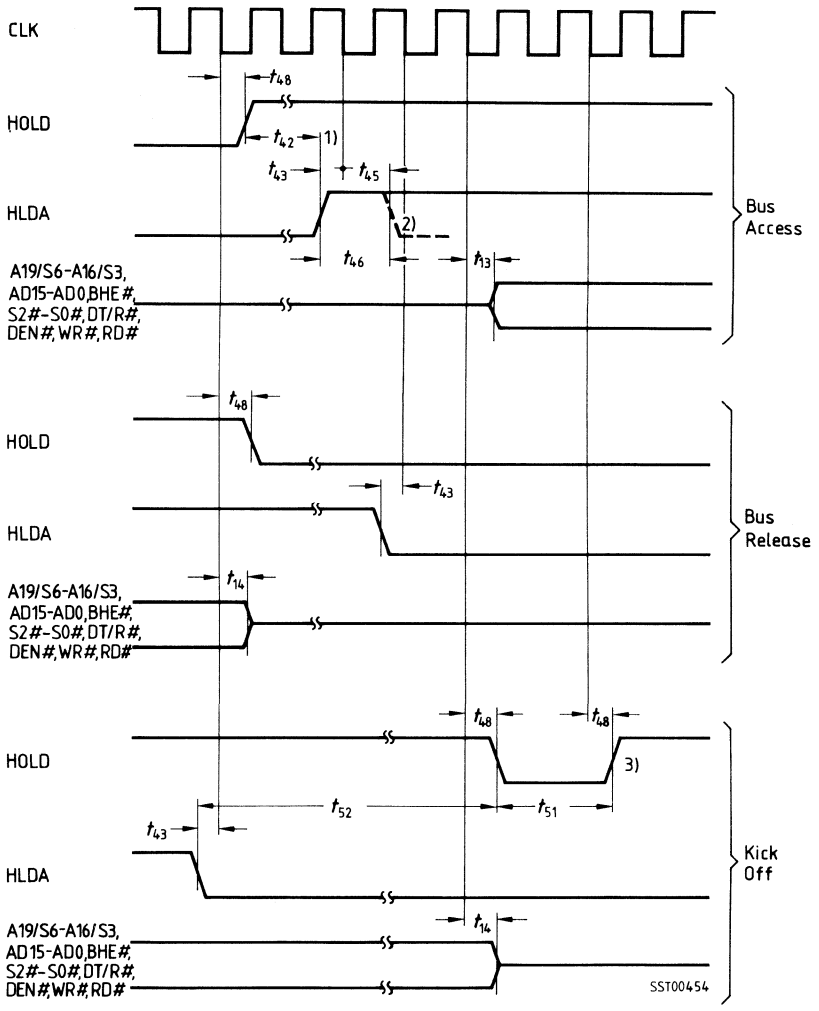
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) The SAB 82257 can be forced off the bus by driving HLDA inactive (see "Bus Arbitration").
4) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycle".
5) The SAB 82257 may execute additional bus cycles, e.g. for command chaining.
6) If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

EOD#/INTOUT Timing (186 mode)



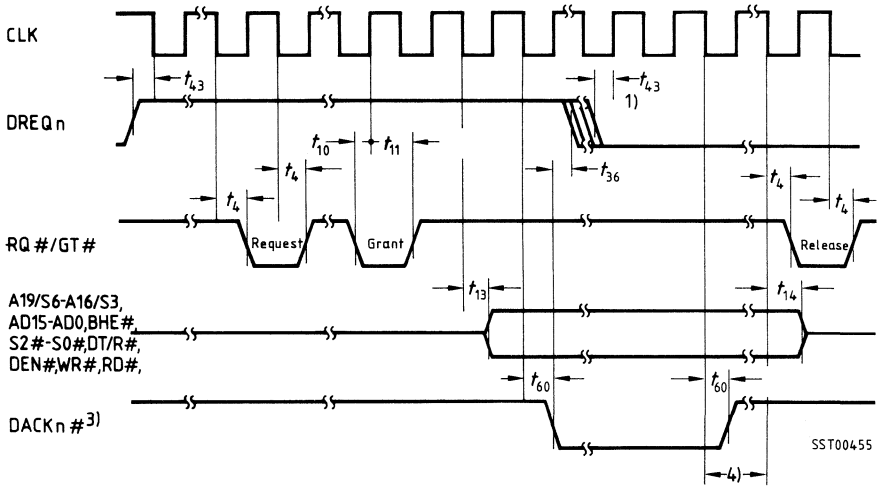
1) Initiated by type 2 command.
2) EOD# input minimum pulse width is 2 CLKs, if the signal is asynchronous.

Bus Arbitration (186 mode)



1) To avoid arbitration conflicts, HLDA should not become active before HOLD.
2) Minimum HLDA high time before kick-off to respond to HOLD signal.
3) Earliest possible reactivation of HOLD after deactivation of HLDA.

DMA Control with RQ#/GT# Protocol (8086 mode)



1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent bus cycles are executed.
2) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".
3) Refers to the highest priority request. Acknowledge of lower priority requests may be delayed by higher priority requests.
4) The SAB 82257 may execute additional bus cycles, e.g. for command chaining.

SIEMENS

Advanced DMA Controller SAB 82258A

for 16-/32-Bit Microcomputer Systems

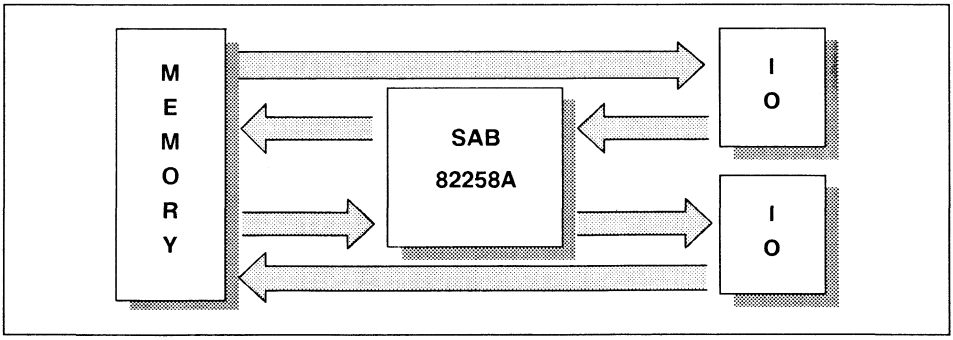
Advance Information

SAB 82258A **8 MHz**

- Fully upward-compatible with SAB 82258 (hardware and software)
- Supports 32-bit fly-by transfers
- 4 independent high-speed DMA channels
- Multiplexer channel operation supporting up to 32 subchannels
- Adaptive on-chip bus interface for direct connection to 16/8-bit processors
- Standalone operation for modular systems
- Programmable bus loading
- Transfer rates up to 20 Mbytes/s (10 MHz system)

SAB 82258A-1 **10 MHz**

- 16 Mbytes addressing range
- 16 Mbytes maximum block size
- Command chaining for automatic processing
- Automatic data chaining (scattering/gathering) for flexible data structures
- "On-the-fly" compare, translate and verify operations
- Single and double cycle transfers
- Automatic assembly/disassembly of data
- Memory-based communication scheme with CPU
- 3 package types: C-CC-68, C-PGA-68, and PL-CC-68



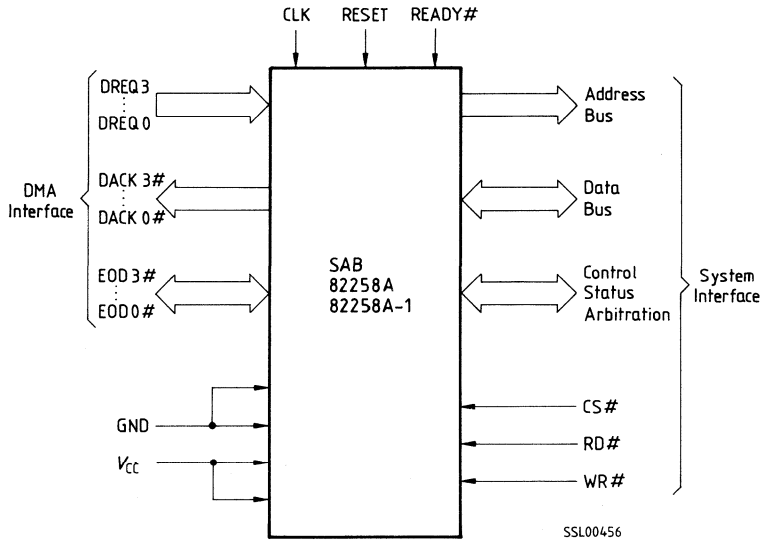
The SAB 82258A is an advanced DMA (direct memory access) controller especially designed for the 16-bit microprocessors SAB 80286 and SAB 8086/186/88/188. In addition the operation with other processors is supported by the remote mode. The 32-bit fly-by transfer mode supports operation with 32-bit microprocessors (like 80386). The SAB 82258A has 4 independent DMA channels which can transfer data at rates up to 10 Mbytes/second at 10 MHz clock frequency in an SAB 80286 system or up to 5 Mbytes/second at 10 MHz in an SAB 8086/80186 system. Using 32-bit fly-by transfers it can transfer 20 Mbytes/ second at 10 MHz. This great bandwidth allows the user to handle very fast data transfers or a large number of concurrent peripherals.

The device is fabricated in advanced +5 V N-channel Siemens MYMOS technology and comes in a 68-pin ceramic leadless chip carrier (C-CC-68), in a 68-pin ceramic pin grid array (C-PGA-68), or in a 68-pin plastic leaded chip carrier (PL-CC-68).

Ordering Information

Type	Ordering code	Package	Function
SAB 82258A-R	Q67120-P250	C-CC-68	Advanced DMA controller, 8 MHz
SAB 82258A-1-R	Q67120-P249	C-CC-68	Advanced DMA controller, 10 MHz
SAB 82258A-A	Q67120-P248	C-PGA-68	Advanced DMA controller, 8 MHz
SAB 82258A-1-A	Q67120-P247	C-PGA-68	Advanced DMA controller, 10 MHz
SAB 82258A-N	Q67120-P246	PL-CC-68	Advanced DMA controller, 8 MHz
SAB 82258A-1-N	Q67120-P245	PL-CC-68	Advanced DMA controller, 10 MHz

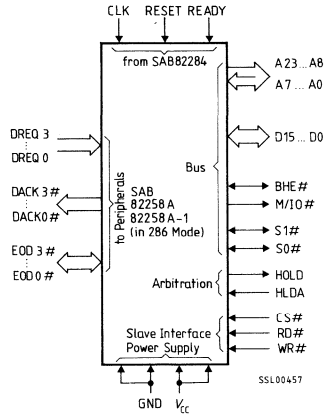
Logic Symbol



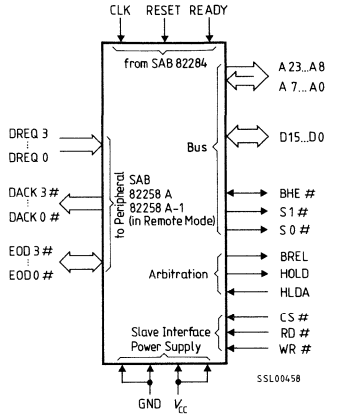
Modes of Operation, Adaptive Bus Interface

The SAB 82258A has been defined to work with all 16-bit processors linke SAB 80286, SAB 80186/188 and SAB 8086/88 without additional support and interface logic. Hence the local buses of the above processors are different in signals, functions and timings, the SAB 82258A has an adaptive bus interface to meet the different requirements of these local buses.

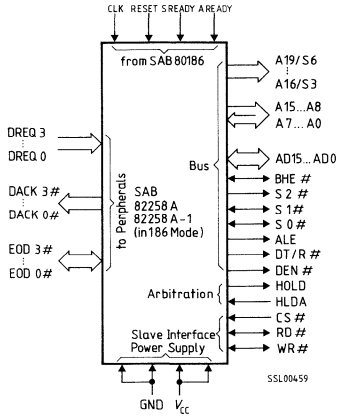
Logic Symbol in 286 Mode



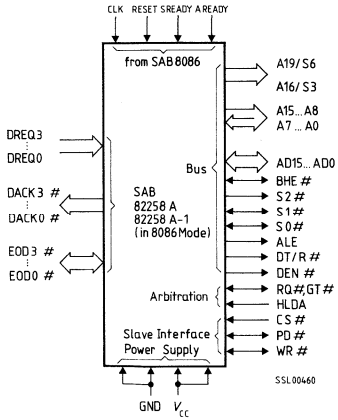
Logic Symbol in Remote Mode



Logic Symbol in 186 Mode



Logic Symbol in 8086 Mode

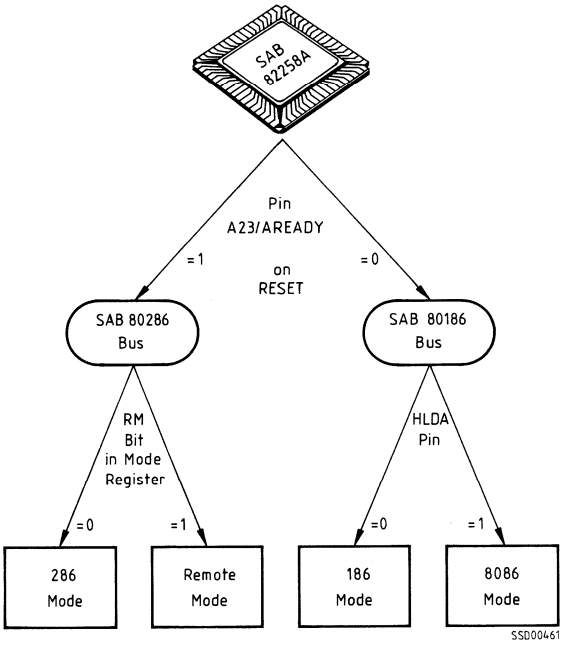


As a result of this, a bus compatibility with identical timing is attained with the processors SAB 80286, SAB 80186 and SAB 8086. A compatibility with the 8-bit bus versions of these processors, SAB 8088 and SAB 80188, is also guaranteed by defining the physical bus width of the SAB 82258A (per software) as 8 bits. The only difference in operation with SAB 8086 or SAB 80186 is that for SAB 8086 the HOLD pin functions as RQ#/GT# line (if HLDA is held high on reset).

The SAB 82258A can also be operated in remote or standalone mode, in which case it is not coupled directly to a processor. In remote mode, the SAB 82258A can be operated as sole bus master in a multimaster environment. The SAB 82258A is programmed to a specific mode of operation by applying defined logic levels to certain pins during reset and by setting the status of several control bits (see figure below).

Note: *Pin 57 (A21/DT/R# of the SAB 82258A) must be high during reset in order to enable proper operation. This is provided if pin A21 is connected to the SAB 80286's address bus. An internal pullup resistor supports applications where pin 57 is left open.*

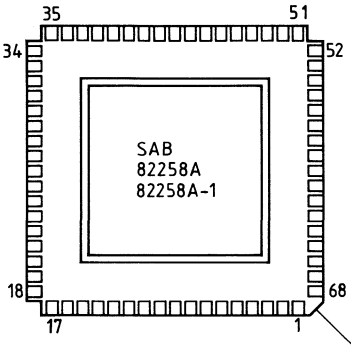
Mode Selection



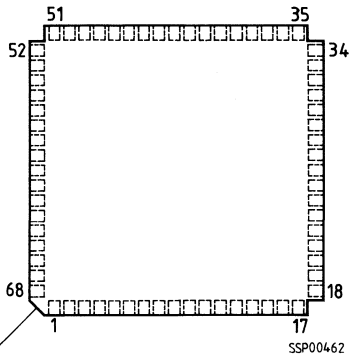
Pin 57 (A21 or DT/R#) must be high during Reset to enter the desired operating mode. An internal pullup pulls this pin high, if nothing is driving it.

Pin Configuration

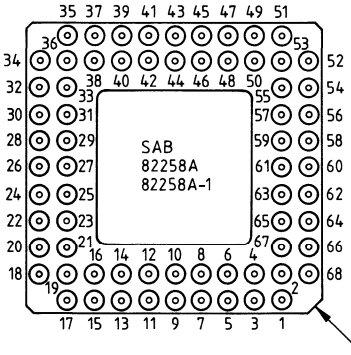
C-CC-68
Pad view



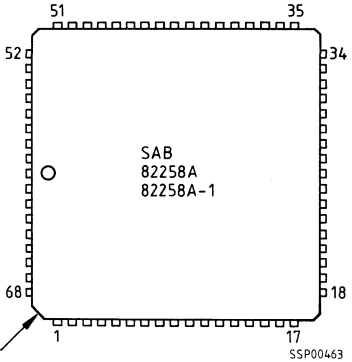
C-CC-68
PC board view



C-PGA-68
Bottom view



PL-CC-68
Top view



The PGA footprint is identical with the C-CC socket and PL-CC socket footprints (as viewed from component side of pc board).

Pin Definitions and Functions

Some pins of the SAB 82258A serve for different purposes according to the different modes of bus operation. The table below summarizes the pinouts of the SAB 82258A in the various modes. A detailed description of the general pin functions as well as the mode-specific pin functions is given in the following sections.

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
16	HOLD	O	HOLD	O	HOLD or RQ#/GT#	O (186) I/O (8086)
17	HLDA	I	HLDA	I	HLDA	I
1	BHE#	I/O	BHE#	I/O	BHE#	I/O
14	M/IO#	O	BREL	O	S2#	O
11	S1#	I/O	S1#	O	S1#	I/O
13	S0#	I/O	S0#	O	S0#	I/O
8	CS#	I	CS#	I	CS#	I
2	RD#	I	RD#	I	RD#	I/O
3	WR#	I	WR#	I	WR#	I/O
10	READY#	I	READY#	I	SREADY	I
59	A23	O	A23	O	AREADY	I
58	A22	O	A22	O	ALE	O
57	A21	O	A21	O	DT/R#	O
56	A20	O	A20	O	DEN#	O
55	A19	O	A19	O	A19/S6	O
54	A18	O	A18	O	A18/S5	O
53	A17	O	A17	O	A17/S4	O
52	A16	O	A16	O	A16/S3	O
51	A15	O	A15	O	A15	O
50	A14	O	A14	O	A14	O
49	A13	O	A13	O	A13	O
48	A12	O	A12	O	A12	O
47	A11	O	A11	O	A11	O
46	A10	O	A10	O	A10	O
45	A9	O	A9	O	A9	O
44	A8	O	A8	O	A8	O
42	A7	I/O	A7	I/O	A7	I/O
41	A6	I/O	A6	I/O	A6	I/O
40	A5	I/O	A5	I/O	A5	I/O

Pin Definitions and Functions (cont'd)

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
39	A4	I/O	A4	I/O	A4	I/O
38	A3	I/O	A3	I/O	A3	I/O
37	A2	I/O	A2	I/O	A2	I/O
36	A1	I/O	A1	I/O	A1	I/O
35	A0	I/O	A0	I/O	AO	I/O
18	D15	I/O	D15	I/O	AD15	I/O
20	D14	I/O	D14	I/O	AD14	I/O
22	D13	I/O	D13	I/O	AD13	I/O
24	D12	I/O	D12	I/O	AD12	I/O
27	D11	I/O	D11	I/O	AD11	I/O
29	D10	I/O	D10	I/O	AD10	I/O
31	D9	I/O	D9	I/O	AD9	I/O
33	D8	I/O	D8	I/O	AD8	I/O
19	D7	I/O	D7	I/O	AD7	I/O
21	D6	I/O	D6	I/O	AD6	I/O
23	D5	I/O	D5	I/O	AD5	I/O
25	D4	I/O	D4	I/O	AD4	I/O
28	D3	I/O	D3	I/O	AD3	I/O
30	D2	I/O	D2	I/O	AD2	I/O
32	D1	I/O	D1	I/O	AD1	I/O
34	D0	I/O	D0	I/O	AD0	I/O
7	DREQ0	I	DREQ0	I	DREQ0	I
6	DREQ1	I	DREQ1	I	DREQ1	I
5	DREQ2	I	DREQ2	I	DREQ2	I
4	DREQ3	I	DREQ3	I	DREQ3	I
61	DACK0#	O	DACK0#	O	DACK0#	O
62	DACK1#	O	DACK1#	O	DACK1#	O
63	DACK2#	O	DACK2#	O	DACK2#	O
64	DACK3#	O	DACK3#	O	DACK3#	O
65	EOD0#	I/O	EOD0#	I/O	EOD0#	I/O
66	EOD1#	I/O	EOD1#	I/O	EOD1#	I/O
67	EOD2#	I/O	EOD2#	I/O	EOD2#	I/O
68	EOD3#	I/O	EOD3#	I/O	EOD3#	I/O
15	RESET	I	RESET	I	RESET	I
12	CLK	I	CLK	I	CLK	I
9,43	GND	–	GND	–	GND	–
26,60	V_{CC}	–	V_{CC}	–	V_{CC}	–

Pin Definitions for All Operating Modes

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>BHE#</td><td>1</td><td>I/O</td><td>BUS HIGH ENABLE
This active low input indicates transfer of data on the upper byte of the data bus, D15 to D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use BHE# to condition chip select functions. BHE# floats to tristate off when the SAB 82258A does not own the bus.
BHE# and A0 encodings
<table>
<tr><th>BHE#</th><th>A0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer (D15-D8)</td></tr>
<tr><td>0</td><td>1</td><td>Byte transfer on upper half of data bus (D15-D8)</td></tr>
<tr><td>1</td><td>0</td><td>Byte transfer on lower half of data bus (D7-D0)</td></tr>
<tr><td>1</td><td>1</td><td>Odd-addressed byte on 8-bit bus (D7-D0)</td></tr>
</table></td></tr>
<tr><td>RD#</td><td>2</td><td>I</td><td>READ
This active low input in conjunction with chip select enables reading the SAB 82258A register which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82258A clock.</td></tr>
<tr><td>WR#</td><td>3</td><td>I</td><td>WRITE
This active low input in conjunction with chip select enables writing into the SAB 82258A registers which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82258A clock.</td></tr>
<tr><td>DREQ0-
DREQ3</td><td>4-7</td><td>I</td><td>DMA REQUEST (0 TO 3)
These active high inputs are used for synchronized DMA transfers. DREQ3 has the meaning of I/O request (IOREQ) if channel 3 is a multiplexer channel. These signals can be asynchronous to the SAB 82258A clock.</td></tr>
</table>

Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CS#	8	I	**CHIP SELECT** This active low input enables the access of a processor to SAB 82258A registers. This access is additionally controlled either by bus status signals or by the read or write command signals. Chip select can be asynchronous to the SAB 82258A clock.
CLK	12	I	**CLOCK** This input provides the fundamental timing. In 286 mode and remote mode it must be two times the system clock. It can be directly connected to the SAB 82284 CLK output. It is divided by two to generate the SAB 82258A internal clock. The on-chip divide-by-two circuitry can be synchronized to the external clock generator by a low-to-high transition on the RESET input, or by the first high-to-low transition on the status inputs S0# or S1# after reset. In 186/8086 mode no internal prescaling is done.
S0#, S1#	11, 13	I/O	**BUS STATUS LINES (0, 1)** These signals control the support circuits. The beginning of a bus cycle is indicated by S1# or S0# or both going active. The termination of a bus cycle is indicated by all status signals going inactive in 186 mode or bus ready signal (READY#) going active in 286 mode. The type of bus cycle is indicated by S0#, S1# and S2# (in 186 mode) or M/IO# (in 286 mode). S2# and M/IO# have the same meaning but in 186 mode the S2# signal can be active only when at least one of S1# or S0# is active, whereas in 286 mode the M/IO# signal is valid with the address on the address lines. The SAB 82258A can generate the following bus cycles by activating the status signals (and M/IO# in 286 mode):

Pin Definitions for All Operating Modes (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>S0#,S1#
(cont'd)</td><td>11, 13</td><td>I/O</td><td>
<table>
<tr><th>M/IO#
or S2#</th><th>S1#</th><th>S0#</th><th>Cycle Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Read I/O-vector
(for multiplexer channel)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from I/O space</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into I/O space</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle, does not occur
in 186 mode</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read from memory space</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write into memory space</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No bus cycle</td></tr>
</table>

When the SAB 82258A is not the master of the local bus the status signals are used as inputs for detection of synchronous accesses to the SAB 82258A. The following table shows the bus status and CS# signals and their interpretation by the SAB 82258.
<table>
<tr><th>CS#</th><th>S1#</th><th>S0#</th><th>Description</th></tr>
<tr><td>1</td><td>X</td><td>X</td><td>SAB 82258A is not
selected (no action)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No SAB 82258A
access (no action)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from an
SAB 82258A register</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into an
SAB 82258A register</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle[1)]</td></tr>
</table>
</td></tr>
</table>

[1)] SAB 82258A is selected but no synchronous access is activated. In this case the SAB 82258A monitors RD# and WR# signals for detection of an asynchronous access.

Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
RESET	15	I	**SYSTEM RESET** An activation of the reset signal forces the SAB 82258A to the initial state. The reset signal must be synchronous to CLK.
DACK0#-DACK3#	61-64	O	**DMA ACKNOWLEDGE (0 TO 3)** These active low inputs acknowledge the requests on the related DREQn signals. They are activated when the requested transfer(s) is (are) performed. If the channel 3 is a multiplexer channel the signal DACK3# has the meaning of I/O acknowledge (IOACK#).
EOD0#-EOD3#	65-68	I/O	**END OF DMA (0 TO 3)** These lines are implemented as open drain output drivers with a high impedance pullup resistor and thus can be used as bidirectional lines. As **outputs** the lines are activated for two system clock cycles at the end of the DMA transfer of the corresponding channel (if enabled) or they are activated under program control (EOD output or interrupt output). If the lines are held internally high but forced to low by external circuitry, they act as "End of DMA" **inputs.** The current transfer is aborted and the SAB 82258A continues with the next command. Additionally, a special function is possible with the EOD2# pin: this pin can also be used as common interrupt signal for all 4 channels. In this mode this line is not an open drain output but a pushpull output (output only). The other EOD# pins may be used as EOD# outputs/inputs as described above.
V_{CC}	26, 60		**POWER SUPPLY** (+ 5 V)
GND	9, 43		**GROUND** (0 V)

Pin Definitions for 286 Mode and Remote Mode

In 286 mode the SAB 82258A bus signals and bus timings are the same as for the SAB 80286 processor. Additional features of the SAB 82258A require a slight change in pin definitions. The processor can access internal registers of the SAB 82258A. Therefore the bus signals must support these accesses. This means that some of the bus control signals must be bidirectional and some additional bus control signals are necessary. All additional pins and their functions are listed below.

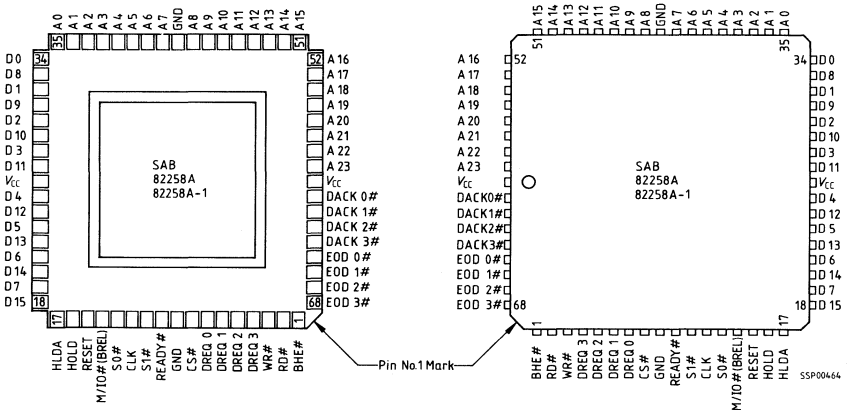
In **remote mode** most of the bus signals are the same as in 286 mode. Pin 14 (M/IO#) serves as BREL output. The HOLD/HLDA arbitration in remote mode is used only for system bus accesses, the resident bus is accessed directly.

The CS# input additionally requests access to the local bus of the SAB 82258A. These accesses are enabled through the BREL output after the SAB 82258A has released the bus.

Pin Configuration in 286 Mode and Remote Mode

Component Pad View – As viewed from underside of component when mounted on the board (Example: C-CC-68)

PC Board View – As viewed from the component side of the pc board (Example:PL-CC-68)



Pin Definitions for 286 Mode and Remote Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
READY#	10	I	**BUS READY** This active low input terminates a bus cycle. Bus cycles are extended without limit until terminated by READY# low. READY# is a synchronous input requiring setup and hold times relative to the system clock to be met for correct operation.
M/IO#	14 (286 mode)	O	**Memory / I/O SELECT** In 286 mode, pin 14 is used to distinguish between memory and I/O space addresses.
BREL	14 (remote mode)	O	**BUS RELEASE** In remote mode pin 14 is used to indicate when the SAB 82258A has released the control of the local bus.
HOLD	16	O	**BUS HOLD REQUEST** This active high output indicates a request for control of the local bus (286 mode) or the system bus (remote mode). When the SAB 82258A relinquishes the bus it drops the HOLD output. HOLD is connected to the bus arbiter in remote mode.
HLDA	17	I	**BUS HOLD ACKNOWLEDGE** This active high input indicates that the SAB 82258A can acquire the control of the bus. When it goes low SAB 82258A must relinquish the bus at the end of its current cycle. HLDA can be asynchronous to the SAB 82258A clock. HLDA is connected to the bus arbiter in remote mode.
D0-D15	18-25, 27-34	I/O	**DATA BUS (0 TO 15)** This is the bidirectional 16-bit data bus. For use with an 8-bit bus, only the lower 8 data lines D7-D0 are relevant.
A0-A7	35-42	I/O	**ADDRESS BUS (0 TO 7)** The lower 8 address lines for DMA transfers. They are also used to input the register address when the processor accesses an SAB 82258A register.
A8-A23	44-59	O	**ADDRESS BUS (8 TO 23)** Higher address outputs.

Pin Definitions for 186 Mode and 8086 Mode

In 186 mode and 8086 mode the SAB 82258A multiplexes the address with data and additional status lines.

Pins A0 to A15 retain their original function while pins A20 to A23 serve for different purposes (not used for address in 186 8086 mode).

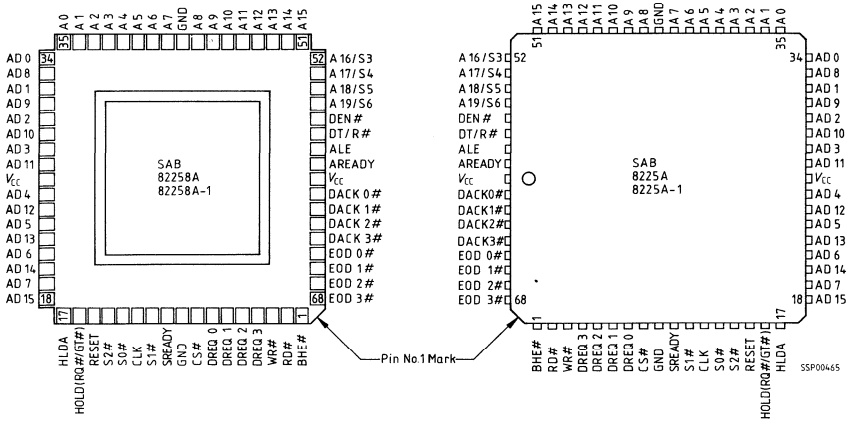
The RD# and WR# lines are additionally used as outputs in 186 8086 mode to support minimum mode systems.

Note that the HLDA input can be used to force the SAB 82258A off the bus in 8086 mode, even though the arbitration is done via the RQ# GT# line!

Pin Configuration in 186 Mode and 8086 Mode

Component Pad View – As viewed from underside of component when mounted on the board (Example: C-CC-68)

PC Board View – As viewed from the component side of the pc board (Example: PL-CC-68)



Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ALE	58	O	**ADDRESS LATCH ENABLE** This active high output provides a strobe signal to separate the address information on the multiplexed AD lines.
DEN#	56	O	**DATA ENABLE** This active low output enables the data transceivers.
DT/R#	57	O	**DATA TRANSMIT/RECEIVE** This signal controls the direction of the data transceivers. When low, data is transferred to the SAB 82258A, when high, the ADMA places data onto the data bus.
S2#	14	O	**STATUS LINE 2** Signal as for SAB 186/8086/88 processors (see also S1#, S0# description in 286 mode).
AREADY	59	I	**ASYNCHRONOUS READY** The rising edge of this signal is internally synchronized, the falling edge must be synchronous to CLK. During reset this signal must be low to enter 186 mode.
SREADY	10	I	**SYNCHRONOUS READY** This signal must be synchronized externally. The use of this pin permits a relaxed system-timing specification by eliminating the clock phase which is required for resolving the signal level when using the AREADY input.
AD0-AD15	18-25 27-34	I/O	**ADDRESS/DATA BUS (0 to 15)** Lower address and data information is multiplexed on pin AD0 to AD15.
A0-A7 A8-A15	35-42 44-51	I/O O	**ADDRESS BUS (0 to 15)** Additionally the demultiplexed address information is available on address pin A0 to A15.

Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A16/S3-A19/S6	52–55	O	**ADDRESS BUS (16 TO 19)/ STATUS LINES (3 TO 6)** The higher address bits are multiplexed with additional status information.
HLDA	17	I	**BUS HOLD ACKNOWLEDGE** This active high input indicates that the SAB 82258A can acquire the control of the bus. When it goes low the SAB 82258A must relinquish the bus at the end of its current bus cycle. HLDA can be asynchronous to the SAB 82258A clock. In 8086 mode, HLDA can be used to force the SAB 82258A off the bus.
HOLD	16 (186 mode)	O	**BUS HOLD REQUEST** This active high output indicates a request for control of the bus. When the SAB 82258A relinquishes the bus, it drops the HOLD output.
RQ#/GT#	16 (8086 mode)	I/O	**REQUEST/GRANT** In 8086 mode the HOLD output acts as RQ#/GT# line. The RQ#/GT# protocol implements a one-line communication dialog required to arbitrate the use of the system bus normally done via HOLD/HLDA. The RQ#/GT# signal is active low and has an internal pullup resistor.

Functional Description

General

The SAB 82258A is an advanced general-purpose DMA controller especially designed for efficient highspeed data transfers on an SAB 80286 bus as well as on an SAB 80186/188 or SAB 8086/88 bus.

It supports two basic operating modes:

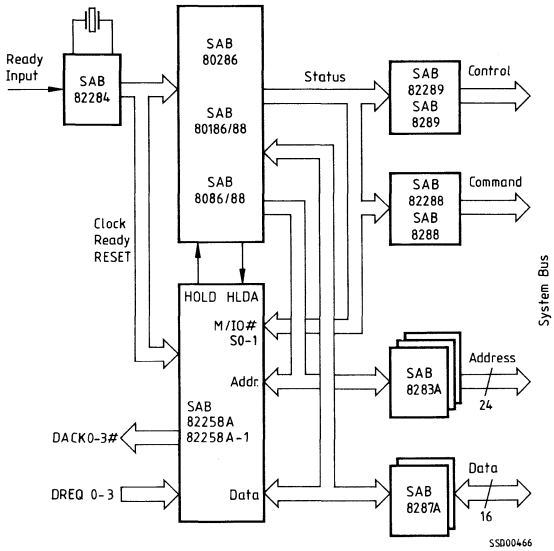
- local mode (tightly coupled to a processor) and
- remote mode (loosely coupled to a processor).

In the first case the SAB 82258A is directly coupled to the CPU and uses the same system support/control devices as the CPU (see figure below). This mode is possible with the above-mentioned processors.

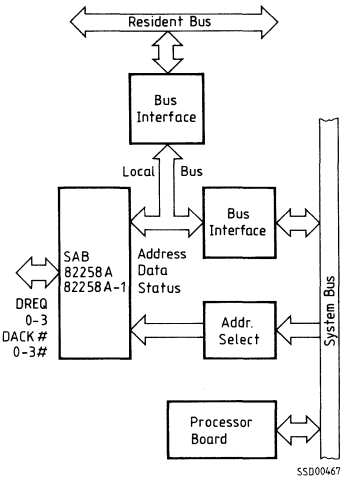
As a second basic operating mode remote (standalone) mode is supported (see figure below). Here the SAB 82258A has its own sets of bus interface circuits and thus can utilize its own local bus. This allows the DMA controller to work in parallel with the main CPU and therefore overall system performance can be increased. Besides, this mode is very useful for the design of modular systems and allows connecting the SAB 82258A to any other processor via the system bus independent of the processor's local bus.

Basic ADMA Operating Modes

a) Local Mode



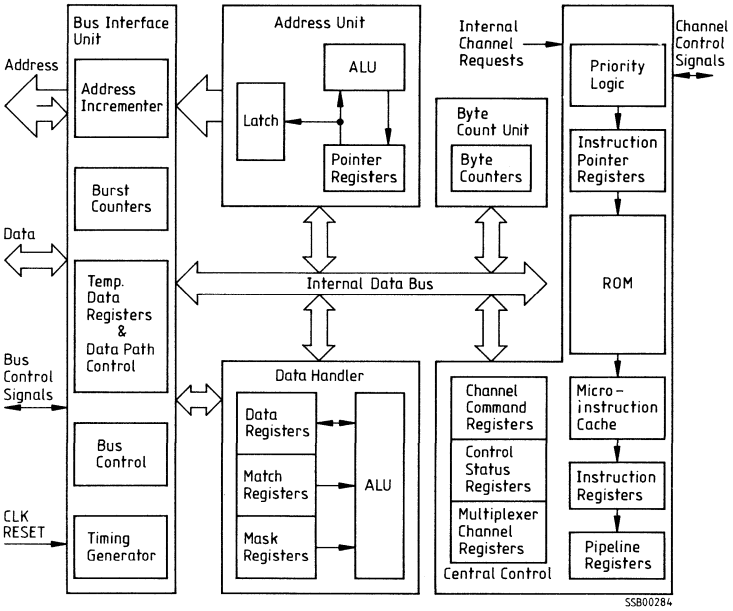
b) Remote Mode



The SAB 82258A has four independent DMA channels that can transfer up to 10 Mbytes/s in single cycle mode (2 clocks/transfer). In 2-cycle transfer mode the maximum rate is 5 Mbytes/s. Switching between channels induces no time penalty. Thus the overall maximum transfer rate of 10 Mbytes s is also valid for multiple channel operation.

This fast operation is possible because of the pipelined architecture of the SAB 82258A which allows the different functional units to work in parallel. The maximum transfer rate can be doubled to 20 Mbytes s (in a 10 MHz system), if the ADMA executes 32-bit fly-by transfers.

Block Diagram of the SAB 82258A



The ADMA supports two address spaces, memory space and I O space, each with a maximum address range of 16 Mbytes. In addition, the maximum block length (byte count) is also 16 Mbytes to support applications where large blocks of data have to be transferred (e.g. graphics).

As source or as destination, four parameters can be selected independently:

- address space (memory or I/O)
- logical bus width (same as physical bus width or 8 bits on a 16-bit physical bus) and
- transfer direction (increasing, decreasing, fixed pointer or constant value).

If the physical bus width of source or destination differs from the logical bus width, an automatic byte/word assembly (word/byte disassembly) takes place. The same is true, if the logical bus widths of source and destination are not identical.

Transfers between different address spaces can be performed within one or two cycles, transfers within one address space can be performed only in two cycles.

The transfers can be executed free running or externally synchronized via DREQ where source or destination synchronization is possible.

In summary, this very symmetrical operation of the SAB 82258A gives the user a great amount of design flexibility.

Adaptive Bus Interface

As shown in the figure on page 4, the SAB 82258A bus interface has two basic timing modes: the 286 mode and the 186 mode. In 286 mode the SAB 82258A is directly coupled to an SAB 80286, in 186 mode to an SAB 80186 or SAB 80188. For each of these two modes a slightly different variation exists:

- For the 286 mode the variation is the remote mode, where the ADMA operates as a bus master on the system bus without being directly coupled to a processor. In this mode the SAB 82258A can utilize its own local bus and the communication with the main processor is done via the system bus. To enable access to ADMA registers by the main processor, the SAB 82258A must release its local bus. This "local bus arbitration" in remote mode is done via the CS# and BREL lines.
- For the 186 mode the variation is the 8086 mode, where the SAB 82258A supports the RQ#/GT# protocol and thus can be directly coupled to an SAB 8086 or SAB 8088.

Memory-Based Communication

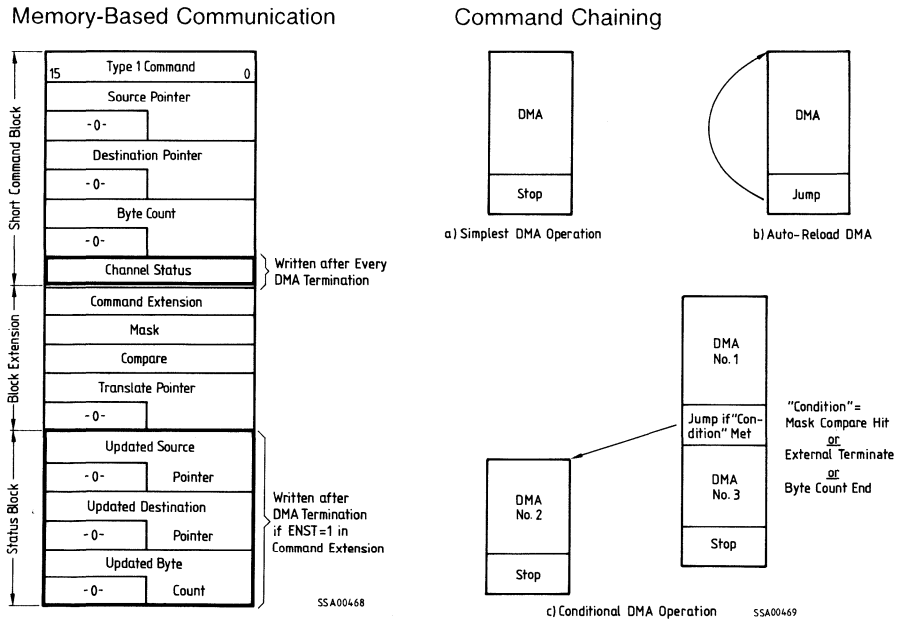
The normal communication between the ADMA and the processor is memory-based. This means that all necessary data for a transfer is contained in a command block in memory accessible for CPU and SAB 82258A (see figure below). To start the transfer the CPU loads one of the command pointer registers of the SAB 82258A with the address of the command block and then issues a "start channel command". Getting the command the SAB 82258A loads the entire command block from memory into its on-chip channel registers and executes it. On completing the operation, channel status information is written back by the SAB 82258A into the channel status word contained in the command block in memory.

If desired, the actual contents of the channel registers, i.e. source pointer, destination pointer and byte count it transferred to the channel status block. The channel status block immediately follows the command block in memory (see figure below).

Command Chaining

Command blocks for any channel can be chained for sequential execution (see figure). When the SAB 82258A has completed the execution of a command, it automatically increments the command pointer and starts to fetch and execute the next command block until a stop command is found. As a result a chain of command blocks can be executed by the ADMA without any CPU intervention. Due to conditional and unconditional STOP and JUMP commands, quite complex sequences of DMA can be executed by the SAB 82258A.

Memory-Based Communication and Command Chaining



Data Chaining

Data chaining allows an automatic, dynamic linking of data blocks scattered in memory. There are two types: list and linked-list data chaining.

If for a DMA the source blocks are to be dynamically linked during DMA, it is called source chaining and the effect is that of gathering data blocks and sending them out effectively as one block.

If one source block is dynamically broken up into multiple destination blocks, it is called destination chaining. This results in scattering of a block.

This dynamic linking and unlinking of data blocks makes the logical sequencing of data independent of its physical sequencing in memory.
In the case of linked list chaining (see figure a) each data block has a descriptor containing information on position of the data block in memory, length of the data block and a pointer to the next descriptor.

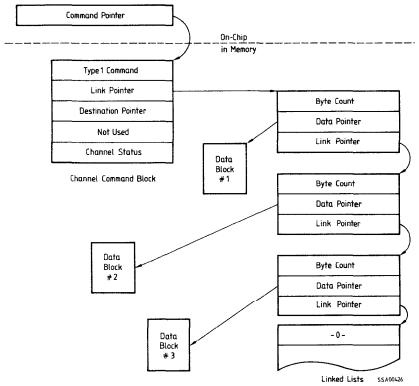
During data transfer the data block 1 is sent out first, then 2 and so on till a "0" is encountered in the byte count field.

The second type of data chaining is list chaining (see figure b).

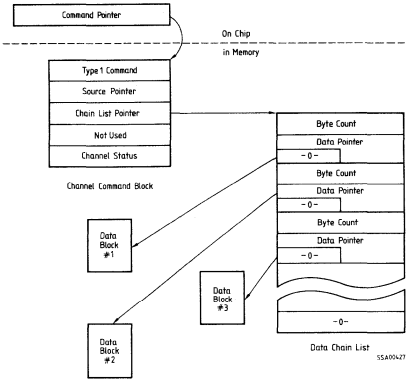
Unlike linked list chaining, here the data block descriptors are continuous in a block and thus determine the sequence of data blocks. The flexibility lost in terms of predefined sequence is gained in terms of linking time.

Data Chaining

a) Linked List Chaining



b) List Chaining



"On-The-Fly" Operations

A normal DMA controller blindly transfers data from source to destination without looking at the data. In case of the ADMA on-the-fly operations are executed during the DMA transfer and allow inspection and/or operation on the transferred data. There are three possible on-the-fly operations:

- mask compare
- translate and
- verify

During a mask compare operation each byte/word transferred is compared to a given pattern. One or more bits can be masked and thus do not contribute to the result of the compare operation. The result can be used by subsequent conditional stop or jump operations.

For translate operation the byte (no word possible) that is fetched from source is added to a translate pointer to build the effective source pointer. The byte pointed to by this pointer is then fetched and sent out to the destination. Of course, a mask compare operation is possible on the byte sent out.

The verify operation is a type of block compare operation to compare each byte/word of data read from a peripheral with the one in a data block in the memory. There are three options:

1. Verify with no termination on mismatch
   (2-cycle transfer only)
2. Verify with termination on mismatch
   (2-cycle transfer only)
3. Verify and save (single cycle transfer only).
   Here an actual transfer with compare takes place.
   The transfer is not stopped on mismatch.

Note: *Verify and save operation and mask compare operation can be used during 32-bit fly-by transfer, but can check a maximum of 16 bits, not a complete double word.*

Multiplexer Channel

When programmed to multiplexer mode, channel 3 (supported by a multiplexer logic) can be used to service up to 32 subchannel request lines (see figures below).Thus it is ideally suited to service a large number of comparatively slow equipment like CRT terminals, line printers, serial links, etc. Since multiple subchannels are processed with the resource of one DMA channel, the overhead of subchannel switching, of course, decreases the total effective throughput on the multiplexer channel.

To allow efficient control even of the subchannels, a separate command pointer for each subchannel is provided within the multiplexer table. Thus an individual subchannel program (command chain) can be used for each subchannel.

Different transfer modes are provided for subchannels:

Byte/word multiplex:

One byte or word is transferred per request. Updating the pointers is done within the actual command block.

Single transfer:

Similar to byte/word multiplex, but with execution of command chaining after each transfer.

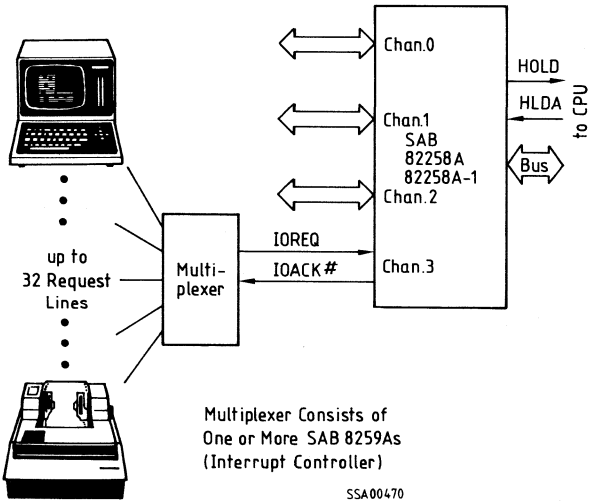
Block multiplex:

I/O request initiates execution of a complete command block, i.e. the complete data block specified is transferred. This allows maximum transfer rates (2-cycle transfers) also for subchannels.

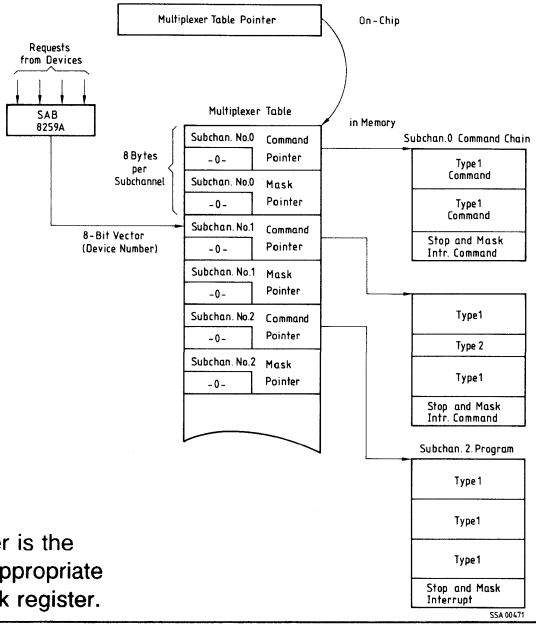
A type 2 command in a subchannel program can issue an interrupt, whereby the multiplexer channel interrupt vector register (MIVR) provides the corresponding subchannel number for the CPU.

A subchannel program is terminated by a stop and mask command which automatically masks the corresponding request line within the SAB 8259A thus blocking this subchannel until it is enabled again by the CPU.

Multiplexer Channel



Structure of the Multiplexer Table



The mask pointer is the address of the appropriate SAB 8259A mask register.

32-Bit Fly-by Transfers

The 32-bit transfer enable bit TR32 (bit 6 of the channel command register extension CCRX) allows the address pointers and byte counters to be modified not only by 1 or 2, but also by 4 in order to count 32-bit double words. Therefore, the SAB 82258A can control 32-bit transfers in single cycle mode. In this mode, data flows past the DMA controller rather than through it. All features that use the data assembly registers (two-cycle mode, compare, verify, etc.), should be avoided, because the 16-bit data port can access only one half of a 32-bit data bus.
Addresses and byte counts must be aligned to double-word boundaries (i.e. multiples of 4) in order to ensure proper operation. Also the effective transfer width (logical and physical bus width) must be programmed to 16 bits. As the external control signals do not allow to distinguish 32-bit fly-by transfers from 16-bit transfers, the transfer mode of a channel must be predefined.

Note: *If the SAB 82258A is to operate in a system with a true 32-bit address bus, the upper address byte (A31 to A24) must be provided by an external page register, as the ADMA's address bus is still 24 bits wide.*

Operating the SAB 82258A

Reset

When activating the reset input, the SAB 82258A is forced into its initial state. All channels and bus activities are stopped, tristate lines are tristated and the others enter the inactive state. While the reset input is active, pin 57 must be held high and lines A23 AREADY and HLDA must be forced to the appropriate levels to select the desired bus interface mode (see figures on page 4, 49 and 62).
After deactivating reset the inactive state is maintained, in addition the state of the SAB 82258A registers is as follows:

- general mode register, general burst register, general delay register, general status register and the four channel status registers are set to zero,
- the vector-not-valid bit of the multiplexer interrupt vector register is set to 1,
- all other registers and bits are undefined.

Note: The general mode register (GMR) should be loaded first to select the mode of operation before any other activity is started on the ADMA.

DMA Interface

The DMA interface consists of three lines:

- DREQ – DMA request
- DACK# – DMA acknowledge and
- EOD# – End of DMA

The first two lines work as request and acknowledge lines to control synchronized DMA transfers as known from conventional DMA controllers.

A special feature of the SAB 82258A are the bidirectional EOD# lines . Firstly they can be used as inputs to receive an asynchronous external terminate signal to terminate a running DMA.
Secondly, as an output, they can be used to send out a pulse which interrupts the CPU and/or signals to the peripheral a specific status (e.g. transfer aborted, or end of a block, or send/receive next block ...).

The EOD# output signal can be generated synchronously to a transfer (during the last transfer) or asynchronously to the transfers by a specific command.

In addition the EOD# output of channel 2 can be used as a collective interrupt output for all DMA channels while the other three retain their normal function.

Slave Interface

The slave interface is used to access the SAB 82258A internal registers. Although nearly all of the communication between CPU and ADMA is done via memory-based data blocks, some direct accesses to ADMA registers are necessary.

For example during the initialization phase the general mode register must be written, or to start a channel the command pointer register and the general command register must be loaded. Also during the debugging phase it is of great benefit to have access to all of the SAB 82258A internal registers.

The slave interface is enabled by the CS# input and consists of the following lines:

- S0#, S1# – status lines (inputs)
- RD#, WR# – control lines (inputs)
- A0-A7 – register address (inputs)
- D0-D15 – data lines (inputs outputs) or
- AD0-AD15 – data lines (inputs/outputs) for synchronous access in 186 mode

Note that all of these lines are outputs, if the SAB 82258A is an active bus master.

In 186 mode and 286 mode two types of accesses are possible:

- Synchronous access by means of the status lines. Processor and SAB 82258A are directly coupled and must use the same clock.
- Asynchronous access by using the control lines RD# and WR# (processor and ADMA may have different clocks).

In all modes except the synchronous access in 186 mode the register address must be supplied on address pins A0 to A7. Using synchronous access in 186 mode the address information is expected at address/data lines AD0 to AD7.
In remote mode only the asynchronous access is possible because the SAB 82258A first has to release its local bus to enable the register access. On receiving an access request (activation of CS# input) the SAB 82258A releases its local bus as soon as possible and signals this by activating the BREL line. Now the CPU can accomplish its access.

Bus Arbitration

To arbitrate access to the bus between the ADMA and the processor, the signals HOLD and HLDA serve for communication. Normally the ADMA competes for the bus via HOLD, the processor grants access to the bus via HLDA. The HLDA signal can also be deactivated in order to force the ADMA off the bus for a certain reason (kick off). After reactivation of HLDA, the ADMA will again get control of the bus.
In 8086 mode this communication is done by pulses via a single RQ# GT# line which uses the HOLD pin. In this case normally the HLDA input has no function. Nevertheless, even in 8086 mode the HLDA input can be used for kick-off. This provides some kind of additional bus arbitration.

Register Set

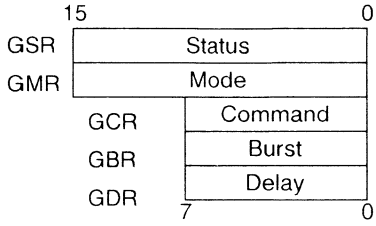
The following figure shows the user visible registers of the SAB 82258A. A set of 5 registers, called the general registers, is used for all of the 4 channels. The mode register is being written to first after reset and it describes the SAB 82258A environment – bus widths, priorities, etc.

The general command register (GCR) is used to start and stop the DMA transfer on different channels. The general status register (GSR) shows the status of all of the 4 channels; if the channel is running, if interrupt is pending, etc. General burst register (GBR) and general delay register (GDR) are used to specify the bus load which is permissible for the SAB 82258A.

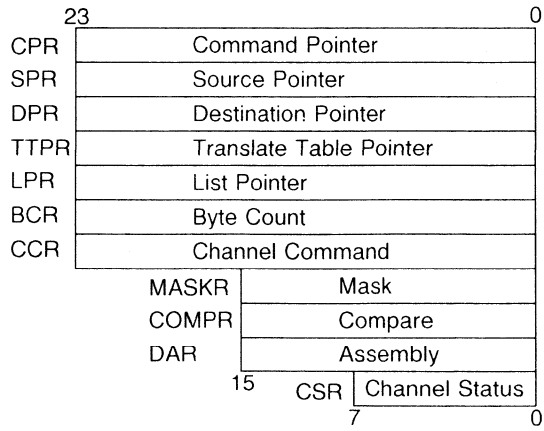
There is a set of channel registers for each of the 4 channels. Most channel registers serve as cache registers and need to be accessed only for debugging. During normal operation they are loaded automatically by the SAB 82258A (see next paragraph). The layout of register addresses shown in the figure on the next page. All register addresses are even. Locations not designated in that figure are reserved and should not be used.

SAB 82258A Register Set

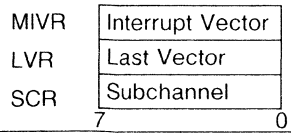
General Register



Channel Register (4 sets; 1 per channel)



Multiplexer Channel Register



Register Address Arrangement

Address Bits 0-5	Address Bits 7, 6: 00	01	10	11
0	GCR			
2	SCR			
4	GSR			
6				
8	GMR			
A	GBR			
C	GDR			
E				
10	CSR 0	CSR 1	CSR 2	CSR 3
12	DAR 0	DAR 1	DAR 2	DAR 3
14	MASKR 0	MASKR 1	MASKR 2	MASKR 3
16	COMPR 0	COMPR 1	COMPR 2	COMPR 3
18				MIVR
1A				LVR
1C				
1E				
20	CPR L0	CPR L1	CPR L2	CPR L3
22	CPR H0	CPR H1	CPR H2	CPR H3
24	SPR L0	SPR L1	SPR L2	SPR L3
26	SPR H0	SPR H1	SPR H2	SPR H3
28	DPR L0	DPR L1	DPR L2	DPR L3
2A	DPR H0	DPR H1	DPR H2	DPR H3
2C	TTPR L0	TTPR L1	TTPR L2	TTPR L3
2E	TTPR H0	TTPR H1	TTPR H2	TTPR H3
30	LPR L0	LPR L1	LPR L2	LPR L3/MTPR L
32	LPR H0	LPR H1	LPR H2	LPR H3/MTPR H
34				
36				
38	BCR L0	BCR L1	BCR L2	BCR L3
3A	BCR H0	BCR H1	BCR H2	BCR H3
3C	CCR L0	CCR L1	CCR L2	CCR L3
3E	CCR H0	CCR H1	CCR H2	CCR H3

Register Address Arrangement (cont'd)

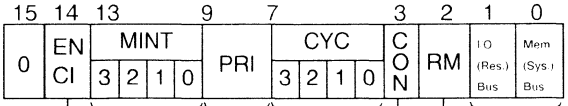
GCR	= General Command Register	MIVR	= Multiplexer Interrupt Vector Register
SCR	= Subchannel Register	LVR	= Last Vector Register
GSR	= General Status Register	CPR	= Command Pointer Register
GMR	= General Mode Register	SPR	= Source Pointer Register
GBR	= General Burst Register	DPR	= Destination Pointer Register
GDR	= General Delay Register	TTPR	= Translate Table Pointer Register
CSR	= Channel Status Register	LPR	= List Pointer Register
DAR	= Data Assembly Register	MTPR	= Multiplexer Table Pointer Register
MASKR	= Mask Register	BCR	= Byte Count Register
COMPR	= Compare Register	CCR	= Channel Command Register

Register Description

General Mode Register

In the general mode register GMR (figure below) the system wide parameters are specified. This register should be programmed first after reset, with an 8-bit bus program low byte first.

General Mode Register (GMR)



Physical Bus Width
0 8-bit
1 16-bit

Remote Mode Enable
0 Local mode
1 Remote mode

Mode of Channel 3
0 Normal channel
1 Multiplexer channel

Transfer Type *)
0 Two-cycle
1 Single-cycle

Channel Priority
00 all fixed, chan. 0 highest
01 Chan. 0,1,2 rotating
Chan. 3 fixed (lowest)
10 Chan. 0,1 rotating
(higher group)
Chan. 2, 3 rotating
(lower group)
11 all rotating

Interrupt Mask for Type 2 Channel Command
0 Interrupt enabled
1 Interrupt disabled

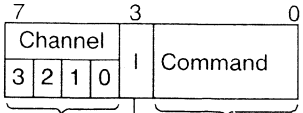
Common Interrupt Enable
0 EOD2 pin = EOD2
1 EOD2 pin = Common Interrupt

*) On multiplexer channel CYC3 identifies the associated control space for the multiplexer matrix(CYC3 = 0/1:SAB 8259A in I/O/memory space).

General Command Register

Individual channels are started and stopped by a command written to the general command register GCR (figure below). The GCR is directly loaded by the CPU.

General Command Register (GCR)



Channel Command

000	NOP	
001	CONTINUE	Channel(s) after it has been stopped by the STOP command
010	START	Channel(s) = Command block at system memory space
011	START	Channel(s) = Command block at resident I/O space
100	STOP	Channel(s)
101	START	Subchannel (number in SCR)
110	STOP	Subchannel (number in SCR)
111	HALT	Single-step channel(s): Start execution and stop before next command block will be loaded

Interrupt Command

0	NOP
1	Clear interrupt(s) of channel(s)

Channel Select

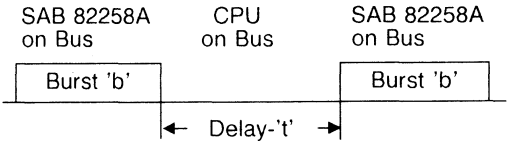
0	Channel not effected
1	Command refers to this channel

General Burst and Delay Register

It is possible to restrict the bus load generated by the SAB 82258A on the CPU bus by programming the burst and the delay register. The bus load is defined by the formula given in figure a) below. The factor b (burst) is programmed in the general burst register GBR, t (delay time) in the general delay register GDR (see figures b and c). Since the SAB 82258A can also execute locked bus cycles. the maximum burst length consists of b + 3 (8-bit bus) or b + 2 (16-bit bus) bus cycles. GBR and GDR must be directly loaded by the CPU. Loading GBR with 0 leads to no bus load limitations for the SAB 82258A (default after reset).

General Burst and Delay Register

a) Bus Loading

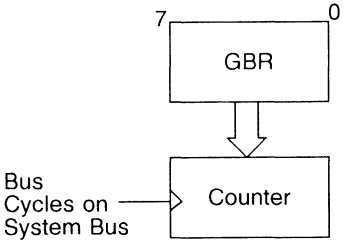


Bus Load due to the SAB 82258A $= \frac{b}{b+t}$

b) General Burst Register (GBR) – to Program 'b'

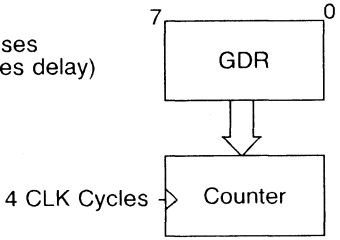
Determines max. number of contiguous bus cycles from the SAB 82258A

If GBR = 0, No Limit



c) General Delay Register (GDR) – to Program 't'

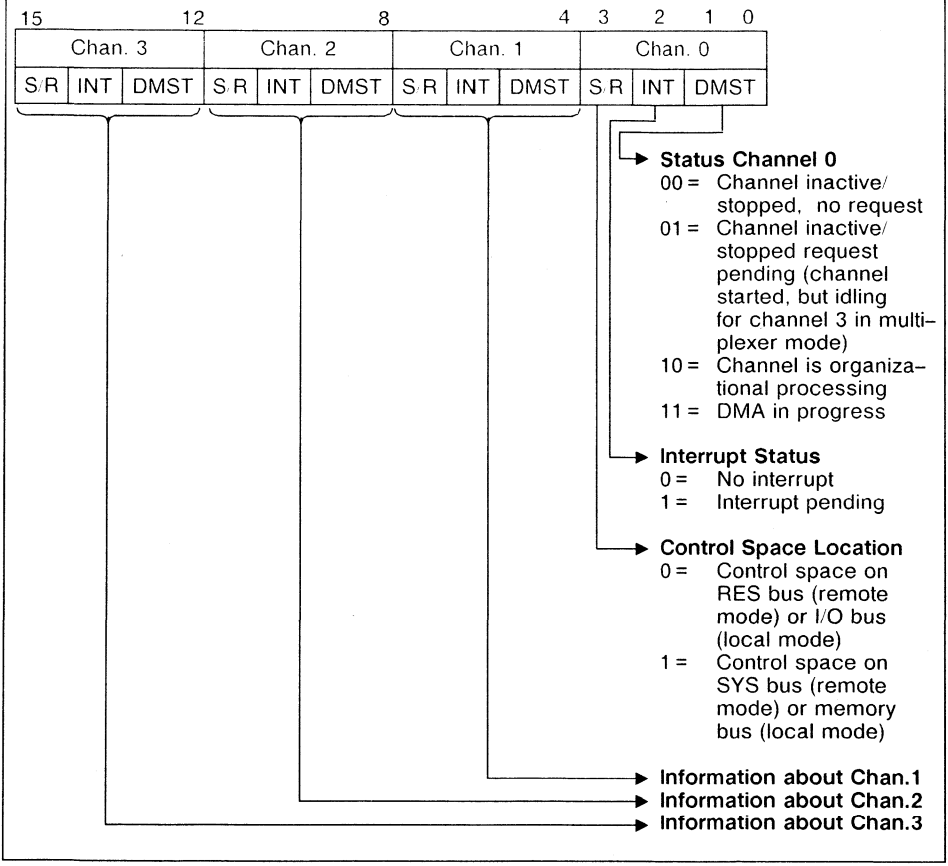
Determines min. number of clock cycles between burst accesses (default after reset = 0,i.e. 4 T-states delay)



General Status Register

The general status register GSR (figure below) shows the current status of all the channels.

General Status Register (GSR)



Channel Commands

The channel commands are contained in the channel command block. Up to 22 bits are used to specify the command. There are two types of channel commands:

- Type 1: for data movement
- Type 2: for command chaining control

The command block for a type 1 command is in general 26 bytes long (see figure „Memory based Communication").

For certain type 1 transfers which, for example, do not use on-the-fly match, translate or verify feature, the command is only 16 bits long and only a short command block is necessary (see figure „Memory based Communication").

The type 1 command fields (see figures below) contain information on:

a. Bus width of source and destination
b. If source and/or destination address should be incremented or decremented or kept constant during the transfer
c. If source/destination is in memory or I/O space (local mode) or in system or resident space (remote mode)
d. If data chaining (list or linked-list) is to be performed
e. If the data transfer is synchronized (source or destination)
f. If an on-the-fly match operation and/or translate operation has to be performed
g. If a verify operation has to be performed
h. If 32-bit fly-by transfers are to be executed.

Type 2 command blocks are 6 bytes long (see figure „Type 2 Command Block") of which the first 2 bytes form the command and the rest is either a relative displacement or an absolute address for the JUMP operation. There are two basic type 2 commands (see figure „Type 2 Command Block"):

a. JUMP – conditional and non-conditional
b. STOP – conditional and non-conditional

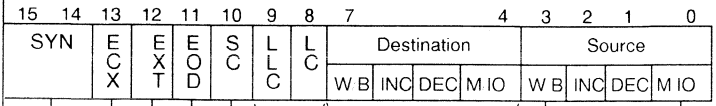
The conditional case tests for either of the 4 condition bits which are altered at the termination of any DMA operation:

- Termination due to byte count end
- Termination due to mask-compare
- Termination due to external terminate
- Verify operation resulting in mismatch.

It is thus possible to JUMP or STOP further execution of commands based on any of these conditions and optionally generate an EOD# or interrupt signal.

The combination of type 1 and 2 commands gives the SAB 82258A a high degree of "programmability". It can thus execute quite complex algorithms with a fairly low demand for CPU service.

Type 1 (DMA) Channel Command



Source Description Associated Space
0 I O or resident
1 Memory or system

Source Pointer
00 Printer not modified
01 Decrement pointer
10 Increment pointer
11 No pointer (constant value)

Logical Bus Width
0 8-bit
1 16-bit

Destination Description
Same as source description

Data Chaining
LLC LC
0 0 No chaining
0 1 List chaining
1 0 Link list chaining
1 1 Not allowed

Select Chaining
0 Destination data chaining
1 Source data chaining

For MUX Channel:
Transfer Chaining
0 Transfer is synchronized
1 Transfer not synchronized

Enable EOD# Output

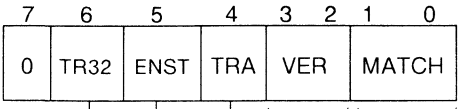
Enable External Terminate Input

Channel Command Block Length
0 Short
1 Long(with command extension)

Synchronization
00 Not valid(type 2 command)
01 Source synchronization
10 Destination synchronization
11 No synchronization (free running)

For Multiplexer Channel
00 Not valid(type 2 command)
01 Byte word multiplex operation
10 Single transfer operation
11 Block multiplex operation

Type 1 Channel Command Extension



Match-Compare
00 Disabled
01 Enable mismatch (byte/word)
10 Enable byte match
11 Enable word match

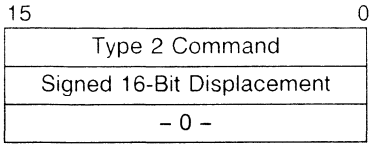
Verify
00 Verify disabled
01 Verify
10 Verify and halt (on mismatch)
11 Verify and save

Translate Enable
0 Translate disabled
1 Translate enabled

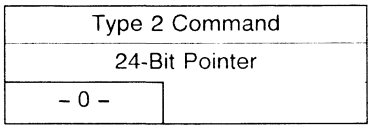
Enable Status Block
0 Update in channel command block disabled
1 Update enabled

32-Bit Transfer Enable
0 Byte/word transfers only
1 32-bit fly-by transfer enabled

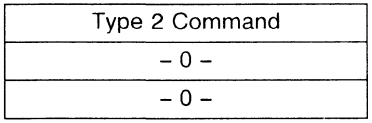
Type 2 Command Blocks (for command chaining control)



– Relative JUMP



– Absolute JUMP

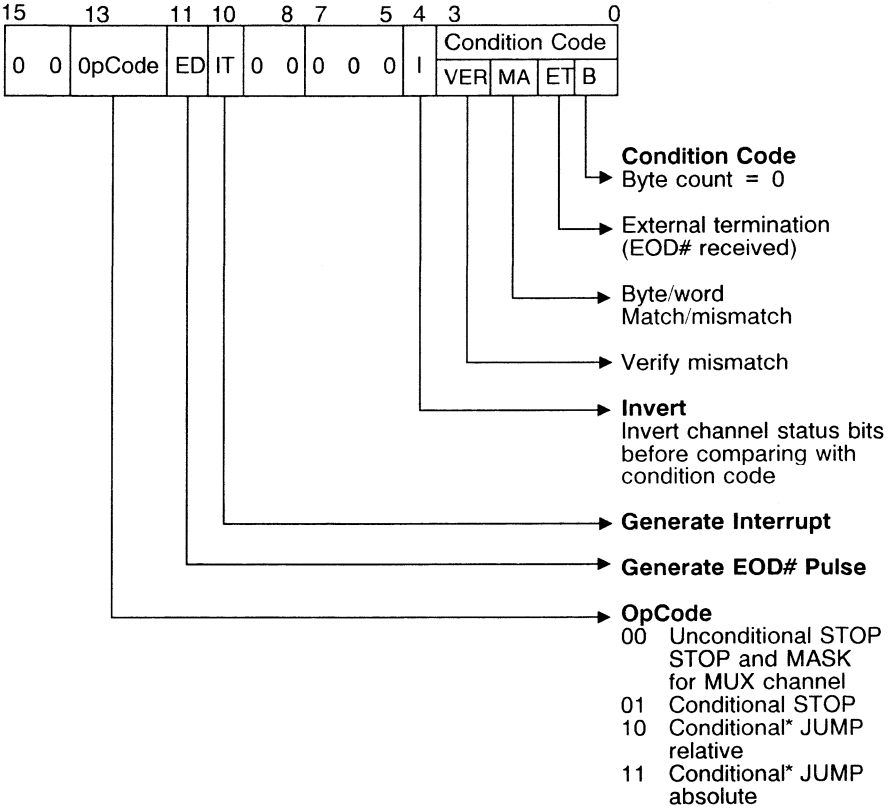


– Conditional STOP

– Unconditional STOP

– STOP and MASK for MUX Channel

Type 2 Command Format

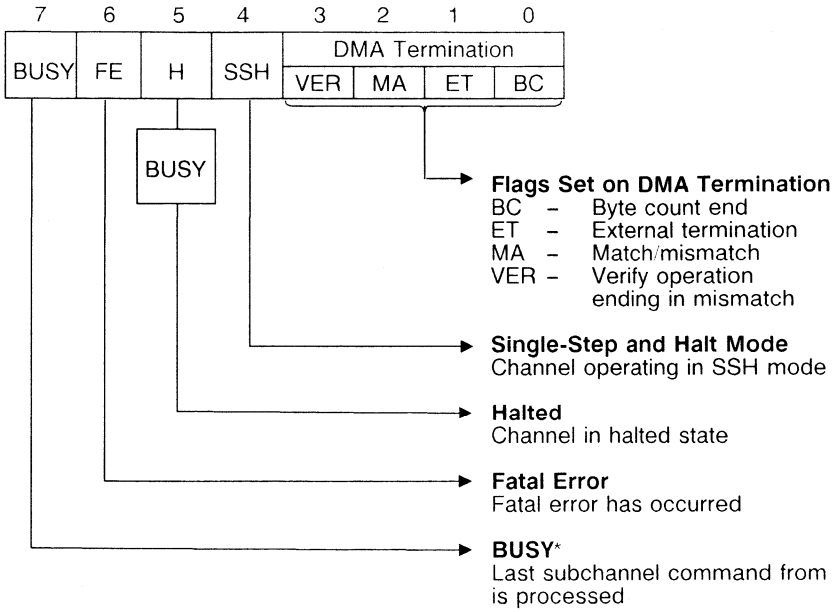


*) Unconditional JUMP when all condition code bits are set 1.

Channel Status Register

For each channel there is a channel status register (see figure below). This register shows the current state of the appropriate channel.

Channel Status Register



*) Valid only for channel 3 in multiplexer mode. In all other cases 0 is returned.

Multiplexer Channel Register

These registers are valid only for channel 3 if programmed as multiplexer channel.

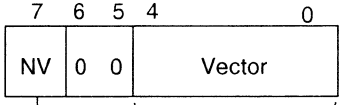
Multiplexer Table Pointer Register (MTPR)

This 24-bit register is used to reference the multiplexer table in memory (see figure „Structure of the Multiplexer Table"). It must be loaded by the CPU. Physically the list pointer register is used, since data chaining is not allowed for multiplexer channel.

Multiplexer Interrupt Vector Register (MIVR)

This 8-bit register is read by the CPU to determine which subchannels are stopped. The vectors of the stopped subchannels are output on subsequent read operations in the order of their priority (0 has highest priority).

Multiplexer Interrupt Vector Register (MIVR)



Subchannel Vector
Vector of the highest priority subchannel stopped and not yet read

Non-Valid
0 Vector is valid
1 Vector is not valid
(no channel stopped or all vectors read)

Last Vector Register (LVR)

The 8-bit register holds the last vector read by the SAB 82258A (from SAB 8259A). In case of a stop caused by a fatal error on channel 3, LVR determines the failing subchannel.

Subchannel Register (SCR)

The 8-bit register must be loaded by the CPU with the desired subchannel number before a subchannel command is written into GCR.

Timings

The bus timings in 286 and remote mode are identical to that for the SAB 80286, in 186 and 8086 mode the timings are identical to that for the SAB 80186. For exact timings see timing diagrams of AC Characteristics.

Asynchronous control inputs are specified with setup and hold times which are only important to determine whether the SAB 82258A responds to the signal in the current cycle or the next cycle.

The following pages hold two sections of AC characteristics and waveforms. The first section refers to 286 mode and remote mode, the second one to 186 mode and 8086 mode.

Absolute Maximum Ratings

Temperature under bias	0 to 70°C
Storage temperature	-65 to + 150°C
Voltage on any pin with respect to ground	-0.5 to + 7 V
Power dissipation	3.6 W

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics [1]

T_C = 0 to 100°C; V_{CC} = +5 V ± 10%

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage (except CLK)	V_{IL}	-0.5	+ 0.8	V	–
Input high voltage (except CLK)	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 3.0 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = -400 µA
Power supply current	I_{CC}	– –	550 385	mA mA	T_C = 0°C, (turn on) T_C = 100°C (steady operation) all outputs open
Input leakage current	I_{LI}				
S0#, S1#, S2#, BHE#, RD#, WR#, M/IO#		–	-200	µA	0 V ≤ V_{IN} ≤ V_{CC}
HOLD(RQ#/GT# mode), EOD#		–	-1.5	mA	0 V ≤ V_{IN} ≤ V_{CC}
A23 (AREADY),A21 [2]		–	-1.5	mA	0 V ≤ V_{IN} ≤ V_{CC}
other pins		–	± 10	µA	0 V ≤ V_{IN} ≤ V_{CC}
Output leakage current	I_{LO}	–	± 10	µA	0.45 V ≤ V_{OUT} ≤ V_{CC}
Clock input low voltage	V_{CL}	-0.5	+ 0.6	V	–
Clock input high voltage	V_{CH}	3.8	V_{CC} + 1.0	V	–

[1]) Clock must be applied.
[2]) This specification is valid only during RESET.

Capacitance

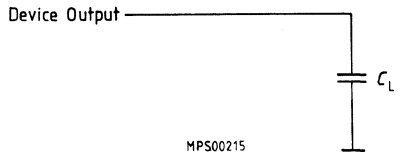
$T_C = 25°C$; V_{CC} = GND = 0 V, $f_c = 1$ MHz

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Capacitance of inputs (except CLK)	C_{IN}	–	10	pF	3)
Capacitance of I/O or outputs	C_{IO}	–	20	pF	3)
Capacitance of CLK input	C_{CLK}	–	12	pF	3)

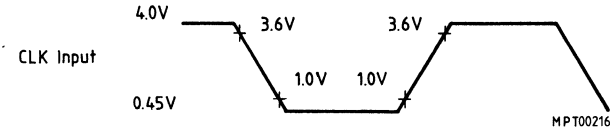
3) Not 100% tested, guaranteed by design characterization.

AC Testing Waveforms

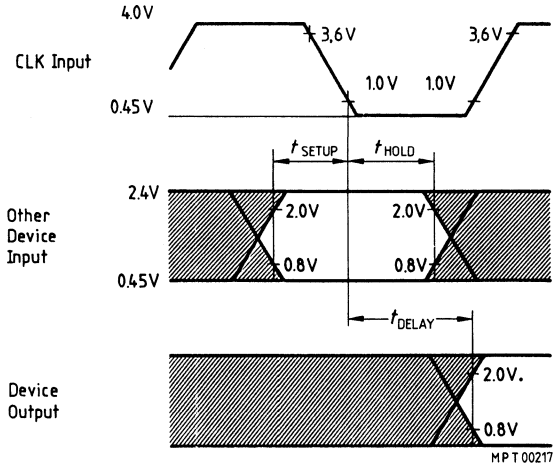
Test Loading on Outputs



Drive and Measurement Points – CLK Input



Setup, Hold and Delay Time Measurement – General



AC Characteristics (286 mode)

T_C = 0 to 100°C; V_{CC} = +5 V ±10%
Any output timing is measured at 1.5 V.

Parameter	Symbol	Limit Values		Unit	Test conditions
		min.	max.		
CLK cycle period	t_1	62	250	ns	–
CLK low time	t_2	15	230	ns	at 1.0 V
CLK high time	t_3	20	235	ns	at 3.6 V
Address/control output delay	t_4	–	60	ns	C_L = 100 pF
Status output delay	t_5	–	40	ns	C_L = 100 pF
Sync data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync READY# setup time	t_8	38	–	ns	–
Sync READY# hold time	t_9	25	–	ns	–
Sync control input setup time	t_{10}	20	–	ns	–
Sync control/address input hold time	t_{11}	20	–	ns	–
Sync address setup time	t_{12}	2.5	–	ns	–
Data/control output delay	t_{13}	–	50	ns	C_L = 100 pF
Data/control float delay	t_{14}	–	50	ns	–
BHE# setup time	t_{15}	60	–	ns	–
Write command width	t_{16}	4CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	2CLK + t_6 + t_{44}	–	ns	–
Async address setup time	t_{18}	t_{43}	–	ns	–
Async data access time	t_{19}	–	5CLK + t_{43} + t_{13}	ns	–

Parameter	Symbol	Limit Values		Unit	Test conditions
		min.	max.		
Mode select setup time	t_{28}	2CLK + 20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Command recovery time	t_{33}	4CLK + t_{43} + t_{44}	–	ns	–
CLK rise time	t_{34}	–	15	ns	1.0 to 3.6 V
CLK fall time	t_{35}	–	15	ns	3.6 to 1.0 V
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
CS# active response time	t_{37}	2CLK	22CLK + t_{43} + t_4	ns	1)
CS# active after BREL inactive	t_{39}	0	–	ns	–
HOLD active to HDLA active	t_{42}	0	–	ns	–
Async input setup time	t_{43}	20	–	ns	2)
Async input hold time	t_{44}	20	–	ns	2)
Async HLDA high time	t_{47}	2CLK + t_{43} + t_{44}	–	ns	3)
HOLD output low time	t_{49}	4CLK- t_{13}	–	ns	–
HLDA low to HOLD low delay	t_{50}	6CLK	22CLK + t_{43} + t_{13}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
CS# hold time	t_{56}	*40*	–	ns	–
DACK# output delay	t_{59}	–	50	ns	–

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 22 CLK
- normal pointer transfer (3 bus cycles): 16 CLK
- splitted pointer transfer (4 bus cycles): 20 CLK

If wait states are used, the time required for the wait states of three of four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

AC Characteristics SAB 82258A-1 (286 mode)

T_C = 0 to 85°C; V_{CC} = +5 V ±5%
Any output timing is measured at 1.5 V.

Parameter	Symbol	Limit Values		Unit	Test conditions
		min.	max.		
CLK cycle period	t_1	50	250	ns	–
CLK low time	t_2	12	234	ns	at 1.0 V
CLK high time	t_3	16	238	ns	at 3.6 V
Address/control output delay	t_4	–	47	ns	C_L = 100 pF
Status output delay	t_5	–	28	ns	C_L = 100 pF
Sync data setup time	t_6	8	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync READY# setup time	t_8	26	–	ns	–
Sync READY# hold time	t_9	25	–	ns	–
Sync control input setup time	t_{10}	20	–	ns	–
Sync control/address input hold time	t_{11}	20	–	ns	–
Sync address setup time	t_{12}	2.5	–	ns	–
Data/control output delay	t_{13}	–	40	ns	C_L = 100 pF
Data/control float delay	t_{14}	–	47	ns	–
BHE# setup time	t_{15}	45	–	ns	–
Write command width	t_{16}	4CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	2CLK + t_6 + t_{44}	–	ns	–
Async address setup time	t_{18}	t_{43}	–	ns	–
Async data access time	t_{19}	–	5CLK + t_{43} + t_{13}	ns	–

Parameter	Symbol	Limit Values		Unit	Test conditions
		min.	max.		
Mode select setup time	t_{28}	2CLK +20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Command recovery time	t_{33}	4CLK + t_{43} + t_{44}	–	ns	–
CLK rise time	t_{34}	–	8	ns	1.0 to 3.6 V
CLK fall time	t_{35}	–	8	ns	3.6 to 1.0 V
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
CS# active response time	t_{37}	2CLK	22CLK + t_{43} + t_4	ns	1)
CS# active after BREL inactive	t_{39}	0	–	ns	–
HOLD active to HDLA active	t_{42}	0	–	ns	–
Async input setup time	t_{43}	20	–	ns	2)
Async input hold time	t_{44}	20	–	ns	2)
Async HLDA high time	t_{47}	2CLK + t_{43} + t_{44}	–	ns	3)
HOLD output low time	t_{49}	4CLK -t_{13}	–	ns	–
HLDA low to HOLD low delay	t_{50}	6CLK	22CLK + t_{43} + t_{13}	ns	1)
Read command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
CS# hold time	t_{56}	*40*	–	ns	–
DACK# output delay	t_{59}	–	40	ns	–

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 22CLK
- normal pointer transfer (3 bus cycles): 16 CLK
- splitted pointer transfer (4 bus cycles): 20 CLK

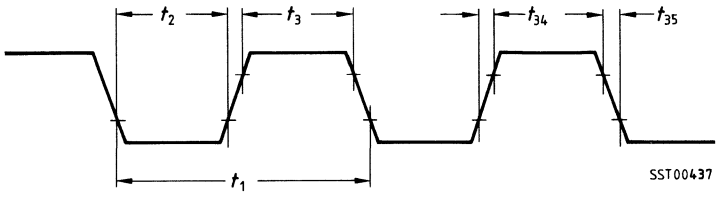
If wait states are used, the time required for the wait states of three of four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

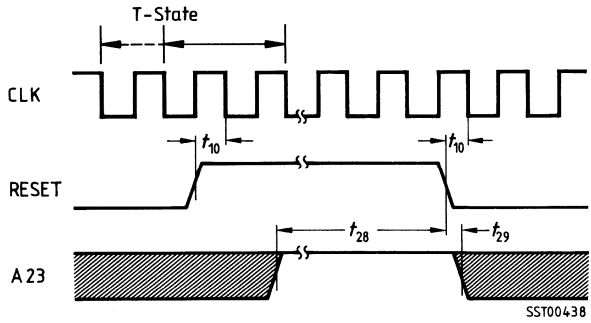
3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

Waveforms

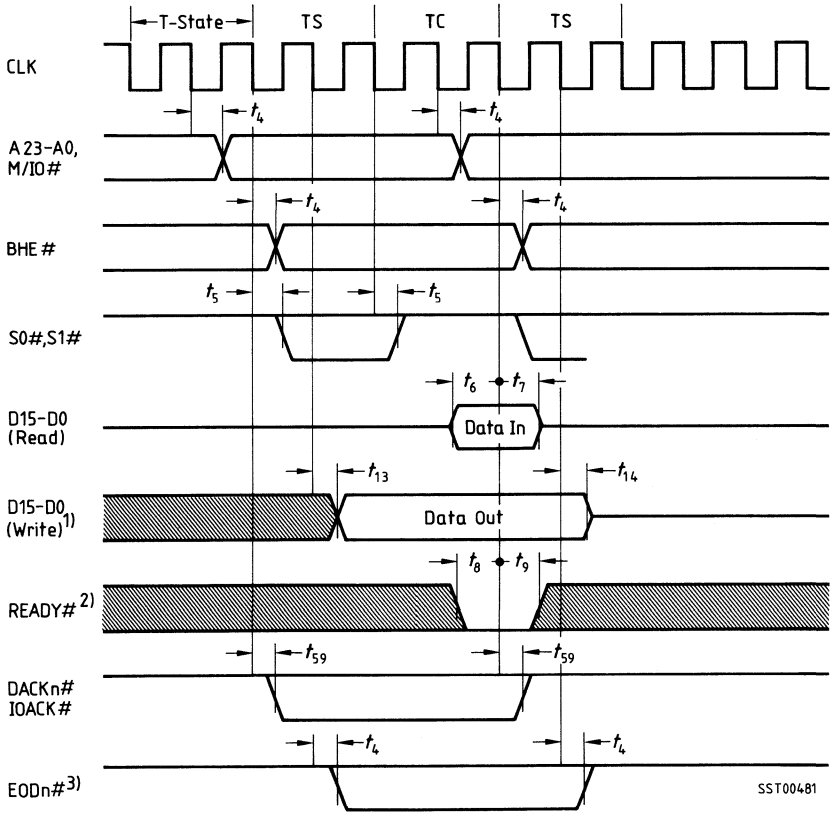
Clock Signal (286 mode)



Mode Selection on RESET (286 mode)

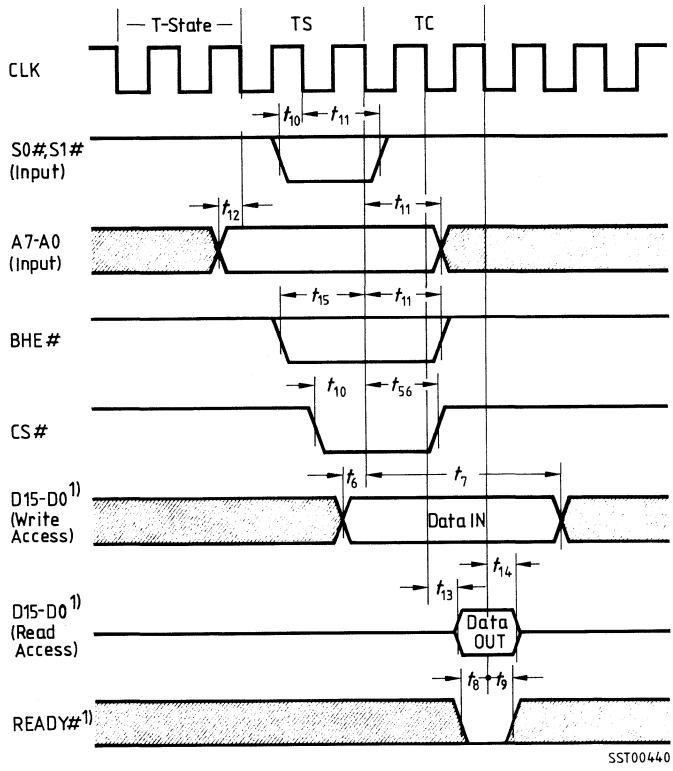


Major Timing for Active Bus Cycles (286 mode)



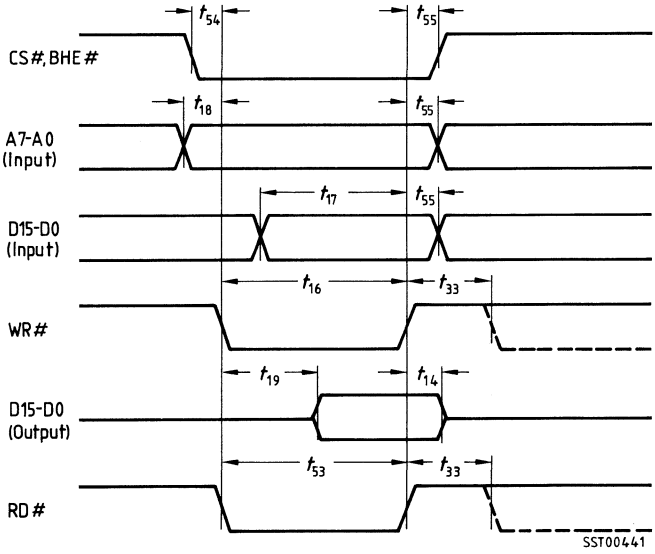
1) If executing a single cycle transfer, D15 to D0 float like during read cycles!
2) TC will be repeated, if READY# is inactive at the sampling point (end of current TC).
3) Initiated by terminal count.

Synchronous Access (286 mode)

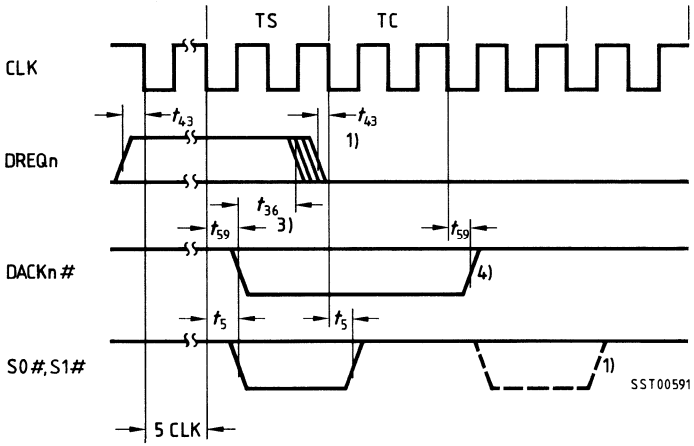


1) The processor will repeat TC, if READY# is not active at the sampling point (end of current TC). The SAB 82258A will output data until the end of the repeated TC (read access) or sample the data bus again at the beginning of the repeated TC (write access).

Asynchronous Access (286 mode)

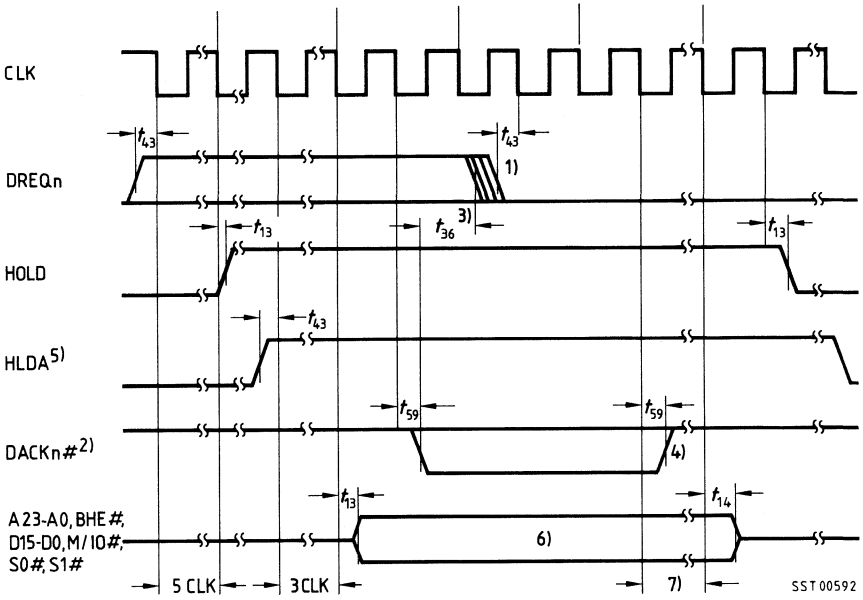


DMA Control Without Bus Arbitration (286 mode)



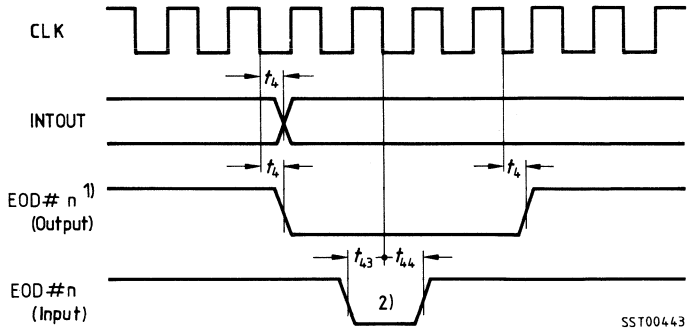
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) Minimum time to execute bus cycle.
4) If the SAB 82258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

DMA Control With Bus Arbitration (286 mode)



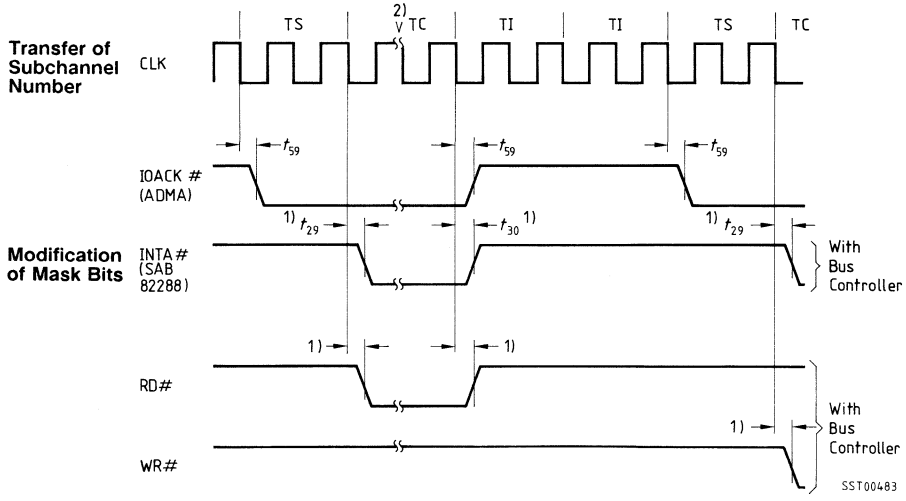
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) Minimum time to execute bus cycle.
4) If the SAB 82258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.
5) The SAB 82258A can be forced off the bus by driving HDLA inactive (see "Bus Arbitration").
6) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycle".
7) The SAB 82258A may execute additional bus cycles, e.g. for command chaining.

EOD#/INTOUT Timing (286 mode)



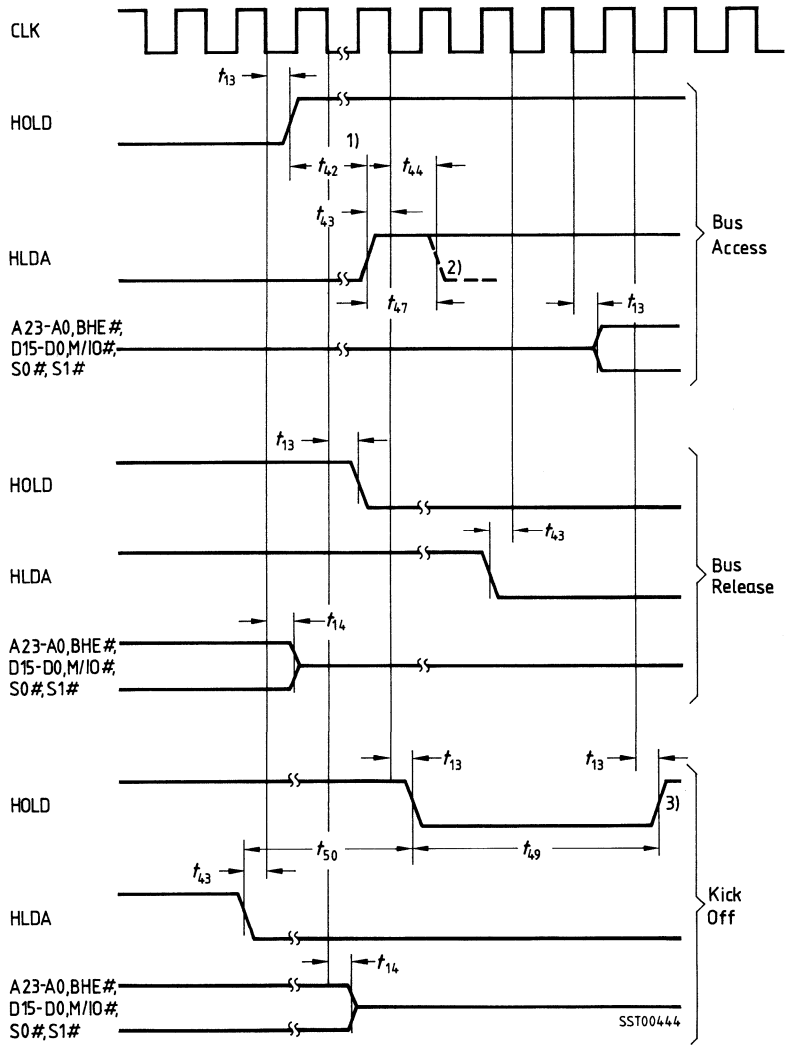
1) Initiated by type 2 command.
2) EOD# input minimum pulse width is 3 CLKs, if the signal is asynchronous.

Access to SAB 8259A (286 mode)



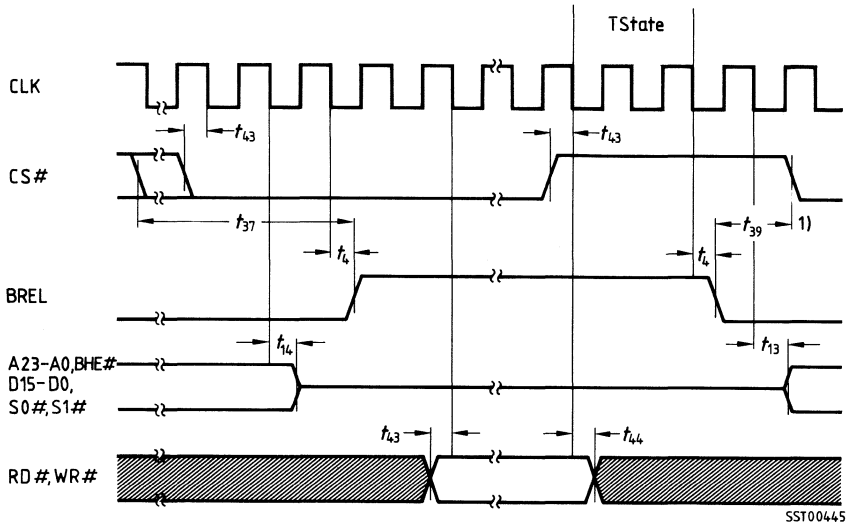
1) These timings are SAB 82288 timings!
2) Additional wait states may be inserted.

Bus Arbitration (286 mode)



1) To avoid arbitration conflicts, HLDA should not become active before HOLD.
2) Minimum HLDA high time before kick-off to respond to HOLD signal.
3) Earliest possible reactivation of HOLD after deactivation of HLDA.

Access in Remote Mode



1) Required to avoid bus conflicts.

This diagram shows the times when the output signals are driven active and input signals are recognized, rather than the exact timing.

AC Characteristics SAB 82258A (186 mode)

T_C = 0 to 100°C; V_{CC} = +5 V ±10%
Any output timing is measured at 1.5 V.

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Control output delay	t_4	–	60	ns	–
Sync address data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync control input setup time	t_{10}	20	–	ns	–
Sync control/address input hold time	t_{11}	20	–	ns	–
Data/control delay	t_{13}	–	50	ns	C_L = 100 pF
Data float delay	t_{14}	–	50	ns	–
Write command width	t_{16}	2CLK +40	–	ns	–
Async data setup time	t_{17}	1CLK +30	–	ns	–
Async address setup time	t_{18}	20	–	ns	–
Async data access time	t_{19}	–	2CLK + t_{22} + t_{43} + t_{13}	ns	–
CLK cycle period	t_{20}	125	500	ns	–
CLK low time	t_{21}	55	–	ns	at 1.5 V
CLK high time	t_{22}	55	–	ns	at 1.5 V
CLK rise time	t_{23}	–	15	ns	1.0 to 3.5 V
CLK fall time	t_{24}	–	15	ns	3.5 to 1.0 V
AREADY active setup time	t_{25}	20	–	ns	2)
AREADY hold time	t_{26}	15	–	ns	2)
AREADY inactive setup time	t_{27}	35	–	ns	–
Mode select setup time	t_{28}	2CLK +20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Address/data output delay	t_{30}	10	50	ns	C_L = 20 to 200 pF
Status output delay	t_{31}	10	55	ns	–
Float delay	t_{32}	10	50	ns	–

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Command recovery time	t_{33}	2CLK + t_{43} + t_{44}	–	ns	–
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
ALE output delay	t_{38}	–	40	ns	-
Address control input hold time	t_{40}	10	–	ns	–
Address input setup time	t_{41}	20	–	ns	–
HOLD active to HDLA active	t_{42}	0	–	ns	–
Async control input setup time	t_{43}	20	–	ns	2)
Async control input hold time	t_{44}	20	–	ns	2)
HLDA hold time	t_{45}	10	–	ns	-
Async HLDA high time	t_{46}	1CLK + t_{43} + t_{45}	–	ns	3)
HOLD output delay	t_{48}	5	70	ns	–
HLDA output low time	t_{51}	2CLK -t_{48max}	–	ns	-
HLDA low to HOLD low delay	t_{52}	3CLK	15CLK + t_{43} + t_{48}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
SREADY hold time	t_{57}	15	–	ns	–
Status setup time	t_{58}	35	–	ns	–
DACK output delay	t_{60}	–	60	ns	–
Status hold time	t_{61}	10			

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 15 CLK
- normal pointer transfer (3 bus cycles): 12 CLK
- splitted pointer transfer (4 bus cycles): 16 CLK

If wait states are used, the time required for the wait states of three of four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

AC Characteristics SAB 82258A-1 (186 mode)

T_C = 0 to 85°C; V_{CC} = +5 V ±5%
Any output timing is measured at 1.5 V.

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Control output delay	t_4	–	56	ns	–
Sync address data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync control input setup time	t_{10}	20	–	ns	–
Sync control/address input hold time	t_{11}	20	–	ns	–
Data/control delay	t_{13}	–	40	ns	C_L = 100 pF
Data float delay	t_{14}	–	40	ns	–
Write command width	t_{16}	2CLK +40	–	ns	–
Async data setup time	t_{17}	1CLK +30	–	ns	–
Async address setup time	t_{18}	20	–	ns	–
Async data access time	t_{19}	–	2CLK + t_{22} + t_{43} + t_{13}	ns	–
CLK cycle period	t_{20}	100	500	ns	–
CLK low time	t_{21}	44	–	ns	at 1.5 V
CLK high time	t_{22}	44	–	ns	at 1.5 V
CLK rise time	t_{23}	–	12	ns	1.0 to 3.5 V
CLK fall time	t_{24}	–	12	ns	3.5 to 1.0 V
AREADY active setup time	t_{25}	15	–	ns	2)
AREADY hold time	t_{26}	15	–	ns	2)
AREADY inactive setup time	t_{27}	25	–	ns	–
Mode select setup time	t_{28}	2CLK +20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Address/data output delay	t_{30}	10	40	ns	C_L = 20 to 200 pF
Status output delay	t_{31}	10	45	ns	–
Float delay	t_{32}	10	40	ns	–

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Command recovery time	t_{33}	2CLK + t_{43} + t_{44}	–	ns	–
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
ALE output delay	t_{38}	–	35	ns	-
Address control input hold time	t_{40}	10	–	ns	–
Address input setup time	t_{41}	20	–	ns	–
HOLD active to HDLA active	t_{42}	0	–	ns	–
Async control input setup time	t_{43}	20	–	ns	2)
Async control input hold time	t_{44}	20	–	ns	2)
HLDA hold time	t_{45}	5	–	ns	-
Async HLDA high time	t_{46}	1CLK + t_{43} + t_{45}	–	ns	3)
HOLD output delay	t_{48}	5	60	ns	–
HLDA output low time	t_{51}	2CLK -t_{48max}	–	ns	-
HLDA low to HOLD low delay	t_{52}	3CLK	15CLK + t_{43} + t_{48}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
SREADY hold time	t_{57}	15	–	ns	–
Status setup time	t_{58}	35	–	ns	–
DACK# output delay	t_{60}	–	56	ns	–
Status hold time	t_{61}	10	–	ns	–

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 15 CLK
- normal pointer transfer (3 bus cycles): 12 CLK
- splitted pointer transfer (4 bus cycles): 16 CLK

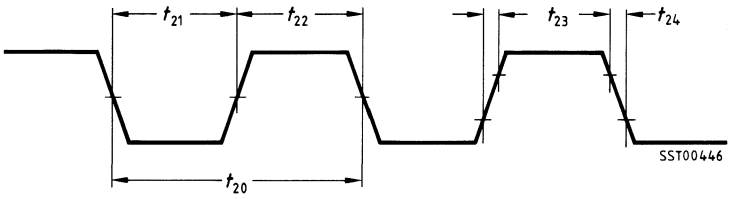
If wait states are used, the time required for the wait states of three of four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

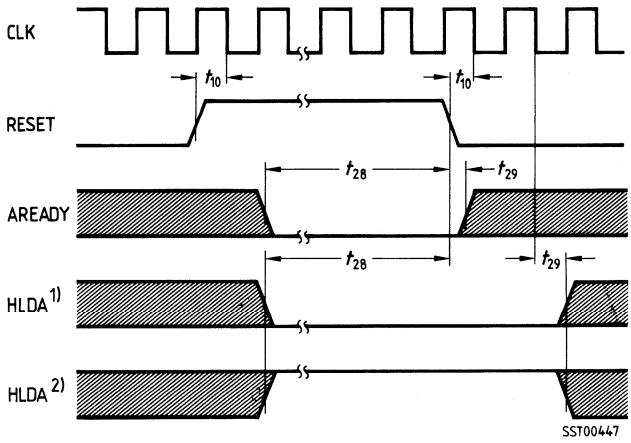
3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

Waveforms

Clock Signal (186 mode)

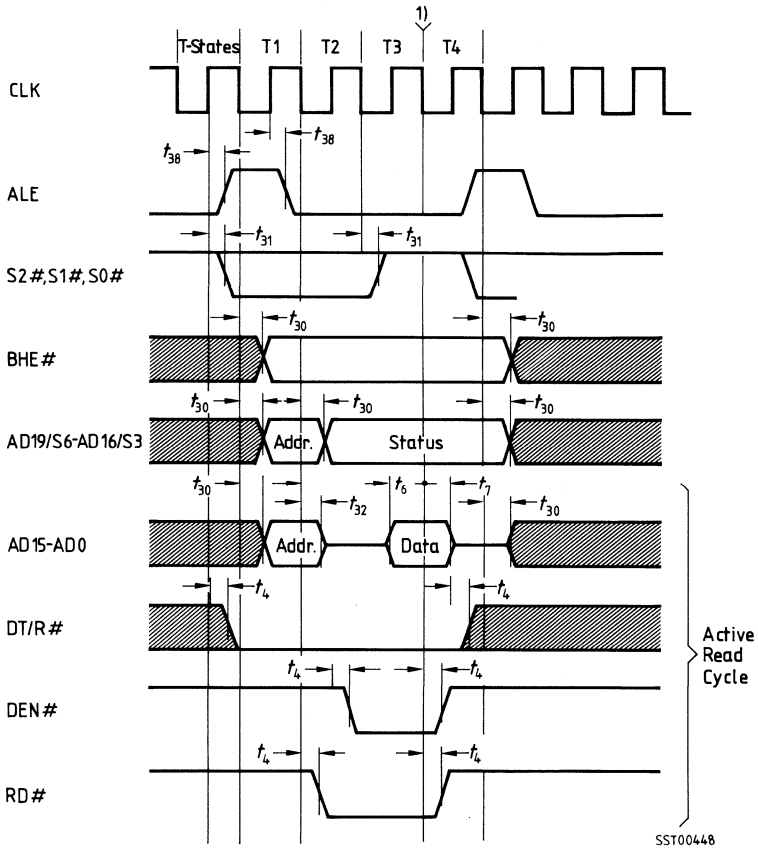


Mode Selection on RESET (186 mode)



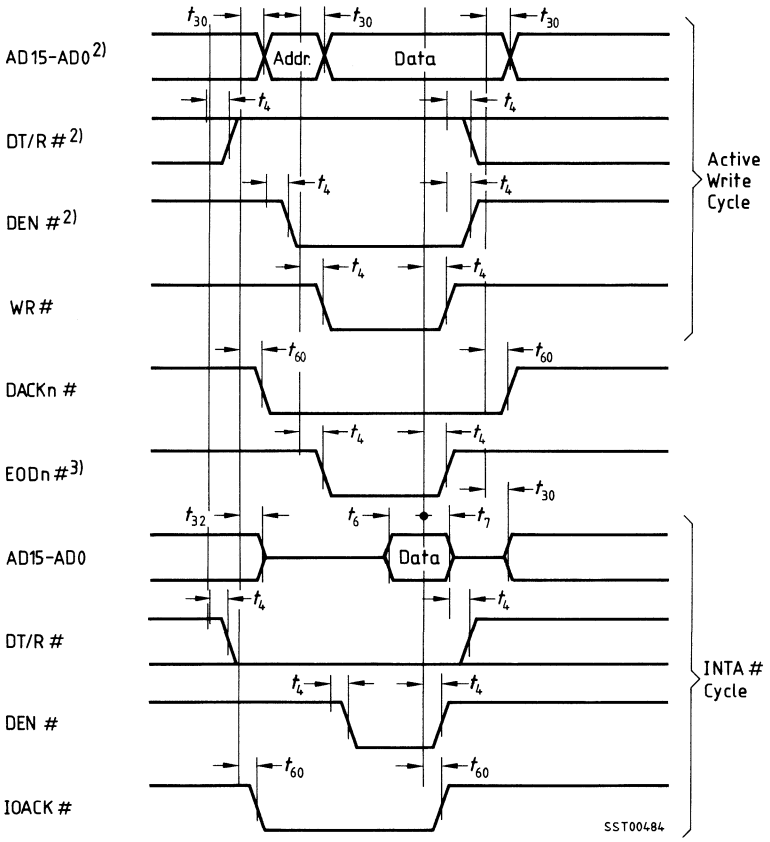
1) To operate in 186 mode with HOLD/HLDA protocol.
2) To operate in 8086 mode with RQ#/GT# protocol.

Major Timing for Active Bus Cycle (186 mode) a)



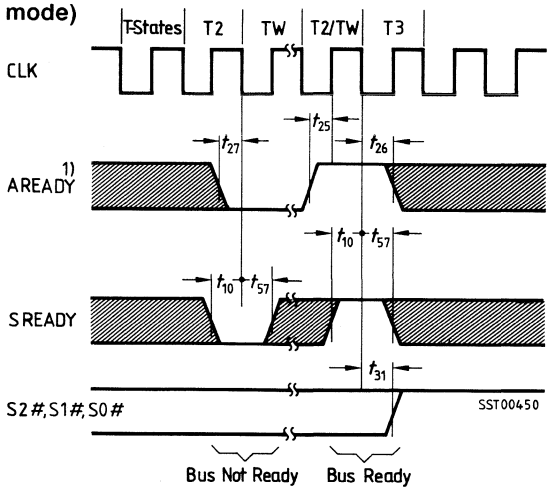
1) A wait state is inserted after T3 or TW, whenever the bus is not ready at the beginning of T3 or TW (see "Bus Cycle Termination"). The status must be valid just prior to T4.

Major Timing for Active Bus Cycle (186 mode) b)



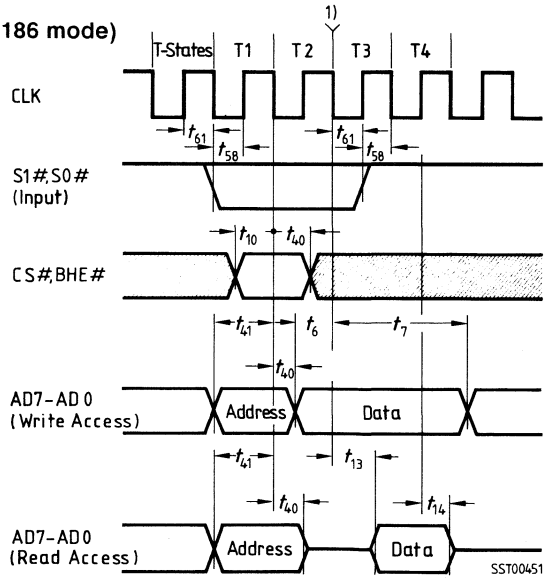
2) For a single-cycle transfer the timing of AD15-AD0,DT/R# and DEN# is identical to a read cycle. AD15-AD0 will float as during a read cycle.
3) Initiated by terminal count.

Bus Cycle Termination (186 mode)



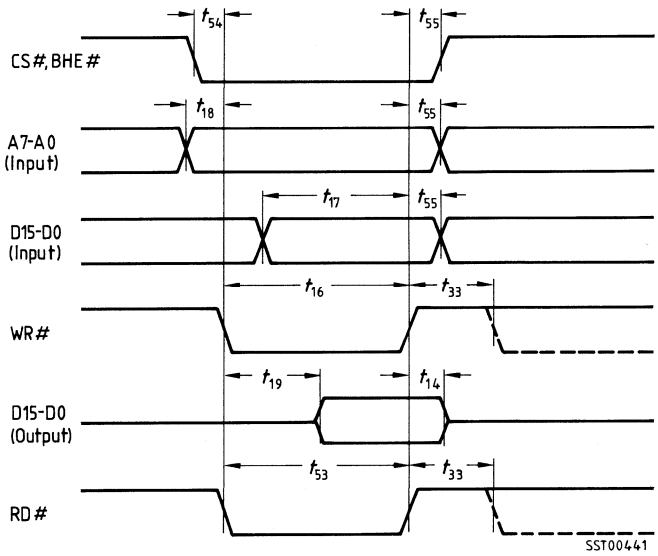
1) Only the rising edge of AREADY is synchronized internally to CLK. The falling edge must be synchronized externally.

Synchronous Access (186 mode)

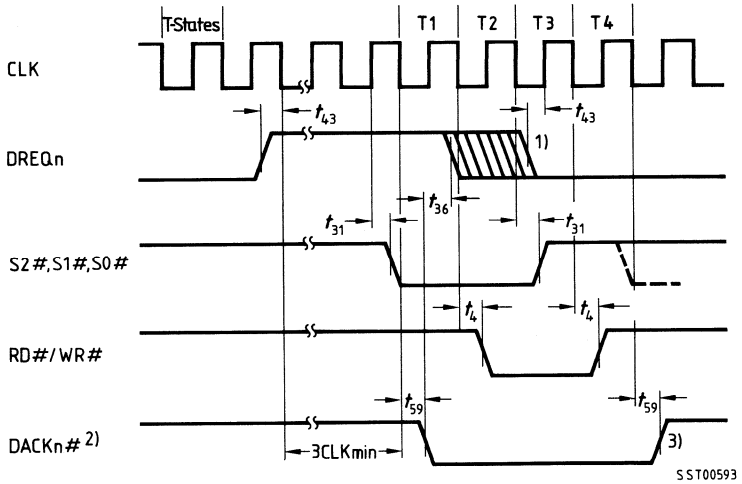


1) Additional wait cycles may be inserted. Status must be valid just prior to T4.

Asynchronous Access (186 mode)

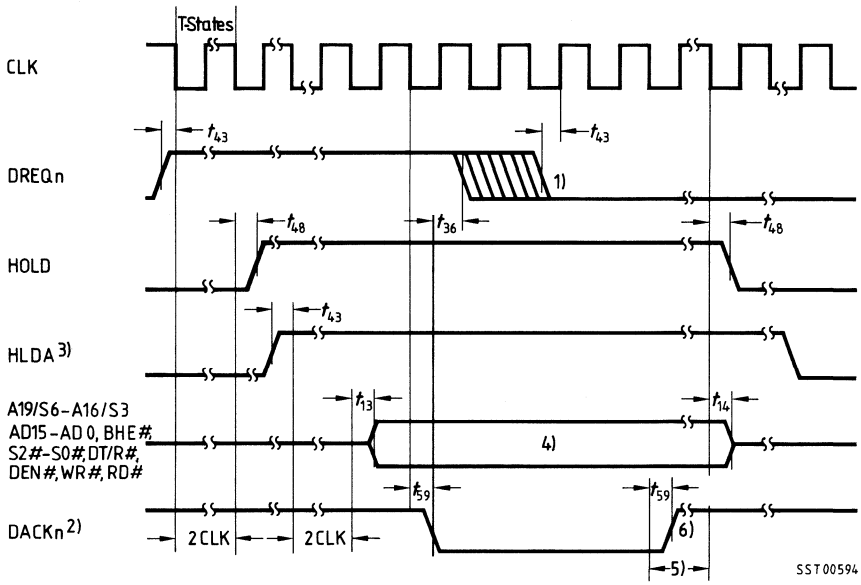


DMA Control Without Bus Arbitration (186 mode)



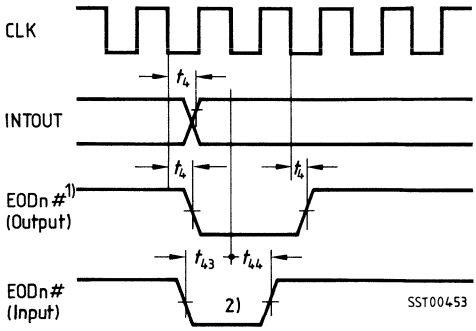
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) If the SAB 82258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

DMA Control With Bus Arbitration (186 mode)



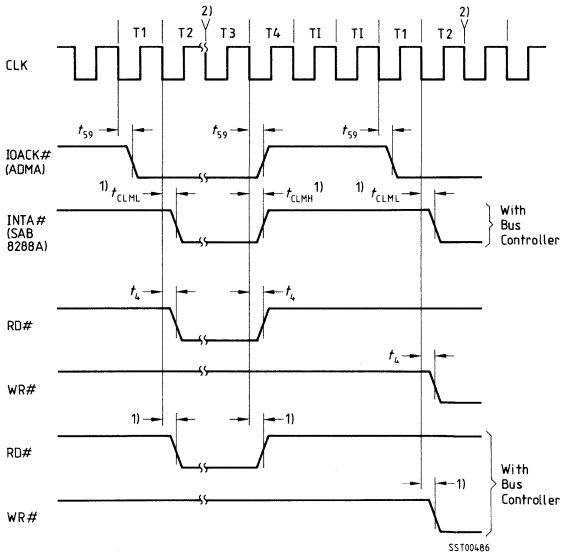
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) The SAB 82258A can be forced off the bus by driving HDLA inactive (see "Bus Arbitration").
4) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycle".
5) The SAB 82258A may execute additional bus cycles, e.g. for command chaining.
6) If the SAB 82258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

EOD#/INTOUT Timing (186 mode)



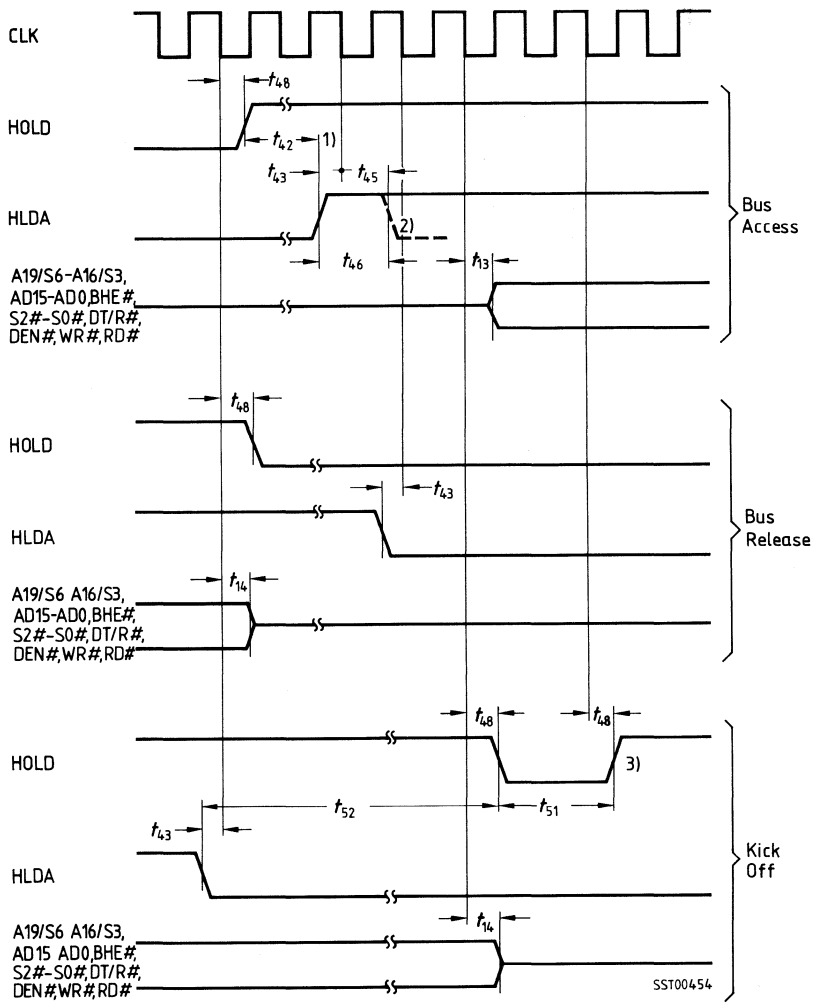
1) Initiated by type 2 command.
2) EOD# input minimum pulse width is 2 CLKs, if the signal is asynchronous.

Access to SAB 8259A (186 mode)



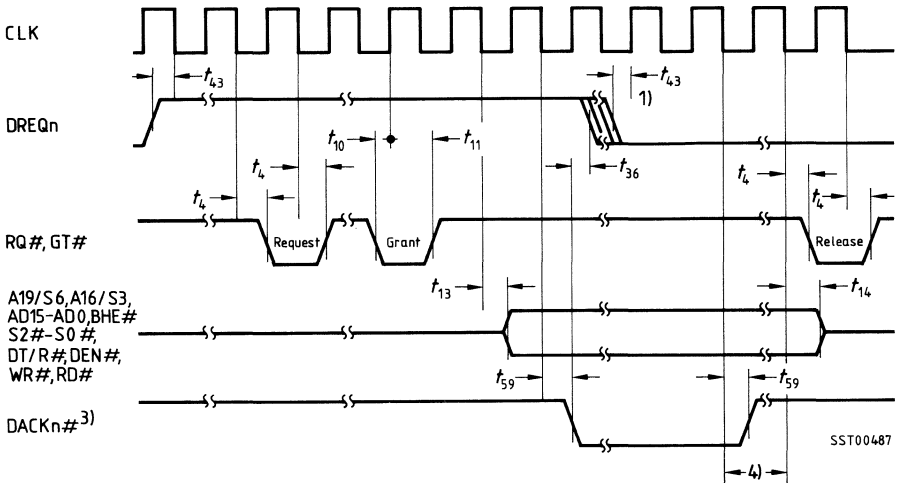
1) These timings are SAB 8288A timings!
2) Additional wait states may be inserted.

Bus Arbitration (186 mode)



1) To avoid arbitration conflicts, HLDA should not become active before HOLD.
2) Minimum HLDA high time before kick-off to respond to HOLD signal.
3) Earliest possible reactivation of HOLD after deactivation of HLDA.

DMA Control with RQ#/GT# Protocol (8086 mode)



1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent bus cycles are executed.
2) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".
3) Refers to the highest priority request. Acknowledge of lower priority requests may be delayed by higher priority requests.
4) The SAB 82258A may execute additional bus cycles, e.g. for command chaining.

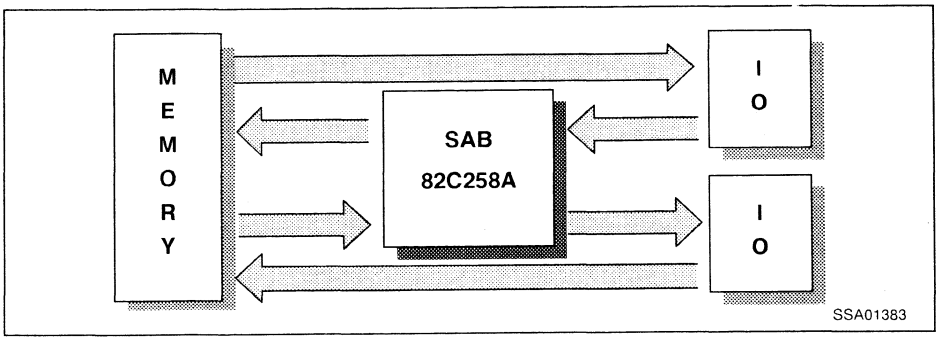
SIEMENS

Advanced DMA Controller SAB 82C258A
for 16-/32-Bit Microcomputer Systems

Advance Information **CMOS**

SAB 82C258A-1	**10 MHz**	**SAB 82C258A-12**	**12.5 MHz**
SAB 82C258A-16	**16 MHz**	**SAB 82C258A-20**	**20 MHz**

- Fully compatible with the SAB 82258A (hardware, software and pin-out). Upward-compatible with the SAB 82258
- Supports 32-bit fly-by transfers
- 4 independent high-speed DMA channels
- Multiplexer channel operation supporting up to 32 subchannels
- Adaptive on-chip bus interface for direct connection to 16-/8-bit processors
- Standalone operation for modular systems
- Programmable bus loading
- 16 Mbytes addressing range
- 16 Mbytes maximum block size
- Transfer rates up to 40 Mbytes/s (20 MHz system)
- Command chaining for automatic processing
- Automatic data chaining (scattering/ gathering) for flexible data structures
- "On-the-fly" compare, translate and verify operations
- Single and double cycle transfers
- Automatic data assembly/disassembly
- Memory-based communication scheme
- Package: PL-CC-68

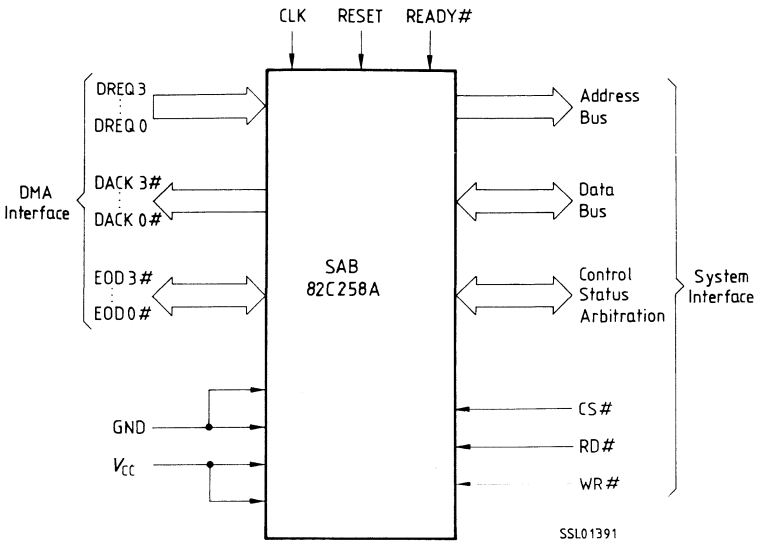


The SAB 82C258A is an advanced DMA (direct memory access) controller especially designed for the 16-bit microprocessors SAB 80286 and SAB 8086/186/88/188. In addition the operation with other processors is supported by the remote mode. The 32-bit fly-by transfer mode supports operation with 32-bit microprocessors (like 80386). The SAB 82C258A has 4 independent DMA channels which can transfer data at rates up to 20 Mbytes/second at 20 MHz clock frequency in an SAB 80286 system or up to 10 Mbytes/second at 20 MHz in an SAB 8086/80186 system. Using 32-bit fly-by transfers it can transfer 40 Mbytes/second at 20 MHz. This great bandwidth allows the user to handle very fast data transfers or a large number of concurrent peripherals.
The device is fabricated in Siemens ACMOS technology and comes in a 68-pin plastic leaded chip carrier (PL-CC-68).

Ordering Information

Type	Ordering code	Package	Function
SAB 82C258A-1-N	Q67120-P312	PL-CC-68	Advanced DMA controller, 10 MHz
SAB 82C258A-12-N	Q67120-P313	PL-CC-68	Advanced DMA controller, 12.5 MHz
SAB 82C258A-16-N	Q67120-P314	PL-CC-68	Advanced DMA controller, 16 MHz
SAB 82C258A-20-N	Q67120-P323	PL-CC-68	Advanced DMA controller, 20 MHz

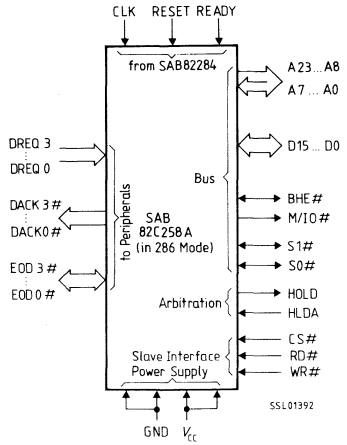
Logic Symbol



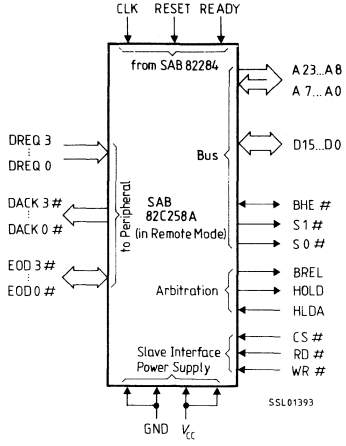
Modes of Operation, Adaptive Bus Interface

The SAB 82C258A has been defined to work with all 16-bit processors linke SAB 80286, SAB 80186/188 and SAB 8086/88 without additional support and interface logic. Hence the local buses of the above processors are different in signals, functions and timings, the SAB 82C258A has an adaptive bus interface to meet the different requirements of these local buses.

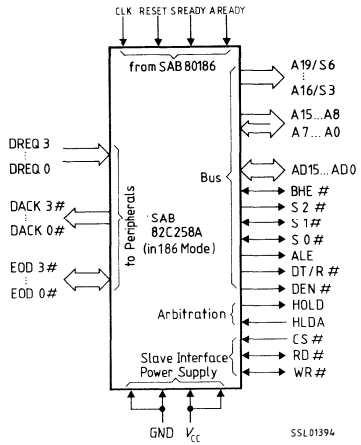
Logic Symbol in 286 Mode



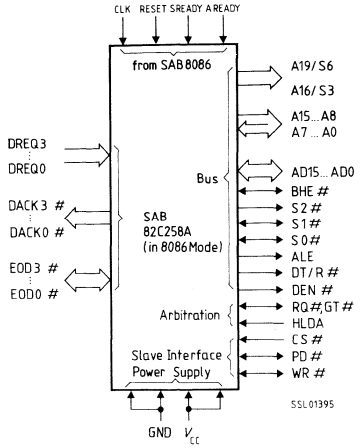
Logic Symbol in Remote Mode



Logic Symbol in 186 Mode



Logic Symbol in 8086 Mode

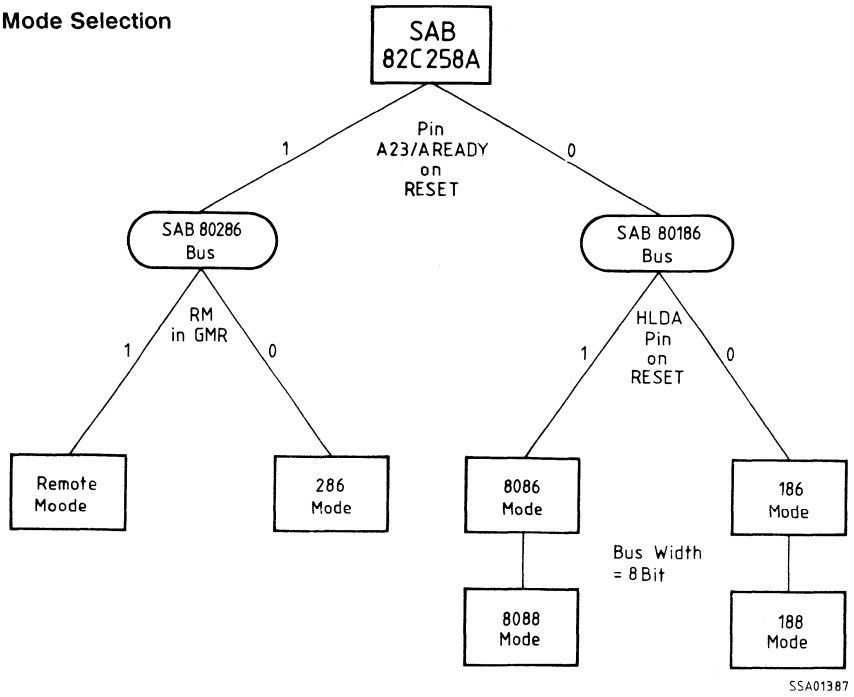


As a result of this, a bus compatibility with identical timing is attained with the processors SAB 80286, SAB 80186 and SAB 8086. A compatibility with the 8-bit bus versions of these processors, SAB 8088 and SAB 80188, is also guaranteed by defining the physical bus width of the SAB 82C258A (per software) as 8 bits. The only difference in operation with SAB 8086 or SAB 80186 is that for SAB 8086 the HOLD pin functions as RQ#/GT# line (if HLDA is held high on reset).

The SAB 82C258A can also be operated in remote or standalone mode, in which case it is not coupled directly to a processor. In remote mode, the SAB 82C258A can be operated as sole bus master in a multimaster environment. The SAB 82C258A is programmed to a specific mode of operation by applying defined logic levels to certain pins during reset and by setting the status of several control bits (see figure below).

Note: *Pin 57 (A21/DT/R# of the SAB 82C258A) must be high during reset in order to enable proper operation. This is provided if pin A21 is connected to the SAB 80286's address bus. An internal pullup resistor supports applications where pin 57 is left open.*

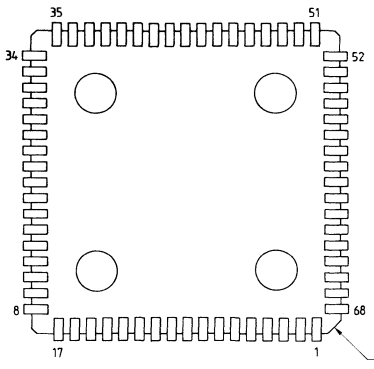
Mode Selection



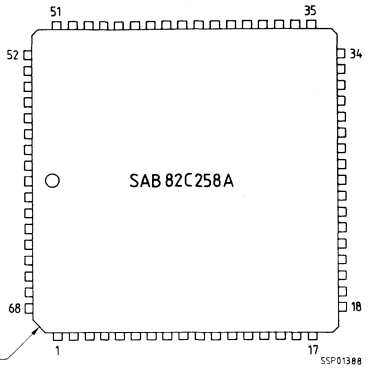
Pin 57 (A21 or DT/R#) must be high during Reset to enter the desired operating mode. An internal pullup pulls this pin high, if nothing is driving it.

Pin Configuration

PL-CC-68
Bottom view



PL-CC-68
Top view



Pin Definitions and Functions

Some pins of the SAB 82C258A serve for different purposes according to the different modes of bus operation. The table below summarizes the pinouts of the SAB 82C258A in the various modes. A detailed description of the general pin functions as well as the mode-specific pin functions is given in the following sections.

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
16	HOLD	O	HOLD	O	HOLD or RQ#/GT#	O (186) I/O (8086)
17	HLDA	I	HLDA	I	HLDA	I
1	BHE#	I/O	BHE#	I/O	BHE#	I/O
14	M/IO#	O	BREL	O	S2#	O
11	S1#	I/O	S1#	O	S1#	I/O
13	S0#	I/O	S0#	O	S0#	I/O
8	CS#	I	CS#	I	CS#	I
2	RD#	I	RD#	I	RD#	I/O
3	WR#	I	WR#	I	WR#	I/O
10	READY#	I	READY#	I	SREADY	I
59	A23	O	A23	O	AREADY	I
58	A22	O	A22	O	ALE	O
57	A21	O	A21	O	DT/R#	O
56	A20	O	A20	O	DEN#	O
55	A19	O	A19	O	A19/S6	O
54	A18	O	A18	O	A18/S5	O
53	A17	O	A17	O	A17/S4	O
52	A16	O	A16	O	A16/S3	O
51	A15	O	A15	O	A15	O
50	A14	O	A14	O	A14	O
49	A13	O	A13	O	A13	O
48	A12	O	A12	O	A12	O
47	A11	O	A11	O	A11	O
46	A10	O	A10	O	A10	O
45	A9	O	A9	O	A9	O
44	A8	O	A8	O	A8	O
42	A7	I/O	A7	I/O	A7	I/O
41	A6	I/O	A6	I/O	A6	I/O
40	A5	I/O	A5	I/O	A5	I/O
39	A4	I/O	A4	I/O	A4	I/O

Pin Definitions and Functions (cont'd)

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
38	A3	I/O	A3	I/O	A3	I/O
37	A2	I/O	A2	I/O	A2	I/O
36	A1	I/O	A1	I/O	A1	I/O
35	A0	I/O	A0	I/O	AO	I/O
18	D15	I/O	D15	I/O	AD15	I/O
20	D14	I/O	D14	I/O	AD14	I/O
22	D13	I/O	D13	I/O	AD13	I/O
24	D12	I/O	D12	I/O	AD12	I/O
27	D11	I/O	D11	I/O	AD11	I/O
29	D10	I/O	D10	I/O	AD10	I/O
31	D9	I/O	D9	I/O	AD9	I/O
33	D8	I/O	D8	I/O	AD8	I/O
19	D7	I/O	D7	I/O	AD7	I/O
21	D6	I/O	D6	I/O	AD6	I/O
23	D5	I/O	D5	I/O	AD5	I/O
25	D4	I/O	D4	I/O	AD4	I/O
28	D3	I/O	D3	I/O	AD3	I/O
30	D2	I/O	D2	I/O	AD2	I/O
32	D1	I/O	D1	I/O	AD1	I/O
34	D0	I/O	D0	I/O	AD0	I/O
7	DREQ0	I	DREQ0	I	DREQ0	I
6	DREQ1	I	DREQ1	I	DREQ1	I
5	DREQ2	I	DREQ2	I	DREQ2	I
4	DREQ3	I	DREQ3	I	DREQ3	I
61	DACK0#	O	DACK0#	O	DACK0#	O
62	DACK1#	O	DACK1#	O	DACK1#	O
63	DACK2#	O	DACK2#	O	DACK2#	O
64	DACK3#	O	DACK3#	O	DACK3#	O
65	EOD0#	I/O	EOD0#	I/O	EOD0#	I/O
66	EOD1#	I/O	EOD1#	I/O	EOD1#	I/O
67	EOD2#	I/O	EOD2#	I/O	EOD2#	I/O
68	EOD3#	I/O	EOD3#	I/O	EOD3#	I/O
15	RESET	I	RESET	I	RESET	I
12	CLK	I	CLK	I	CLK	I
9,43	GND	–	GND	–	GND	–
26,60	V_{CC}	–	V_{CC}	–	V_{CC}	–

Pin Definitions for All Operating Modes

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>BHE#</td><td>1</td><td>I/O</td><td>BUS HIGH ENABLE
This active low input indicates transfer of data on the upper byte of the data bus, D15 to D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use BHE# to condition chip select functions. BHE# floats to tristate off when the SAB 82C258A does not own the bus.
BHE# and A0 encodings
<table>
<tr><th>BHE#</th><th>A0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer (D15-D8)</td></tr>
<tr><td>0</td><td>1</td><td>Byte transfer on upper half of data bus (D15-D8)</td></tr>
<tr><td>1</td><td>0</td><td>Byte transfer on lower half of data bus (D7-D0)</td></tr>
<tr><td>1</td><td>1</td><td>Odd-addressed byte on 8-bit bus (D7-D0)</td></tr>
</table></td></tr>
<tr><td>RD#</td><td>2</td><td>I</td><td>READ
This active low input in conjunction with chip select enables reading the SAB 82C258A register which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82C258A clock.</td></tr>
<tr><td>WR#</td><td>3</td><td>I</td><td>WRITE
This active low input in conjunction with chip select enables writing into the SAB 82C258A registers which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82C258A clock.</td></tr>
<tr><td>DREQ0-
DREQ3</td><td>4-7</td><td>I</td><td>DMA REQUEST (0 TO 3)
These active high inputs are used for synchronized DMA transfers. DREQ3 has the meaning of I/O request (IOREQ) if channel 3 is a multiplexer channel. These signals can be asynchronous to the SAB 82C258A clock.</td></tr>
</table>

Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CS#	8	I	**CHIP SELECT** This active low input enables the access of a processor to SAB 82C258A registers. This access is additionally controlled either by bus status signals or by the read or write command signals. Chip select can be asynchronous to the SAB 82C258A clock.
CLK	12	I	**CLOCK** This input provides the fundamental timing. In 286 mode and remote mode it must be two times the system clock. It can be directly connected to the SAB 82284 CLK output. It is divided by two to generate the SAB 82C258A internal clock. The on-chip divide-by-two circuitry can be synchronized to the external clock generator by a low-to-high transition on the RESET input, or by the first high-to-low transition on the status inputs S0# or S1# after reset. In 186/8086 mode no internal prescaling is done.
S0#, S1#	11, 13	I/O	**BUS STATUS LINES (0, 1)** These signals control the support circuits. The beginning of a bus cycle is indicated by S1# or S0# or both going active. The termination of a bus cycle is indicated by all status signals going inactive in 186 mode or bus ready signal (READY#) going active in 286 mode. The type of bus cycle is indicated by S0#, S1# and S2# (in 186 mode) or M/IO# (in 286 mode). S2# and M/IO# have the same meaning but in 186 mode the S2# signal can be active only when at least one of S1# or S0# is active, whereas in 286 mode the M/IO# signal is valid with the address on the address lines. The SAB 82C258A can generate the following bus cycles by activating the status signals (and M/IO# in 286 mode):

Pin Definitions for All Operating Modes (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>S0#,S1#
(cont'd)</td><td>11, 13</td><td>I/O</td><td>
<table>
<tr><th>M/IO#
or S2#</th><th>S1#</th><th>S0#</th><th>Cycle Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Read I/O-vector
(for multiplexer channel)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from I/O space</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into I/O space</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle, does not occur
in 186 mode</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read from memory space</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write into memory space</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No bus cycle</td></tr>
</table>

When the SAB 82C258A is not the master of the local bus the status signals are used as inputs for detection of synchronous accesses to the SAB 82C258A. The following table shows the bus status and CS# signals and their interpretation by the SAB 82C258A.
<table>
<tr><th>CS#</th><th>S1#</th><th>S0#</th><th>Description</th></tr>
<tr><td>1</td><td>X</td><td>X</td><td>SAB 82C258A is not
selected (no action)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No SAB 82C258A
access (no action)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from an
SAB 82C258A register</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into an
SAB 82C258A register</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle[1)]</td></tr>
</table>
</td></tr>
</table>

1) SAB 82C258A is selected but no synchronous access is activated. In this case the SAB 82C258A monitors RD# and WR# signals for detection of an asynchronous access.

Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
RESET	15	I	**SYSTEM RESET** An activation of the reset signal forces the SAB 82C258A to the initial state. The reset signal must be synchronous to CLK.
DACK0#-DACK3#	61-64	O	**DMA ACKNOWLEDGE (0 TO 3)** These active low inputs acknowledge the requests on the related DREQn signals. They are activated when the requested transfer(s) is (are) performed. If the channel 3 is a multiplexer channel the signal DACK3# has the meaning of I/O acknowledge (IOACK#).
EOD0#-EOD3#	65-68	I/O	**END OF DMA (0 TO 3)** These lines are implemented as open drain output drivers with a high impedance pullup resistor and thus can be used as bidirectional lines. As **outputs** the lines are activated for two system clock cycles at the end of the DMA transfer of the corresponding channel (if enabled) or they are activated under program control (EOD output or interrupt output). If the lines are held internally high but forced to low by external circuitry, they act as "End of DMA" **inputs.** The current transfer is aborted and the SAB 82C258A continues with the next command. Additionally, a special function is possible with the EOD2# pin: this pin can also be used as common interrupt signal for all 4 channels. In this mode this line is not an open drain output but a pushpull output (output only). The other EOD# pins may be used as EOD# outputs/inputs as described above.
V_{CC}	26, 60		**POWER SUPPLY** (+ 5 V)
GND	9, 43		**GROUND** (0 V)

Pin Definitions for 286 Mode and Remote Mode

In 286 mode the SAB 82C258A bus signals and bus timings are the same as for the SAB 80286 processor. Additional features of the SAB 82C258A require a slight change in pin definitions. The processor can access internal registers of the SAB 82C258A. Therefore the bus signals must support these accesses. This means that some of the bus control signals must be bidirectional and some additional bus control signals are necessary. All additional pins and their functions are listed below.

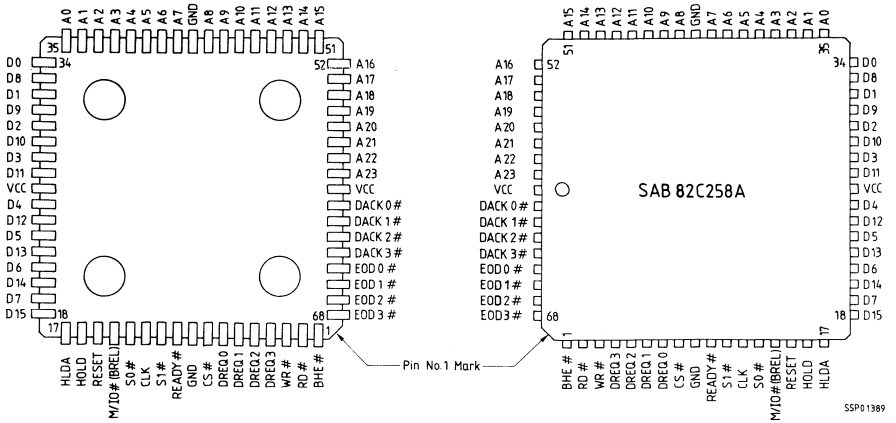
In **remote mode** most of the bus signals are the same as in 286 mode. Pin 14 (M IO#) serves as BREL output. The HOLD/HLDA arbitration in remote mode is used only for system bus accesses, the resident bus is accessed directly.

The CS# input additionally requests access to the local bus of the SAB 82C258A. These accesses are enabled through the BREL output after the SAB 82C258A has released the bus.

Pin Configuration in 286 Mode and Remote Mode

Component Pad View – As viewed from underside of component when mounted on the board

PC Board View – As viewed from the component side of the pc board



Pin Definitions for 286 Mode and Remote Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
READY#	10	I	**BUS READY** This active low input terminates a bus cycle. Bus cycles are extended without limit until terminated by READY# low. READY# is a synchronous input requiring setup and hold times relative to the system clock to be met for correct operation.
M/IO#	14 (286 mode)	O	**Memory / I/O SELECT** In 286 mode, pin 14 is used to distinguish between memory and I/O space addresses.
BREL	14 (remote mode)	O	**BUS RELEASE** In remote mode pin 14 is used to indicate when the SAB 82C258A has released the control of the local bus.
HOLD	16	O	**BUS HOLD REQUEST** This active high output indicates a request for control of the local bus (286 mode) or the system bus (remote mode). When the SAB 82C258A relinquishes the bus it drops the HOLD output. HOLD is connected to the bus arbiter in remote mode.
HLDA	17	I	**BUS HOLD ACKNOWLEDGE** This active high input indicates that the SAB 82C258A can acquire the control of the bus. When it goes low SAB 82C258A must relinquish the bus at the end of its current cycle. HLDA can be asynchronous to the SAB 82C258A clock. HLDA is connected to the bus arbiter in remote mode.
D0-D15	18-25, 27-34	I/O	**DATA BUS (0 TO 15)** This is the bidirectional 16-bit data bus. For use with an 8-bit bus, only the lower 8 data lines D7-D0 are relevant.
A0-A7	35-42	I/O	**ADDRESS BUS (0 TO 7)** The lower 8 address lines for DMA transfers. They are also used to input the register address when the processor accesses an SAB 82258A register.
A8-A23	44-59	O	**ADDRESS BUS (8 TO 23)** Higher address outputs.

Pin Definitions for 186 Mode and 8086 Mode

In 186 mode and 8086 mode the SAB 82C258A multiplexes the address with data and additional status lines.

Pins A0 to A15 retain their original function while pins A20 to A23 serve for different purposes (not used for address in 186/8086 mode).

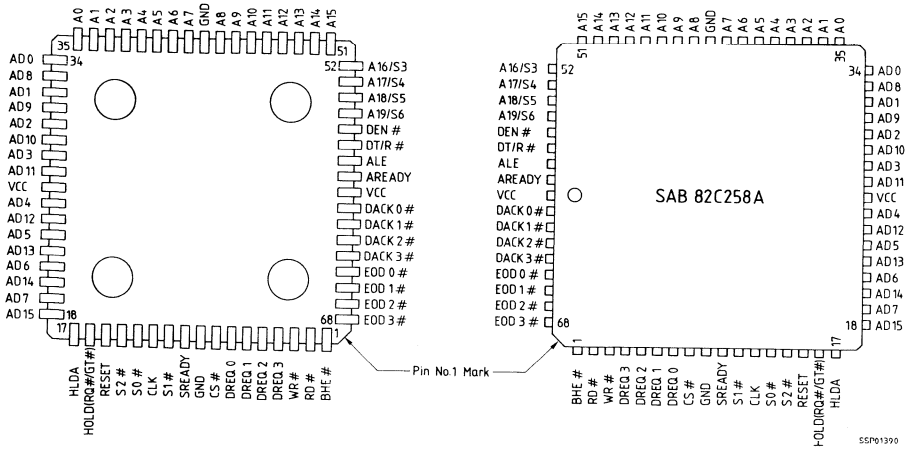
The RD# and WR# lines are additionally used as outputs in 186/8086 mode to support minimum mode systems.

Note that the HLDA input can be used to force the SAB 82C258A off the bus in 8086 mode, even though the arbitration is done via the RQ#/GT# line!

Pin Configuration in 186 Mode and 8086 Mode

Component Pad View – As viewed from underside of component when mounted on the board

PC Board View – As viewed from the component side of the pc board



Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ALE	58	O	**ADDRESS LATCH ENABLE** This active high output provides a strobe signal to separate the address information on the multiplexed AD lines.
DEN#	56	O	**DATA ENABLE** This active low output enables the data transceivers.
DT/R#	57	O	**DATA TRANSMIT/RECEIVE** This signal controls the direction of the data transceivers. When low, data is transferred to the SAB 82C258A, when high, the SAB 82C258A places data onto the data bus.
S2#	14	O	**STATUS LINE 2** Signal as for SAB 186/8086/88 processors (see also S1#, S0# description in 286 mode).
AREADY	59	I	**ASYNCHRONOUS READY** The rising edge of this signal is internally synchronized, the falling edge must be synchronous to CLK. During reset this signal must be low to enter 186 mode.
SREADY	10	I	**SYNCHRONOUS READY** This signal must be synchronized externally. The use of this pin permits a relaxed system-timing specification by eliminating the clock phase which is required for resolving the signal level when using the AREADY input.
AD0-AD15	18-25 27-34	I/O	**ADDRESS/DATA BUS (0 to 15)** Lower address and data information is multiplexed on pin AD0 to AD15.
A0-A7 A8-A15	35-42 44-51	I/O O	**ADDRESS BUS (0 to 15)** Additionally the demultiplexed address information is available on address pin A0 to A15.

Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A16/S3-A19/S6	52–55	O	**ADDRESS BUS (16 TO 19)/ STATUS LINES (3 TO 6)** The higher address bits are multiplexed with additional status information.
HLDA	17	I	**BUS HOLD ACKNOWLEDGE** This active high input indicates that the SAB 82C258A can acquire the control of the bus. When it goes low the SAB 82C258A must relinquish the bus at the end of its current bus cycle. HLDA can be asynchronous to the SAB 82C258A clock. In 8086 mode, HLDA can be used to force the SAB 82C258A off the bus.
HOLD	16 (186 mode)	O	**BUS HOLD REQUEST** This active high output indicates a request for control of the bus. When the SAB 82C258A relinquishes the bus, it drops the HOLD output.
RQ#/ GT#	16 (8086 mode)	I/O	**REQUEST/GRANT** In 8086 mode the HOLD output acts as RQ#/GT# line. The RQ#/GT# protocol implements a one-line communication dialog required to arbitrate the use of the system bus normally done via HOLD/HLDA. The RQ#/GT# signal is active low and has an internal pullup resistor.

Functional Description

General

The SAB 82C258A is an advanced general-purpose DMA controller especially designed for efficient highspeed data transfers on an SAB 80286 bus as well as on an SAB 80186/188 or SAB 8086/88 bus.

It supports two basic operating modes:

- local mode (tightly coupled to a processor) and
- remote mode (loosely coupled to a processor).

In the first case the SAB 82C258A is directly coupled to the CPU and uses the same system support/control devices as the CPU (see figure below). This mode is possible with the above-mentioned processors.

As a second basic operating mode remote (standalone) mode is supported (see figure below). Here the SAB 82C258A has its own sets of bus interface circuits and thus can utilize its own local bus. This allows the DMA controller to work in parallel with the main CPU and therefore overall system performance can be increased. Besides, this mode is very useful for the design of modular systems and allows connecting the SAB 82C258A to any other processor via the system bus independent of the processor's local bus.

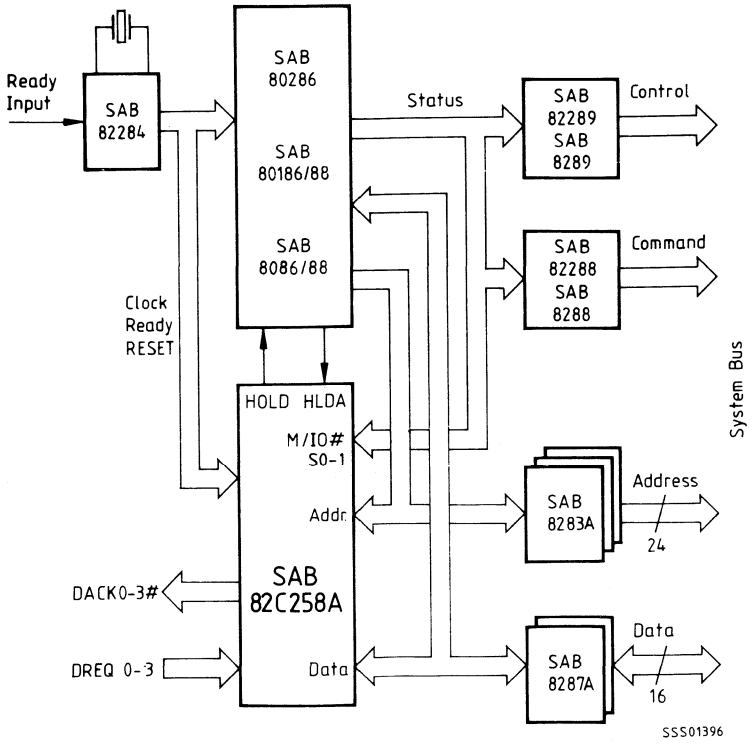
The SAB 82C258A has four independent DMA channels that can transfer up to 20 Mbytes/s in single cycle mode (2 clocks/transfer). In 2-cycle transfer mode the maximum rate is 10 Mbytes/s. Switching between channels induces no time penalty. Thus the overall maximum transfer rate of 20 Mbytes/s is also valid for multiple channel operation.

This fast operation is possible because of the pipelined architecture of the SAB 82C258A which allows the different functional units to work in parallel. The maximum transfer rate can be doubled to 40 Mbytes/s (in a 20 MHz system), if the SAB 82C258A executes 32-bit fly-by transfers.

The SAB 82C258A supports two address spaces, memory space and I/O space, each with a maximum address range of 16 Mbytes. In addition, the maximum block length (byte count) is also 16 Mbytes to support applications where large blocks of data have to be transferred (e.g. graphics).

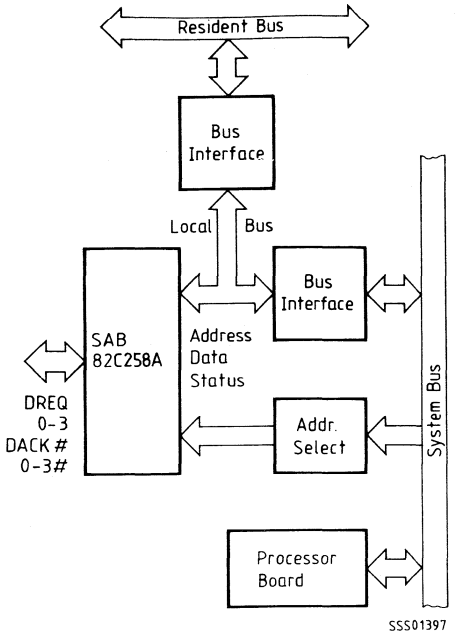
Basic SAB 82C258A Operating Modes

a) Local Mode



Basic SAB 82C258A Operating Modes

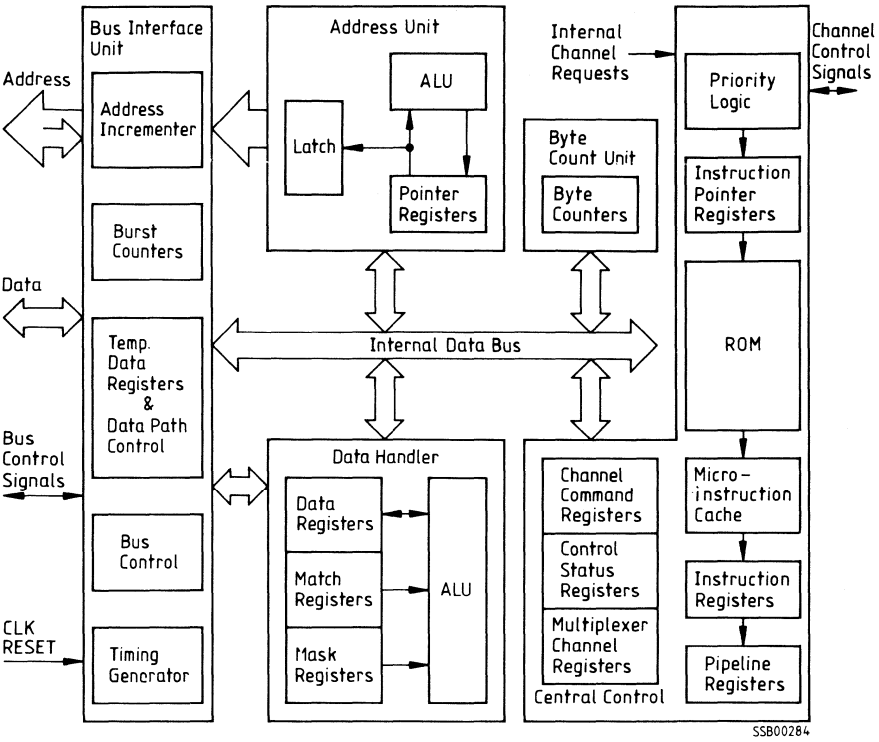
b) Remote Mode



As source or as destination, four parameters can be selected independently:

- address space (memory or I/O)
- physical bus width (8 bits or 16 bits)
- logical bus width (same as physical bus width or 8 bits on a 16-bit physical bus) and
- transfer direction (increasing, decreasing, fixed pointer or constant value).

Block Diagram of the SAB 82C258A



If the physical bus width of source or destination differs from the logical bus width, an automatic byte/word assembly (word/byte disassembly) takes place. The same is true, if the logical bus widths of source and destination are not identical.

Transfers between different address spaces can be performed within one or two cycles, transfers within one address space can be performed only in two cycles.

The transfers can be executed free running or externally synchronized via DREQ where source or destination synchronization is possible.

In summary, this very symmetrical operation of the SAB 82C258A gives the user a great amount of design flexibility.

Adaptive Bus Interface

As shown in the figure on page 4, the SAB 82C258A bus interface has two basic timing modes: the 286 mode and the 186 mode. In 286 mode the SAB 82C258A is directly coupled to an SAB 80286, in 186 mode to an SAB 80186 or SAB 80188. For each of these two modes a slightly different variation exists:

- For the 286 mode the variation is the remote mode, where the SAB 82C258A operates as a bus master on the system bus without being directly coupled to a processor. In this mode the SAB 82C258A can utilize its own local bus and the communication with the main processor is done via the system bus. To enable access to SAB 82C258A registers by the main processor, the SAB 82C258A must release its local bus. This "local bus arbitration" in remote mode is done via the CS# and BREL lines.
- For the 186 mode the variation is the 8086 mode, where the SAB 82C258A supports the RQ#/GT# protocol and thus can be directly coupled to an SAB 8086 or SAB 8088.

Memory-Based Communication

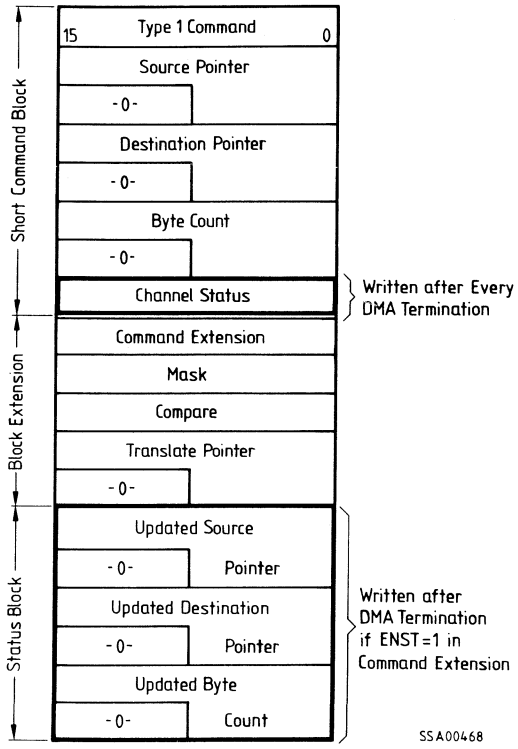
The normal communication between the SAB 82C258A and the processor is memory-based. This means that all necessary data for a transfer is contained in a command block in memory accessible for CPU and SAB 82C258A (see figure below). To start the transfer the CPU loads one of the command pointer registers of the SAB 82C258A with the address of the command block and then issues a "start channel command". Getting the command the SAB 82C258A loads the entire command block from memory into its on-chip channel registers and executes it. On completing the operation, channel status information is written back by the SAB 82C258A into the channel status word contained in the command block in memory.

If desired, the actual contents of the channel registers, i.e. source pointer, destination pointer and byte count it transferred to the channel status block. The channel status block immediately follows the command block in memory (see figure below).

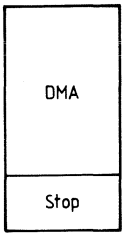
Command Chaining

Command blocks for any channel can be chained for sequential execution (see figure). When the SAB 82C258A has completed the execution of a command, it automatically increments the command pointer and starts to fetch and execute the next command block until a stop command is found. As a result a chain of command blocks can be executed by the SAB 82C258A without any CPU intervention. Due to conditional and unconditional STOP and JUMP commands, quite complex sequences of DMA can be executed by the SAB 82C258A.

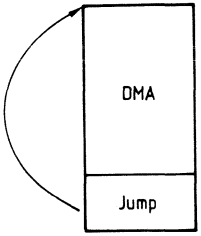
Memory-Based Communication



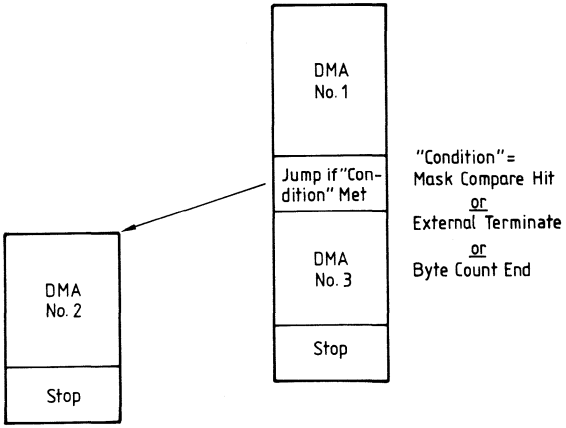
Command Chaining



a) Simplest DMA Operation



b) Auto-Reload DMA



c) Conditional DMA Operation SSA00469

Data Chaining

Data chaining allows an automatic, dynamic linking of data blocks scattered in memory. There are two types: list and linked-list data chaining.

If for a DMA the source blocks are to be dynamically linked during DMA, it is called source chaining and the effect is that of gathering data blocks and sending them out effectively as one block.

If one source block is dynamically broken up into multiple destination blocks, it is called destination chaining. This results in scattering of a block.

This dynamic linking and unlinking of data blocks makes the logical sequencing of data independent of its physical sequencing in memory.
In the case of linked list chaining (see figure a) each data block has a descriptor containing information on position of the data block in memory, length of the data block and a pointer to the next descriptor.

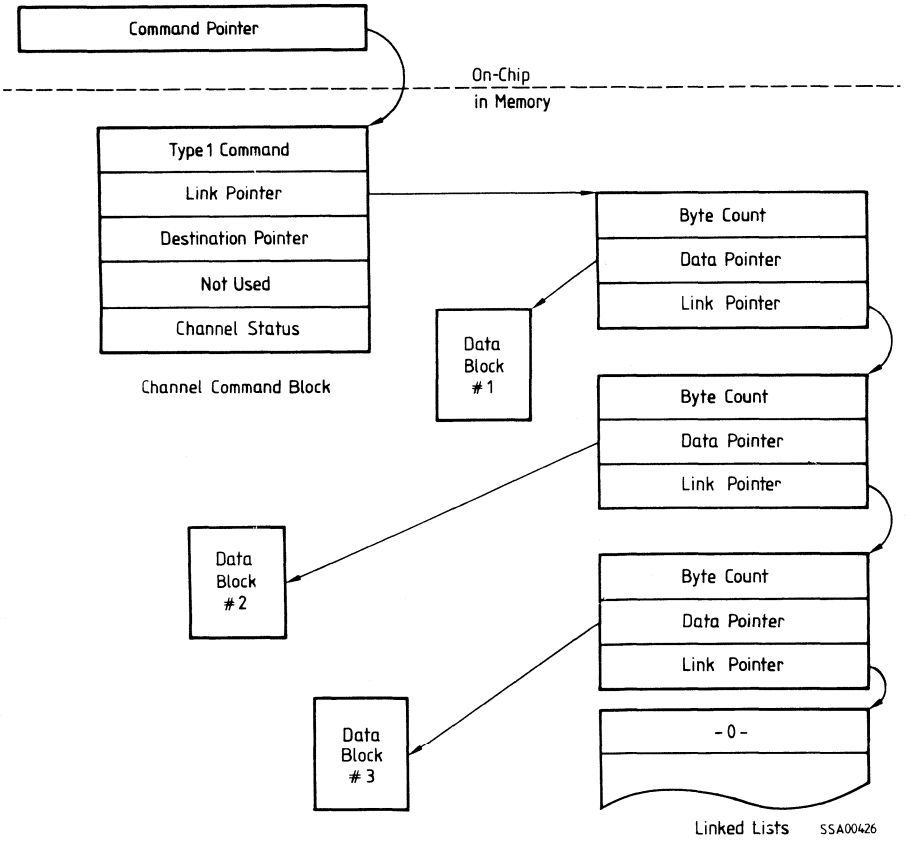
During data transfer the data block 1 is sent out first, then 2 and so on till a "0" is encountered in the byte count field.

The second type of data chaining is list chaining (see figure b).

Unlike linked list chaining, here the data block descriptors are continuous in a block and thus determine the sequence of data blocks. The flexibility lost in terms of predefined sequence is gained in terms of linking time.

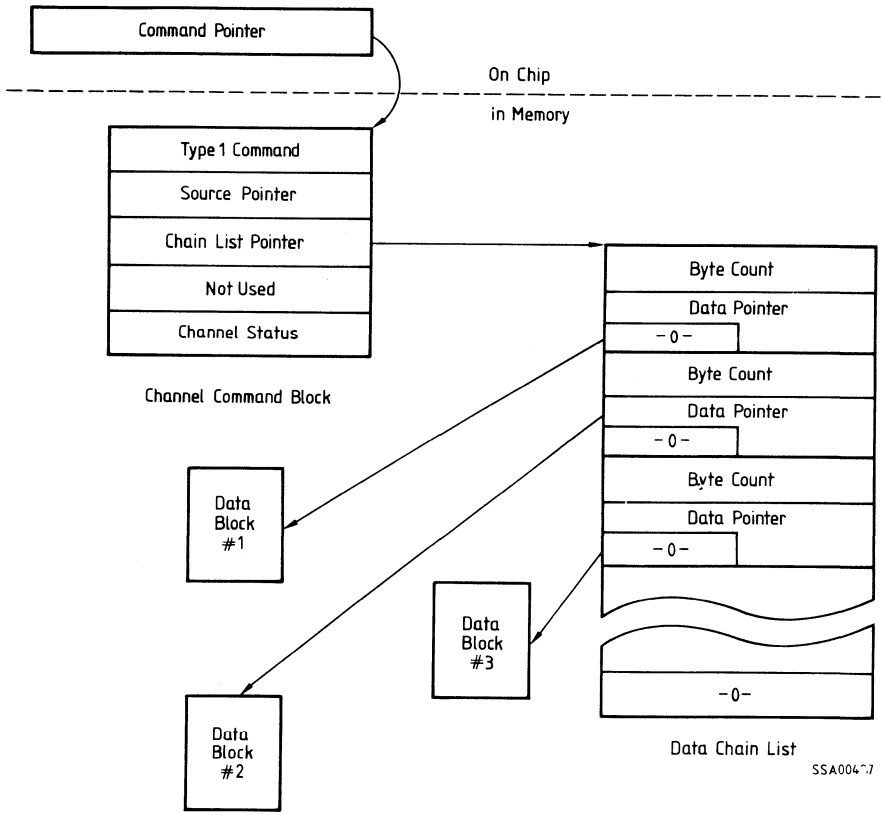
Data Chaining

a) Linked List Chaining



Data Chaining

b) List Chaining



"On-The-Fly" Operations

A normal DMA controller blindly transfers data from source to destination without looking at the data. In case of the SAB 82C258A on-the-fly operations are executed during the DMA transfer and allow inspection and/or operation on the transferred data. There are three possible on-the-fly operations:
- mask/compare
- translate and
- verify

During a mask/compare operation each byte/word transferred is compared to a given pattern. One or more bits can be masked and thus do not contribute to the result of the compare operation. The result can be used by subsequent conditional stop or jump operations.

For translate operation the byte (no word possible) that is fetched from source is added to a translate pointer to build the effective source pointer. The byte pointed to by this pointer is then fetched and sent out to the destination. Of course, a mask/compare operation is possible on the byte sent out.

The verify operation is a type of block compare operation to compare each byte/word of data read from a peripheral with the one in a data block in the memory. There are three options:

1. Verify with no termination on mismatch
   (2-cycle transfer only)
2. Verify with termination on mismatch
   (2-cycle transfer only)
3. Verify and save (single cycle transfer only).
   Here an actual transfer with compare takes place.
   The transfer is not stopped on mismatch.

Note: *Verify and save operation and mask/compare operation can be used during 32-bit fly-by transfer, but can check a maximum of 16 bits, not a complete double word.*

Multiplexer Channel

When programmed to multiplexer mode, channel 3 (supported by a multiplexer logic) can be used to service up to 32 subchannel request lines (see figures below).Thus it is ideally suited to service a large number of comparatively slow equipment like CRT terminals, line printers, serial links, etc. Since multiple subchannels are processed with the resource of one DMA channel, the overhead of subchannel switching, of course, decreases the total effective throughput on the multiplexer channel.

To allow efficient control even of the subchannels, a separate command pointer for each subchannel is provided within the multiplexer table. Thus an individual subchannel program (command chain) can be used for each subchannel.

Different transfer modes are provided for subchannels:

Byte/word multiplex

One byte or word is transferred per request. Updating the pointers is done within the actual command block.

Single transfer

Similar to byte/word multiplex, but with execution of command chaining after each transfer.

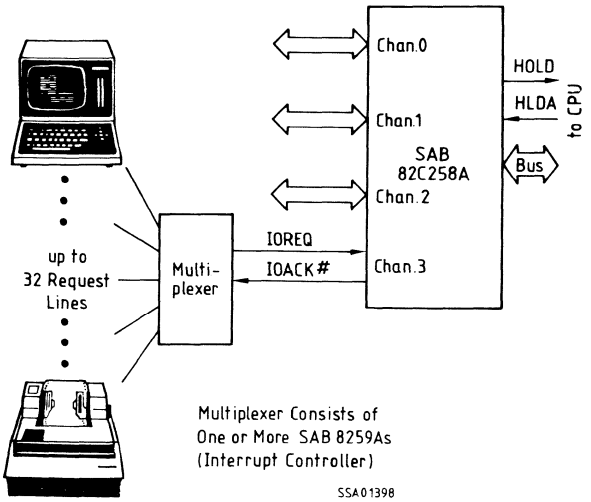
Block multiplex

I/O request initiates execution of a complete command block, i.e. the complete data block specified is transferred. This allows maximum transfer rates (2-cycle transfers) also for subchannels.

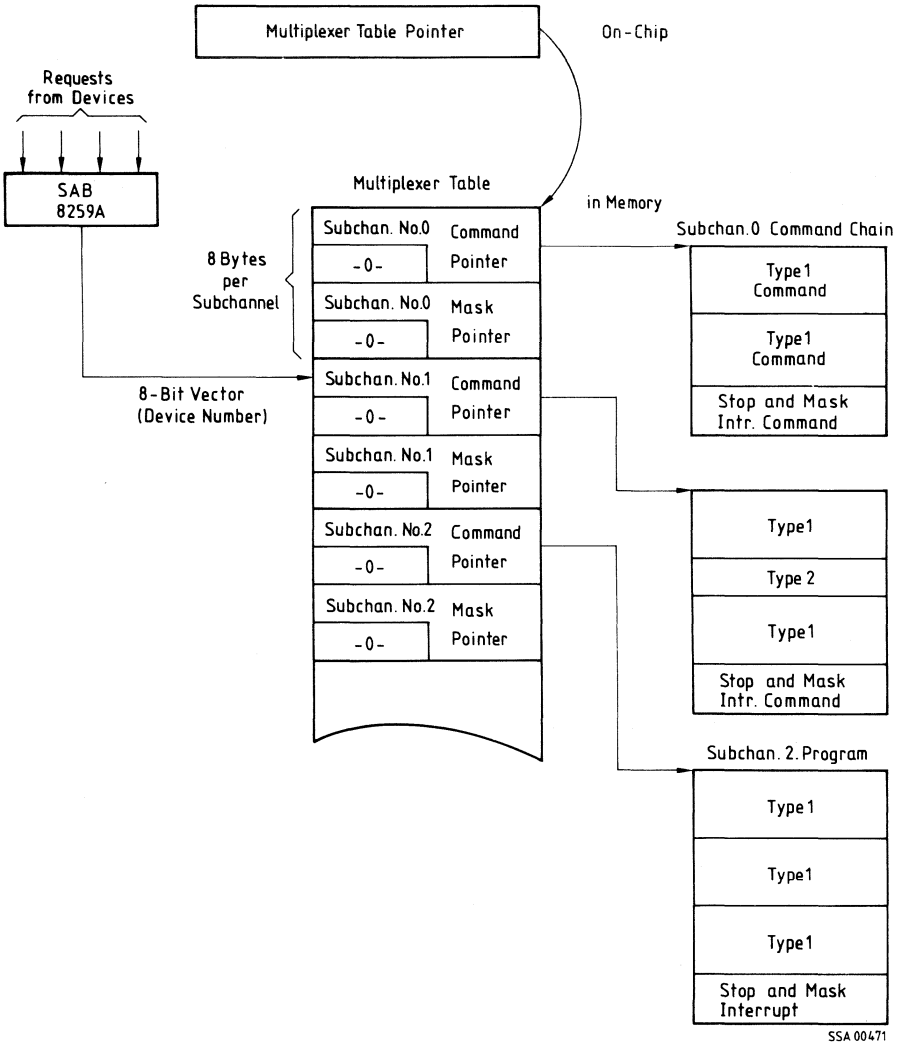
A type 2 command in a subchannel program can issue an interrupt, whereby the multiplexer channel interrupt vector register (MIVR) provides the corresponding subchannel number for the CPU.

A subchannel program is terminated by a stop and mask command which automatically masks the corresponding request line within the SAB 8259A thus blocking this subchannel until it is enabled again by the CPU.

Multiplexer Channel



Structure of the Multiplexer Table



The mask pointer is the address of the appropriate SAB 8259A mask register.

32-Bit Fly-by Transfers

The 32-bit transfer enable bit TR32 (bit 6 of the channel command register extension CCRX) allows the address pointers and byte counters to be modified not only by 1 or 2, but also by 4 in order to count 32-bit double words. Therefore, the SAB 82C258A can control 32-bit transfers in single cycle mode. In this mode, data flows past the DMA controller rather than through it. All features that use the data assembly registers (two-cycle mode, compare, verify, etc.), should be avoided, because the 16-bit data port can access only one half of a 32-bit data bus.
Addresses and byte counts must be aligned to double-word boundaries (i.e. multiples of 4) in order to ensure proper operation. Also the effective transfer width (logical and physical bus width) must be programmed to 16 bits. As the external control signals do not allow to distinguish 32-bit fly-by transfers from 16-bit transfers, the transfer mode of a channel must be predefined.

Note: *If the SAB 82C258A is to operate in a system with a true 32-bit address bus, the upper address byte (A31 to A24) must be provided by an external page register, as the SAB 82C258A's address bus is still 24 bits wide.*

Operating the SAB 82C258A

Reset

When activating the reset input, the SAB 82C258A is forced into its initial state. All channels and bus activities are stopped, tristate lines are tristated and the others enter the inactive state. While the reset input is active, pin 57 must be held high and lines A23/AREADY and HLDA must be forced to the appropriate levels to select the desired bus interface mode (see figures on page 4, 49 and 62).
After deactivating reset the inactive state is maintained, in addition the state of the SAB 82C258A registers is as follows:

- general mode register, general burst register, general delay register, general status register and the four channel status registers are set to zero,
- the vector-not-valid bit of the multiplexer interrupt vector register is set to 1,
- all other registers and bits are undefined.

Note: *The general mode register (GMR) should be loaded first to select the mode of operation before any other activity is started on the SAB 82C258A.*

DMA Interface

The DMA interface consists of three lines:

- DREQ – DMA request
- DACK# – DMA acknowledge and
- EOD# – End of DMA

The first two lines work as request and acknowledge lines to control synchronized DMA transfers as known from conventional DMA controllers.

A special feature of the SAB 82C258A are the bidirectional EOD# lines . Firstly they can be used as inputs to receive an asynchronous external terminate signal to terminate a running DMA.
Secondly, as an output, they can be used to send out a pulse which interrupts the CPU and/or signals to the peripheral a specific status (e.g. transfer aborted, or end of a block, or send/receive next block ...).

The EOD# output signal can be generated synchronously to a transfer (during the last transfer) or asynchronously to the transfers by a specific command.

In addition the EOD# output of channel 2 can be used as a collective interrupt output for all DMA channels while the other three retain their normal function.

Slave Interface

The slave interface is used to access the SAB 82C258A internal registers. Although nearly all of the communication between CPU and SAB 82C258A is done via memory-based data blocks, some direct accesses to SAB 82C258A registers are necessary.

For example during the initialization phase the general mode register must be written, or to start a channel the command pointer register and the general command register must be loaded. Also during the debugging phase it is of great benefit to have access to all of the SAB 82C258A internal registers.

The slave interface is enabled by the CS# input and consists of the following lines:

- S0#, S1# – status lines (inputs)
- RD#, WR# – control lines (inputs)
- A0-A7 – register address (inputs)
- D0-D15 – data lines (inputs/outputs) or
- AD0-AD15 – data lines (inputs/outputs) for synchronous access in 186 mode

Note that all of these lines are outputs, if the SAB 82C258A is an active bus master.

In 186 mode and 286 mode two types of accesses are possible:

- Synchronous access by means of the status lines. Processor and SAB 82C258A are directly coupled and must use the same clock.
- Asynchronous access by using the control lines RD# and WR# (processor and SAB 82C258A may have different clocks).

In all modes except the synchronous access in 186 mode the register address must be supplied on address pins A0 to A7. Using synchronous access in 186 mode the address information is expected at address/data lines AD0 to AD7.
In remote mode only the asynchronous access is possible because the SAB 82C258A first has to release its local bus to enable the register access. On receiving an access request (activation of CS# input) the SAB 82C258A releases its local bus as soon as possible and signals this by activating the BREL line. Now the CPU can accomplish its access.

Bus Arbitration

To arbitrate access to the bus between the SAB 82C258A and the processor, the signals HOLD and HLDA serve for communication. Normally the SAB 82C258A competes for the bus via HOLD, the processor grants access to the bus via HLDA. The HLDA signal can also be deactivated in order to force the SAB 82C258A off the bus for a certain reason (kick off). After reactivation of HLDA, the SAB 82C258A will again get control of the bus. In 8086 mode this communication is done by pulses via a single RQ#/GT# line which uses the HOLD pin. In this case normally the HLDA input has no function. Nevertheless, even in 8086 mode the HLDA input can be used for kick-off. This provides some kind of additional bus arbitration.

Register Set

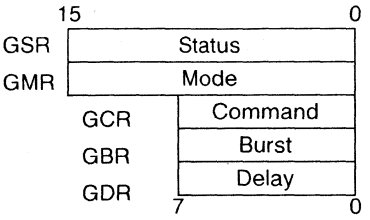
The following figure shows the user visible registers of the SAB 82C258A. A set of 5 registers, called the general registers, is used for all of the 4 channels. The mode register is being written to first after reset and it describes the SAB 82C258A environment – bus widths, priorities, etc.

The general command register (GCR) is used to start and stop the DMA transfer on different channels. The general status register (GSR) shows the status of all of the 4 channels; if the channel is running, if interrupt is pending, etc. General burst register (GBR) and general delay register (GDR) are used to specify the bus load which is permissible for the SAB 82C258A.

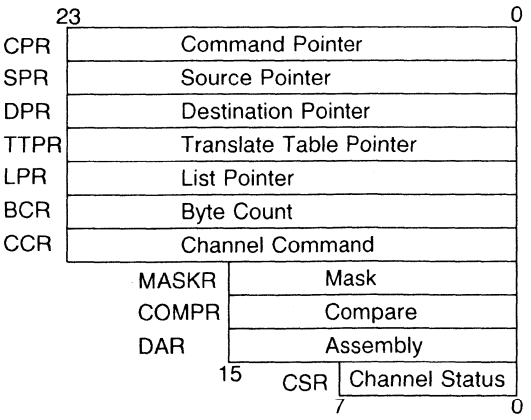
There is a set of channel registers for each of the 4 channels. Most channel registers serve as cache registers and need to be accessed only for debugging. During normal operation they are loaded automatically by the SAB 82C258A (see next paragraph). The layout of register addresses shown in the figure on the next page. All register addresses are even. Locations not designated in that figure are reserved and should not be used.

SAB 82C258A Register Set

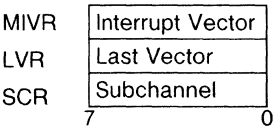
General Register



Channel Register (4 sets; 1 per channel)



Multiplexer Channel Register



SSA00472

Register Address Arrangement

Address Bits 0-5	Address Bits 7, 6			
	00	01	10	11
0	GCR			
2	SCR			
4	GSR			
6				
8	GMR			
A	GBR			
C	GDR			
E				
10	CSR 0	CSR 1	CSR 2	CSR 3
12	DAR 0	DAR 1	DAR 2	DAR 3
14	MASKR 0	MASKR 1	MASKR 2	MASKR 3
16	COMPR 0	COMPR 1	COMPR 2	COMPR 3
18				MIVR
1A				LVR
1C				
1E				
20	CPR L0	CPR L1	CPR L2	CPR L3
22	CPR H0	CPR H1	CPR H2	CPR H3
24	SPR L0	SPR L1	SPR L2	SPR L3
26	SPR H0	SPR H1	SPR H2	SPR H3
28	DPR L0	DPR L1	DPR L2	DPR L3
2A	DPR H0	DPR H1	DPR H2	DPR H3
2C	TTPR L0	TTPR L1	TTPR L2	TTPR L3
2E	TTPR H0	TTPR H1	TTPR H2	TTPR H3
30	LPR L0	LPR L1	LPR L2	LPR L3/MTPR L
32	LPR H0	LPR H1	LPR H2	LPR H3/MTPR H
34				
36				
38	BCR L0	BCR L1	BCR L2	BCR L3
3A	BCR H0	BCR H1	BCR H2	BCR H3
3C	CCR L0	CCR L1	CCR L2	CCR L3
3E	CCR H0	CCR H1	CCR H2	CCR H3

GCR = General Command Register
SCR = Subchannel Register
GSR = General Status Register
GMR = General Mode Register
GBR = General Burst Register
GDR = General Delay Register
CSR = Channel Status Register
DAR = Data Assembly Register
MASKR = Mask Register
COMPR = Compare Register

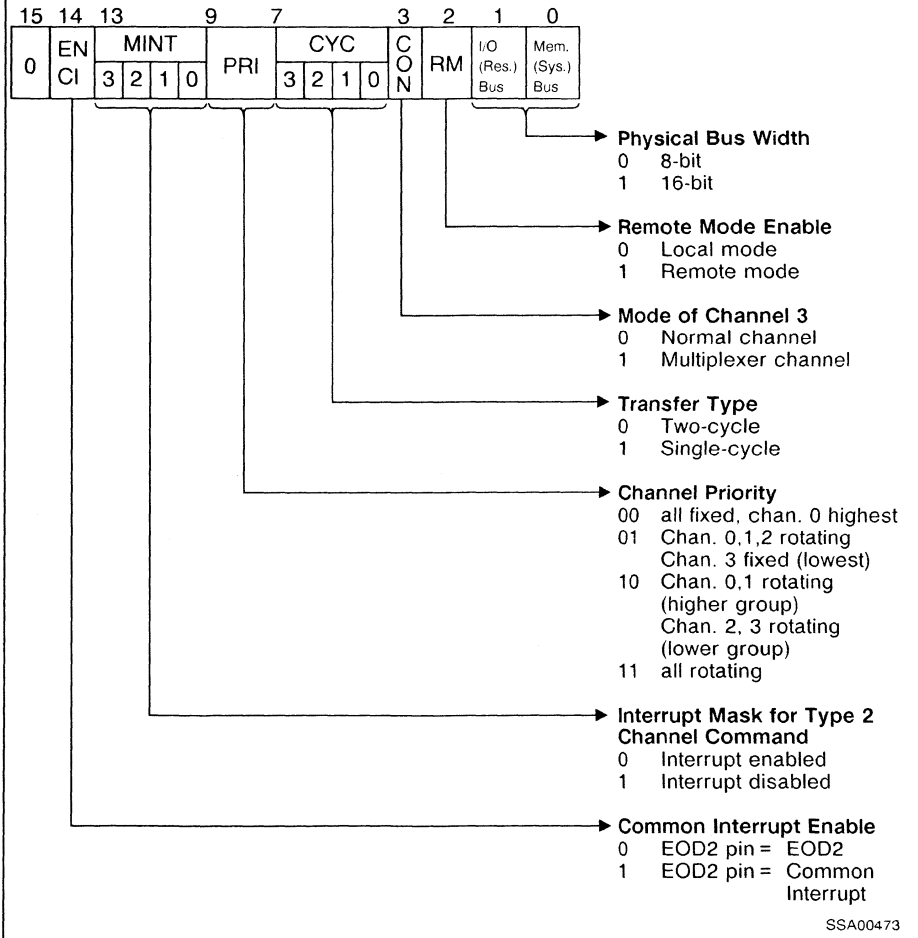
MIVR = Multiplexer Interrupt Vector Register
LVR = Last Vector Register
CPR = Command Pointer Register
SPR = Source Pointer Register
DPR = Destination Pointer Register
TTPR = Translate Table Pointer Register
LPR = List Pointer Register
MTPR = Multiplexer Table Pointer Register
BCR = Byte Count Register
CCR = Channel Command Register

Register Description

General Mode Register

In the general mode register GMR (figure below) the system wide parameters are specified. This register should be programmed first after reset, with an 8-bit bus program low byte first.

General Mode Register (GMR)



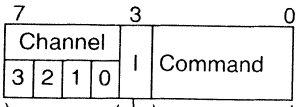
SSA00473

*) On multiplexer channel CYC3 identifies the associated control space for the multiplexer matrix (CYC3 = 0/1:SAB 8259A in I/O/memory space).

General Command Register

Individual channels are started and stopped by a command written to the general command register GCR (figure below). The GCR is directly loaded by the CPU.

General Command Register (GCR)



Channel Command

000	NOP	
001	CONTINUE	Channel(s) after it has been stopped by the STOP command
010	START	Channel(s) = Command block at system memory space
011	START	Channel(s) = Command block at resident I/O space
100	STOP	Channel(s)
101	START	Subchannel (number in SCR)
110	STOP	Subchannel (number in SCR)
111	HALT	Single-step channel(s): Start execution and stop before next command block will be loaded

Interrupt Command

0	NOP
1	Clear interrupt(s) of channel(s)

Channel Select

0	Channel not effected
1	Command refers to this channel

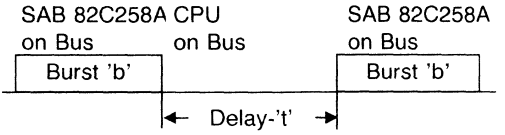
SSA00430

General Burst and Delay Register

It is possible to restrict the bus load generated by the SAB 82C258A on the CPU bus by programming the burst and the delay register. The bus load is defined by the formula given in figure a) below. The factor b (burst) is programmed in the general burst register GBR, t (delay time) in the general delay register GDR (see figures b and c). Since the SAB 82C258A can also execute locked bus cycles, the maximum burst length consists of b + 3 (8-bit bus) or b + 2 (16-bit bus) bus cycles. GBR and GDR must be directly loaded by the CPU. Loading GBR with 0 leads to no bus load limitations for the SAB 82C258A (default after reset).

General Burst and Delay Register

a) Bus Loading

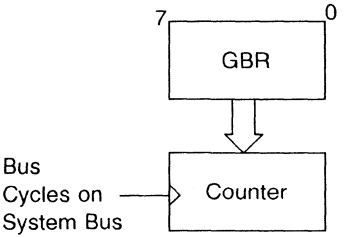


$$\text{Bus Load due to the SAB 82C258A} = \frac{b}{b+t}$$

b) General Burst Register (GBR) – to Program 'b'

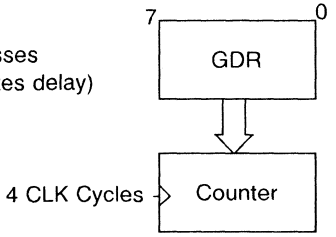
Determines max. number of contiguous bus cycles from the SAB 82C258A

If GBR = 0, No Limit



c) General Delay Register (GDR) – to Program 't'

Determines min. number of clock cycles between burst accesses (default after reset = 0,i.e. 4 T-states delay)



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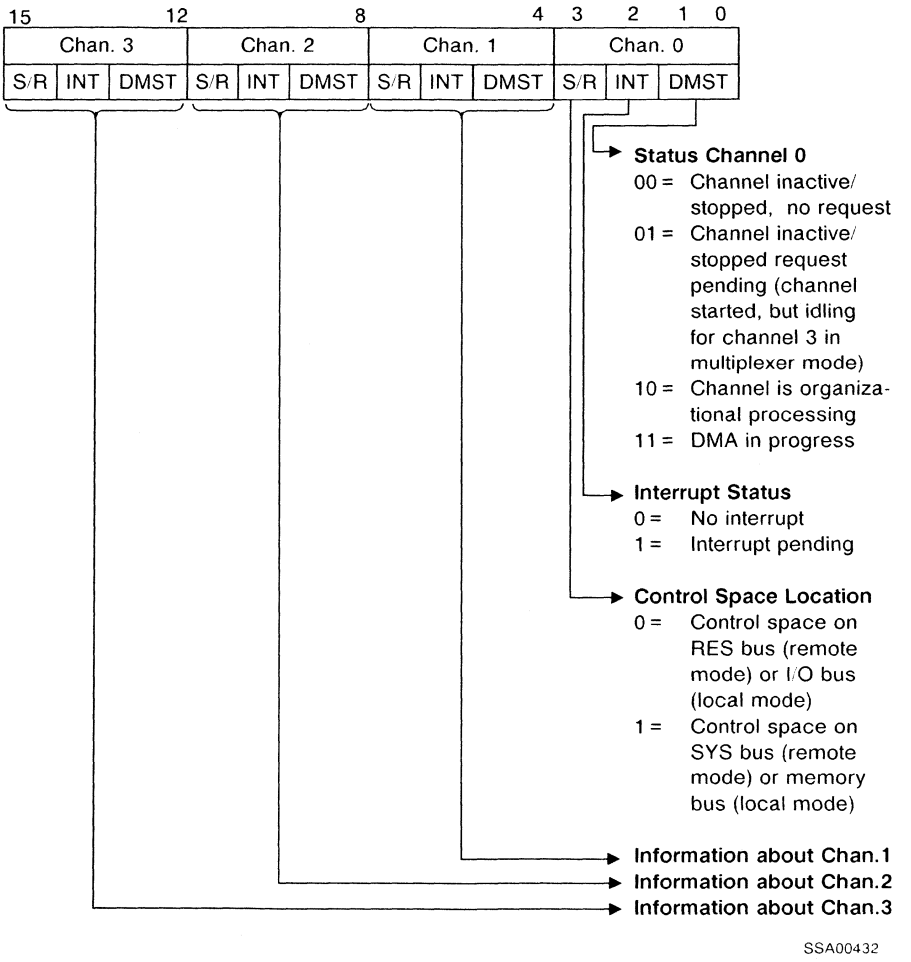
General Status Register

The general status register GSR (figure below) shows the current status of all the channels.

General Status Register (GSR)



Channel Commands

The channel commands are contained in the channel command block. Up to 22 bits are used to specify the command. There are two types of channel commands:

- Type 1: for data movement
- Type 2: for command chaining control

The command block for a type 1 command is in general 26 bytes long (see figure „Memory based Communication").

For certain type 1 transfers which, for example, do not use on-the-fly match, translate or verify feature, the command is only 16 bits long and only a short command block is necessary (see figure „Memory based Communication").

The type 1 command fields (see figures below) contain information on:

a. Bus width of source and destination
b. If source and/or destination address should be incremented or decremented or kept constant during the transfer
c. If source/destination is in memory or I/O space (local mode) or in system or resident space (remote mode)
d. If data chaining (list or linked-list) is to be performed
e. If the data transfer is synchronized (source or destination)
f. If an on-the-fly match operation and/or translate operation has to be performed
g. If a verify operation has to be performed
h. If 32-bit fly-by transfers are to be executed.

Type 2 command blocks are 6 bytes long (see figure „Type 2 Command Block") of which the first 2 bytes form the command and the rest is either a relative displacement or an absolute address for the JUMP operation. There are two basic type 2 commands (see figure „Type 2 Command Block"):

a. JUMP – conditional and non-conditional
b. STOP – conditional and non-conditional

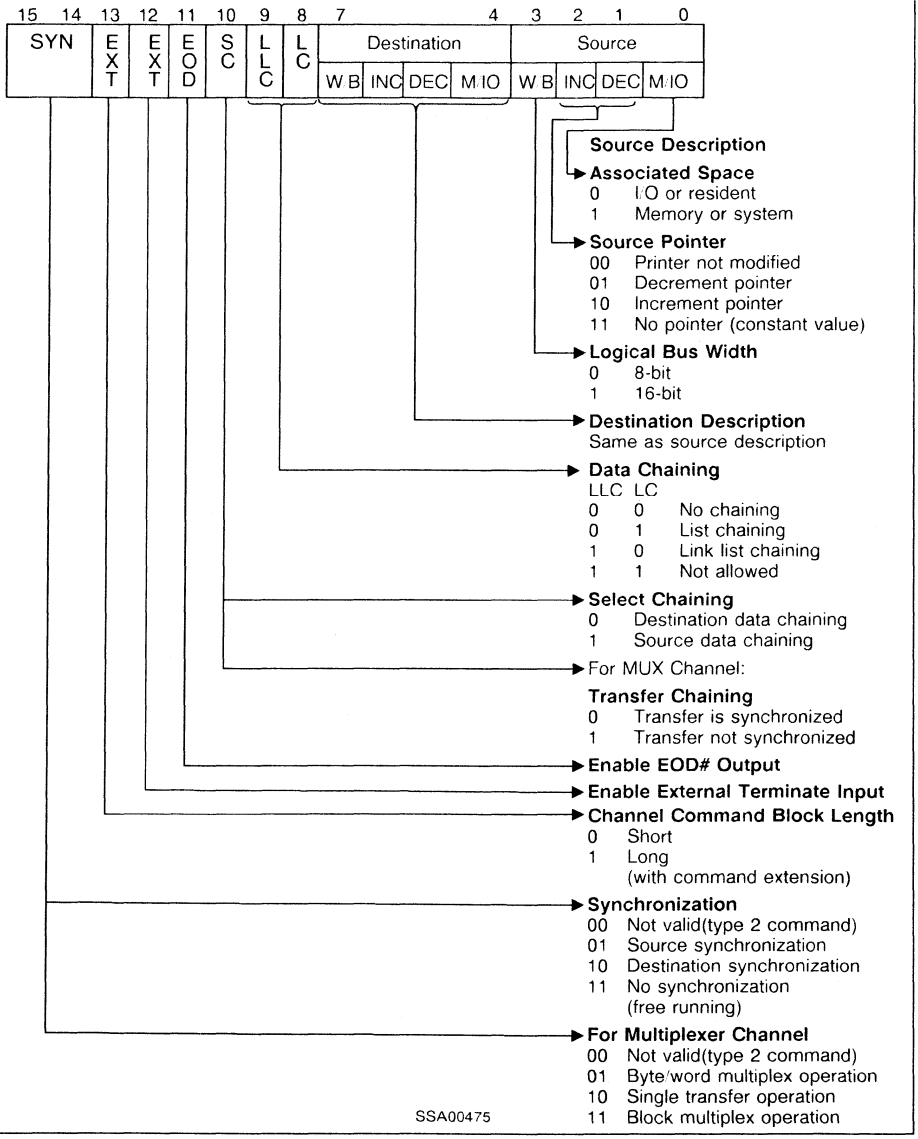
The conditional case tests for either of the 4 condition bits which are altered at the termination of any DMA operation:

- Termination due to byte count end
- Termination due to mask-compare
- Termination due to external terminate
- Verify operation resulting in mismatch.

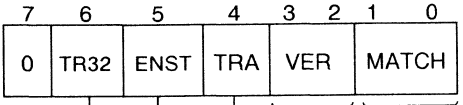
It is thus possible to JUMP or STOP further execution of commands based on any of these conditions and optionally generate an EOD# or interrupt signal.

The combination of type 1 and 2 commands gives the SAB 82C258A a high degree of "programmability". It can thus execute quite complex algorithms with a fairly low demand for CPU service.

Type 1 (DMA) Channel Command



Type 1 Channel Command Extension



Match-Compare
00 Disabled
01 Enable mismatch (byte/word)
10 Enable byte match
11 Enable word match

Verify
00 Verify disabled
01 Verify
10 Verify and halt (on mismatch)
11 Verify and save

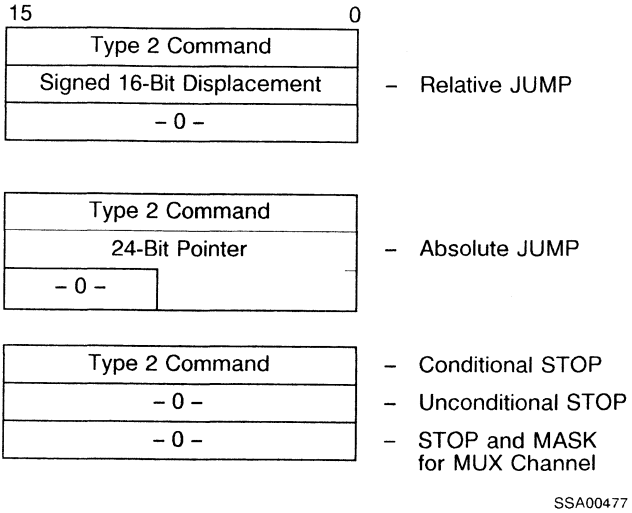
Translate Enable
0 Translate disabled
1 Translate enabled

Enable Status Block
0 Update in channel command block disabled
1 Update enabled

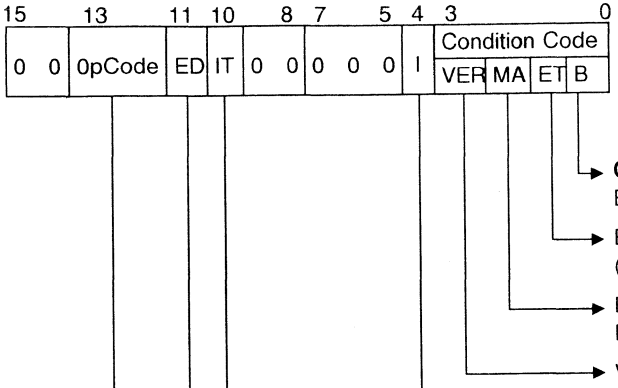
32-Bit Transfer Enable
0 Byte/word transfers only
1 32-bit fly-by transfer enabled

SSA00476

Type 2 Command Blocks (for command chaining control)



Type 2 Command Format



Condition Code
Byte count = 0

External termination
(EOD# received)

Byte/word
Match/mismatch

Verify mismatch

Invert
Invert channel status bits before comparing with condition code

Generate Interrupt

Generate EOD# Pulse

OpCode
00 Unconditional STOP
STOP and MASK for MUX channel
01 Conditional STOP
10 Conditional* JUMP relative
11 Conditional* JUMP absolute

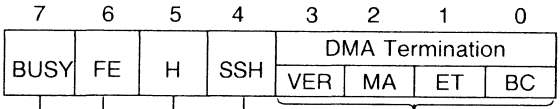
SSA00478

*) Unconditional JUMP when all condition code bits are set 1.

Channel Status Register

For each channel there is a channel status register (see figure below). This register shows the current state of the appropriate channel.

Channel Status Register



Flags Set on DMA Termination
BC – Byte count end
ET – External termination
MA – Match/mismatch
VER – Verify operation ending in mismatch

Single-Step and Halt Mode
Channel operating in SSH mode

Halted
Channel in halted state

Fatal Error
Fatal error has occurred

BUSY *)
Last subchannel command from CPU is processed

SSA00479

*) Valid only for channel 3 in multiplexer mode. In all other cases 0 is returned.

Multiplexer Channel Register

These registers are valid only for channel 3 if programmed as multiplexer channel.

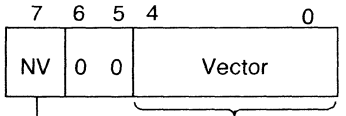
Multiplexer Table Pointer Register (MTPR)

This 24-bit register is used to reference the multiplexer table in memory (see figure „Structure of the Multiplexer Table"). It must be loaded by the CPU. Physically the list pointer register is used, since data chaining is not allowed for multiplexer channel.

Multiplexer Interrupt Vector Register (MIVR)

This 8-bit register is read by the CPU to determine which subchannels are stopped. The vectors of the stopped subchannels are output on subsequent read operations in the order of their priority (0 has highest priority).

Multiplexer Interrupt Vector Register (MIVR)



Subchannel Vector
Vector of the highest priority subchannel stopped and not yet read

Non-Valid
0 Vector is valid
1 Vector is not valid
(no channel stopped or all vectors read)

SSA00480

Last Vector Register (LVR)

The 8-bit register holds the last vector read by the SAB 82C258A (from SAB 8259A). In case of a stop caused by a fatal error on channel 3, LVR determines the failing subchannel.

Subchannel Register (SCR)

The 8-bit register must be loaded by the CPU with the desired subchannel number before a subchannel command is written into GCR.

Timings

The bus timings in 286 and remote mode are identical to that for the SAB 80286, in 186 and 8086 mode the timings are identical to that for the SAB 80186. The bus timings are also compatible with the timings of the available CMOS processors. For exact timings see timing diagrams of AC Characteristics.

Asynchronous control inputs are specified with setup and hold times which are only important to determine whether the SAB 82C258A responds to the signal in the current cycle or the next cycle.

The following pages hold two sections of AC characteristics and waveforms. The first section refers to 286 mode and remote mode, the second one to 186 mode and 8086 mode.

Absolute Maximum Ratings

Ambient Temperature under bias ..... 0 to 70°C
Storage temperature ..... – 65 to + 150°C
Voltage on any pin with respect to ground ..... – 0.5 to + 7 V
Power dissipation ..... 3 W

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_C = 0 to 85°C; V_{CC} = + 5 V ± 5%

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage (except CLK)	V_{IL}	– 0.5	+ 0.8	V	–
Input high voltage (except CLK)	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 3.0 mA
Output high voltage	V_{OH}	3.0	–	V	I_{OH} = – 400 µA
Power supply current	I_{CC}	–	250	mA	T_C = 25°C all outputs open
Input leakage current	I_{LI}				
S0#, S1#, S2#, BHE#, RD#, WR#, M/IO#		–	– 200	µA	0 V ≤ V_{IN} ≤ V_{CC}
HOLD (RQ#/GT# mode), EOD# A23 (AREADY), A21 [2]		–	–1.5	mA	0 V ≤ V_{IN} ≤ V_{CC}
other pins		–	± 10	µA	0 V ≤ V_{IN} ≤ V_{CC}
Output leakage current	I_{LO}	–	± 10	µA	0.45 V ≤ V_{OUT} ≤ V_{CC}
Clock input low voltage	V_{CL}	– 0.5	+ 0.6	V	–
Clock input high voltage	V_{CH}	3.8	V_{CC} + 1.0	V	–

[1]) This specification is valid only during RESET.

Capacitance

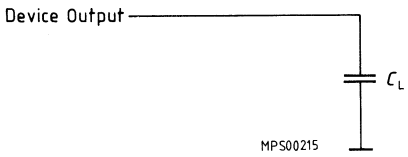
$T_C = 25°C$; V_{CC} = GND = 0 V, $f_C = 1$ MHz

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Capacitance of inputs (except CLK)	C_{IN}	–	10	pF	2)
Capacitance of I/O or outputs	C_{IO}	–	20	pF	2)
Capacitance of CLK input	C_{CLK}	–	12	pF	2)

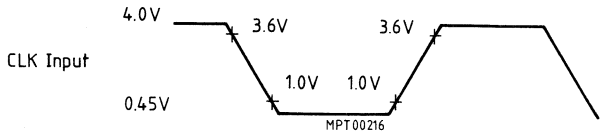
2) Not 100% tested, guaranteed by design characterization.

AC Testing Waveforms

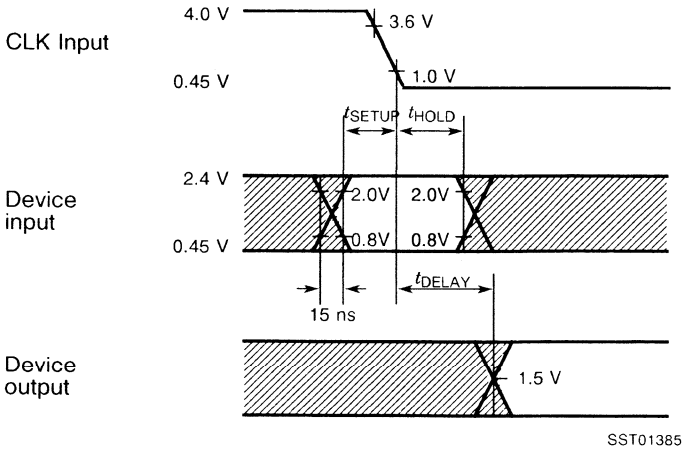
Test Loading on Outputs



Drive and Measurement Points – CLK Input



Setup, Hold and Delay Time Measurement – General



AC Characteristics SAB 82C258A-1 (286 mode)

T_C = 0 to 85 °C; V_{CC} = +5 V ±5%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
CLK cycle period	t_1	50	–	ns	–
CLK low time	t_2	12	–	ns	at 1.0 V
CLK high time	t_3	16	–	ns	at 3.6 V
Address/control output delay	t_4	–	35	ns	C_L = 100 pF
Status output delay	t_5	–	22	ns	C_L = 100 pF
Sync data setup time	t_6	8	–	ns	–
Sync data hold time	t_7	8	–	ns	–
Sync READY# setup time	t_8	26	–	ns	–
Sync READY# hold time	t_9	15	–	ns	–
Sync control input setup time	t_{10}	20	–	ns	–
Sync control address input hold time	t_{11}	20	–	ns	–
Sync address setup time	t_{12}	2	–	ns	–
Data/control output delay	t_{13}	–	30	ns	C_L = 100 pF
Data/control float delay	t_{14}	–	40	ns	–
BHE# setup time	t_{15}	40	–	ns	–
Write command width	t_{16}	4CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	2CLK + t_6 + t_{44}	–	ns	–
Async address setup time	t_{18}	t_{43}	–	ns	–
Async data access time	t_{19}	–	5CLK + t_{43} + t_{13}	ns	–
Mode select setup time	t_{28}	2CLK + 20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Command recovery time	t_{33}	4CLK + t_{43} + t_{44}	–	ns	–

AC Characteristics SAB 82C258A-1 (286 mode) cont'd

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
CLK rise time	t_{34}	–	8	ns	1.0 to 3.6 V
CLK fall time	t_{35}	–	8	ns	3.6 to 1.0 V
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
CS# active response time	t_{37}	2CLK	22CLK + t_{43} + t_{44}	ns	1)
CS# active after BREL inactive	t_{39}	0	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async input setup time	t_{43}	20	–	ns	2)
Async input hold time	t_{44}	20	–	ns	2)
Async HLDA high time	t_{47}	2CLK + t_{43} + t_{44}	–	ns	3)
HOLD output low time	t_{49}	4CLK − t_{13}	–	ns	–
HLDA low to HOLD low delay	t_{50}	6CLK	22CLK + t_{43} + t_{13}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
CS# hold time	t_{56}	40	–	ns	–
DACK# output delay	t_{59}	–	3	ns	–

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 22 CLK
- normal pointer transfer (3 bus cycles): 16 CLK
- splitted pointer transfer (4 bus cycles): 20 CLK

If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

AC Characteristics SAB 82C258A-12 (286 mode)

T_C = 0 to 85°C; V_{CC} = +5 V ±5%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
CLK cycle period	t_1	40	–	ns	–
CLK low time	t_2	11	–	ns	at 1.0 V
CLK high time	t_3	13	–	ns	at 3.6 V
Address/control output delay	t_4	–	32	ns	C_L = 100 pF
Status output delay	t_5	–	18	ns	C_L = 100 pF
Sync data setup time	t_6	5	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync READY# setup time	t_8	22	–	ns	–
Sync READY# hold time	t_9	10	–	ns	–
Sync control input setup time	t_{10}	16	–	ns	–
Sync control/address input hold time	t_{11}	16	–	ns	–
Sync address setup time	t_{12}	2	–	ns	–
Data/control output delay	t_{13}	–	25	ns	C_L = 100 pF
Data/control float delay	t_{14}	–	32	ns	–
BHE# setup time	t_{15}	36	–	ns	–
Write command width	t_{16}	4CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	2CLK + t_6 + t_{44}	–	ns	–
Async address setup time	t_{18}	t_{43}	–	ns	–
Async data access time	t_{19}	–	5CLK + t_{43} + t_{13}	ns	–
Mode select setup time	t_{28}	2CLK + 18	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–

AC Characteristics SAB 82C258A-12 (286 mode) cont'd

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Command recovery time	t_{33}	4CLK + t_{43} + t_{44}	–	ns	–
CLK rise time	t_{34}	–	8	ns	1.0 to 3.6 V
CLK fall time	t_{35}	–	8	ns	3.6 to 1.0 V
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
CS# active response time	t_{37}	2CLK	22CLK + t_{43} + t_4	ns	1)
CS# active after BREL inactive	t_{39}	0	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async input setup time	t_{43}	18	–	ns	2)
Async input hold time	t_{44}	18	–	ns	2)
Async HLDA high time	t_{47}	2CLK + t_{43} + t_{44}	–	ns	3)
HOLD output low time	t_{49}	4CLK − t_{13}	–	ns	–
HLDA low to HOLD low delay	t_{50}	6CLK	22CLK + t_{43} + t_{13}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	18	–	ns	–
Async access hold time	t_{55}	18	–	ns	–
CS# hold time	t_{56}	30	–	ns	–
DACK# output delay	t_{59}	–	30	ns	–

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 22 CLK
- normal pointer transfer (3 bus cycles): 16 CLK
- splitted pointer transfer (4 bus cycles): 20 CLK

If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

AC Characteristics SAB 82C258A-16 (286 mode)

T_C = 0 to 85°C; V_{CC} = +5 V ±5%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
CLK cycle period	t_1	31	–	ns	–
CLK low time	t_2	8	–	ns	at 1.0 V
CLK high time	t_3	11	–	ns	at 3.6 V
Address/control output delay	t_4	–	28	ns	C_L = 100 pF
Status output delay	t_5	–	18	ns	C_L = 100 pF
Sync data setup time	t_6	5	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync READY# setup time	t_8	15	–	ns	–
Sync READY# hold time	t_9	5	–	ns	–
Sync control input setup time	t_{10}	11	–	ns	–
Sync control/address input hold time	t_{11}	12	–	ns	–
Sync address setup time	t_{12}	2	–	ns	–
Data/control output delay	t_{13}	–	20	ns	C_L = 100 pF
Data/control float delay	t_{14}	–	28	ns	–
BHE# setup time	t_{15}	28	–	ns	–
Write command width	t_{16}	4CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	2CLK + t_6 + t_{44}	–	ns	–
Async address setup time	t_{18}	t_{43}	–	ns	–
Async data access time	t_{19}	–	5CLK + t_{43} + t_{13}	ns	–
Mode select setup time	t_{28}	2CLK + 14	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–

AC Characteristics SAB 82C258A-16 (286 mode) cont'd

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Command recovery time	t_{33}	4CLK + t_{43} + t_{44}	–	ns	–
CLK rise time	t_{34}	–	5	ns	1.0 to 3.6 V
CLK fall time	t_{35}	–	5	ns	3.6 to 1.0 V
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
CS# active response time	t_{37}	2CLK	22CLK + t_{43} + t_4	ns	1)
CS# active after BREL inactive	t_{39}	0	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async input setup time	t_{43}	14	–	ns	2)
Async input hold time	t_{44}	14	–	ns	2)
Async HLDA high time	t_{47}	2CLK + t_{43} + t_{44}	–	ns	3)
HOLD output low time	t_{49}	4CLK – t_{13}	–	ns	–
HLDA low to HOLD low delay	t_{50}	6CLK	22CLK + t_{43} + t_{13}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	14	–	ns	–
Async access hold time	t_{55}	14	–	ns	–
CS# hold time	t_{56}	22	–	ns	–
DACK# output delay	t_{59}	–	25	ns	–

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 22 CLK
- normal pointer transfer (3 bus cycles): 16 CLK
- splitted pointer transfer (4 bus cycles): 20 CLK

If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

AC Characteristics SAB 82C258A-20 (286 mode)

T_C = 0 to 85°C; V_{CC} = +5 V ±5%

Any output timing is measured at 1.5 V

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
CLK cycle period	t_1	25	–	ns	–
CLK low time	t_2	7	–	ns	at 1.0 V
CLK high time	t_3	9	–	ns	at 3.6 V
Address/control output delay	t_4	–	22	ns	C_L = 100 pF
Status output delay	t_5	–	14	ns	C_L = 100 pF
Sync data setup time	t_6	5	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync READY# setup time	t_8	11	–	ns	–
Sync READY# hold time	t_9	3	–	ns	–
Sync control input setup time	t_{10}	8	–	ns	–
Sync control/address input hold time	t_{11}	8	–	ns	–
Sync address setup time	t_{12}	1	–	ns	–
Data/control output delay	t_{13}	–	15	ns	C_L = 100 pF
Data/control float delay	t_{14}	–	25	ns	–
BHE# setup time	t_{15}	22	–	ns	–
Write command width	t_{16}	4CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	2CLK + t_6 + t_{44}	–	ns	–
Async address setup time	t_{18}	t_{43}	–	ns	–
Async data access time	t_{19}	–	5CLK + t_{43} + t_{13}	ns	–
Mode select setup time	t_{28}	2CLK + 11	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Command recovery time	t_{33}	4CLK + t_{43} + t_{44}	–	ns	–

AC Characteristics SAB 82C258A-20 (286 mode) cont'd

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
CLK rise time	t_{34}	–	4	ns	1.0 to 3.6 V
CLK fall time	t_{35}	–	4	ns	3.6 to 1.0 V
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
CS# active response time	t_{37}	2CLK	22CLK + t_{43} + t_4	ns	1)
CS# active after BREL inactive	t_{39}	0	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async input setup time	t_{43}	11	–	ns	2)
Async input hold time	t_{44}	11	–	ns	2)
Async HLDA high time	t_{47}	2CLK + t_{43} + t_{44}	–	ns	3)
HOLD output low time	t_{49}	4CLK – t_{13}	–	ns	–
HLDA low to HOLD low delay	t_{50}	6CLK	22CLK + t_{43} + t_{13}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	11	–	ns	–
Async access hold time	t_{55}	11	–	ns	–
CS# hold time	t_{56}	17	–	ns	–
DACK# output delay	t_{59}	–	18	ns	–

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 22 CLK
- normal pointer transfer (3 bus cycles): 16 CLK
- splitted pointer transfer (4 bus cycles): 20 CLK

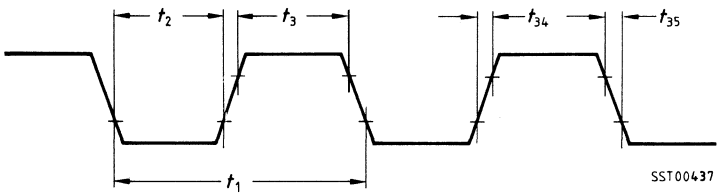
If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

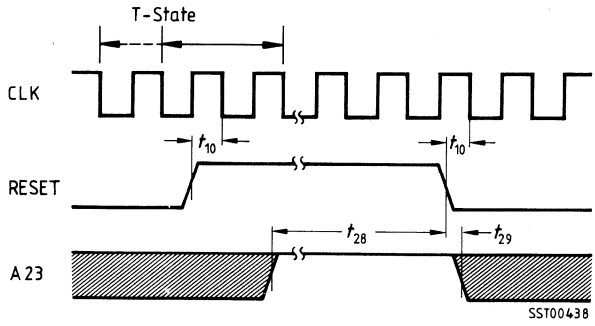
3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

Waveforms

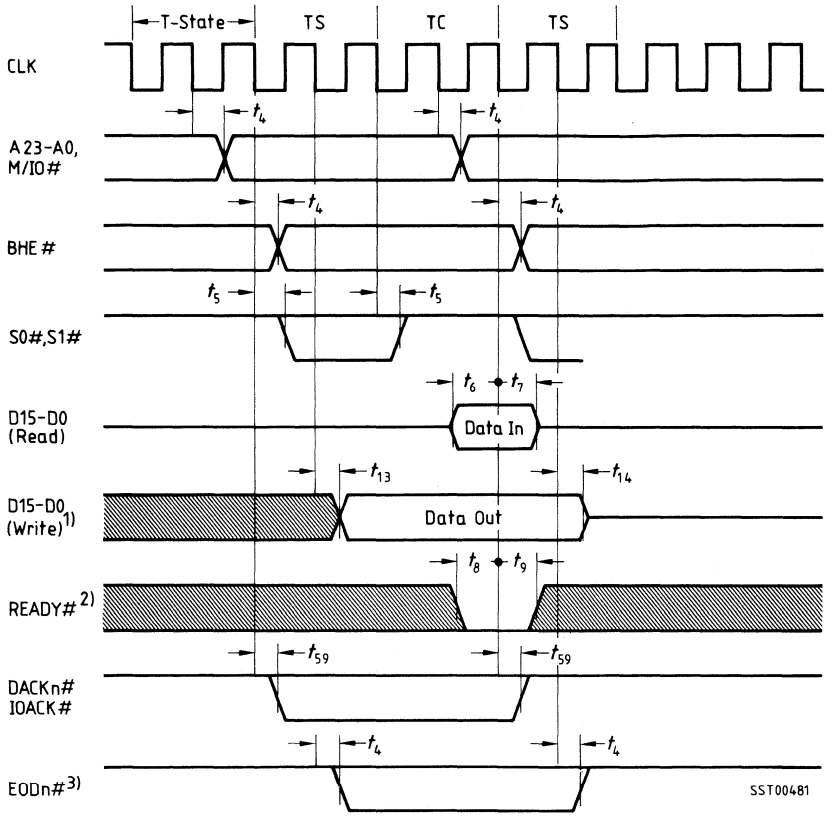
Clock Signal (286 mode)



Mode Selection on RESET (286 mode)

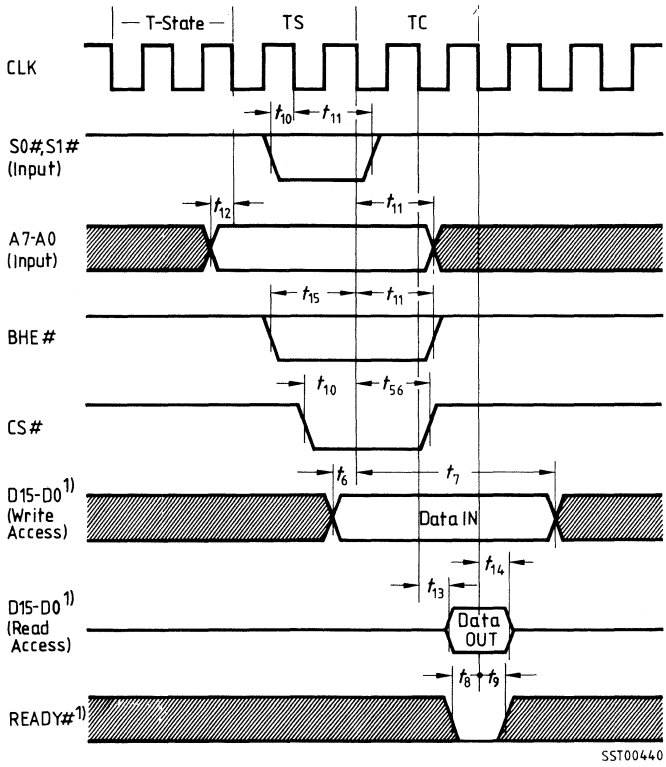


Major Timing for Active Bus Cycles (286 mode)



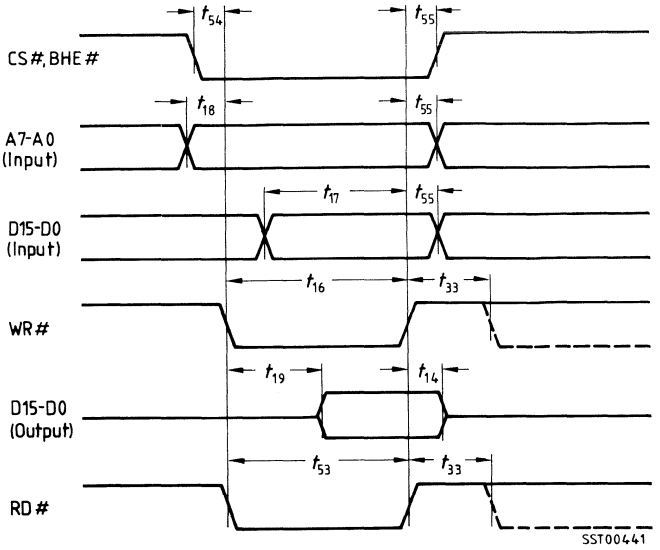
1) If executing a single cycle transfer, D15 to D0 float like during read cycles!
2) TC will be repeated, if READY# is inactive at the sampling point (end of current TC).
3) Initiated by terminal count.

Synchronous Access (286 mode)

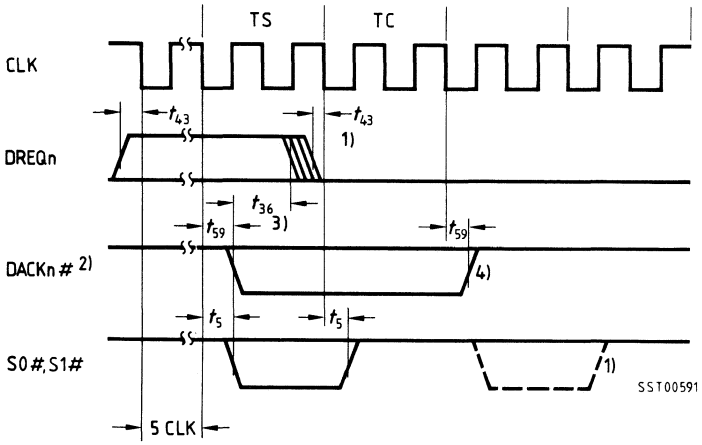


1) The processor will repeat TC, if READY# is not active at the sampling point (end of current TC). The SAB 82C258A will output data until the end of the repeated TC (read access) or sample the data bus again at the beginning of the repeated TC (write access).

Asynchronous Access (286 mode)

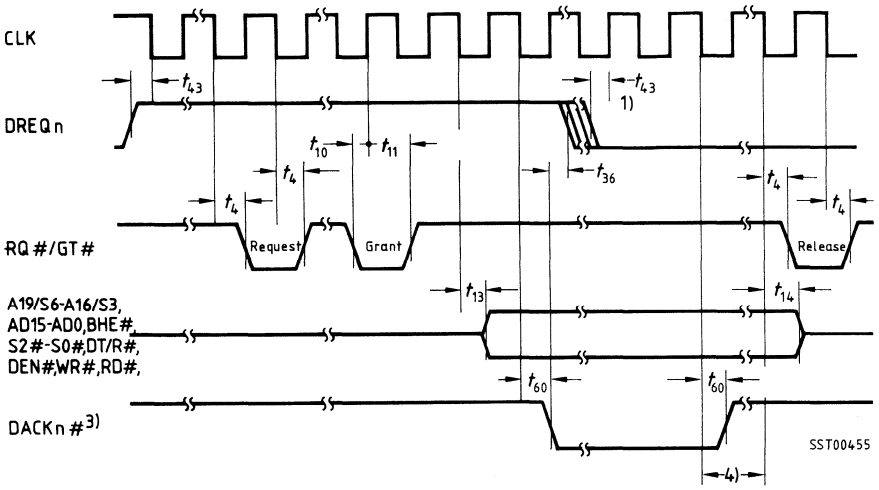


DMA Control Without Bus Arbitration (286 mode)



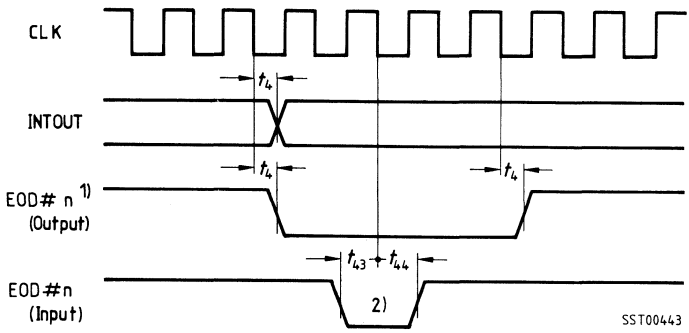
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) Minimum time to execute bus cycle.
4) If the SAB 82C258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

DMA Control With Bus Arbitration (286 mode)



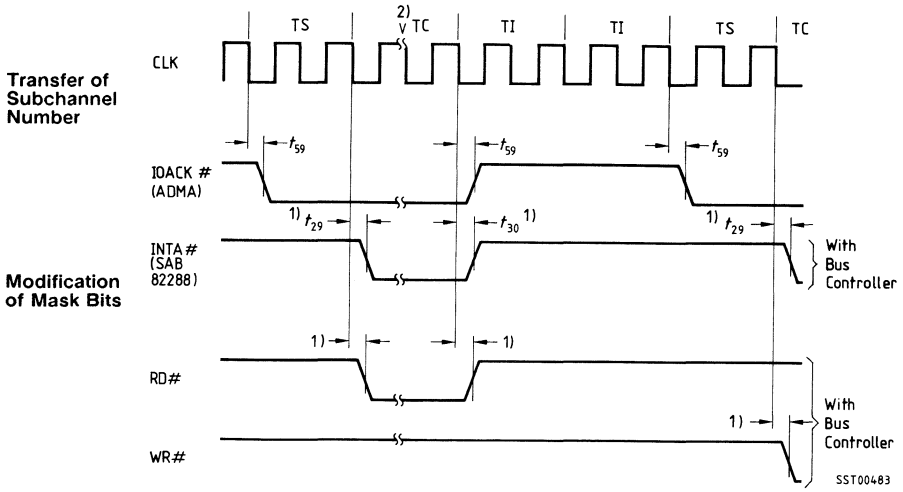
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) Minimum time to execute bus cycle.
4) If the SAB 82C258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.
5) The SAB 82C258A can be forced off the bus by driving HDLA inactive (see "Bus Arbitration").
6) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycle".
7) The SAB 82C258A may execute additional bus cycles, e.g. for command chaining.

EOD#/INTOUT Timing (286 mode)



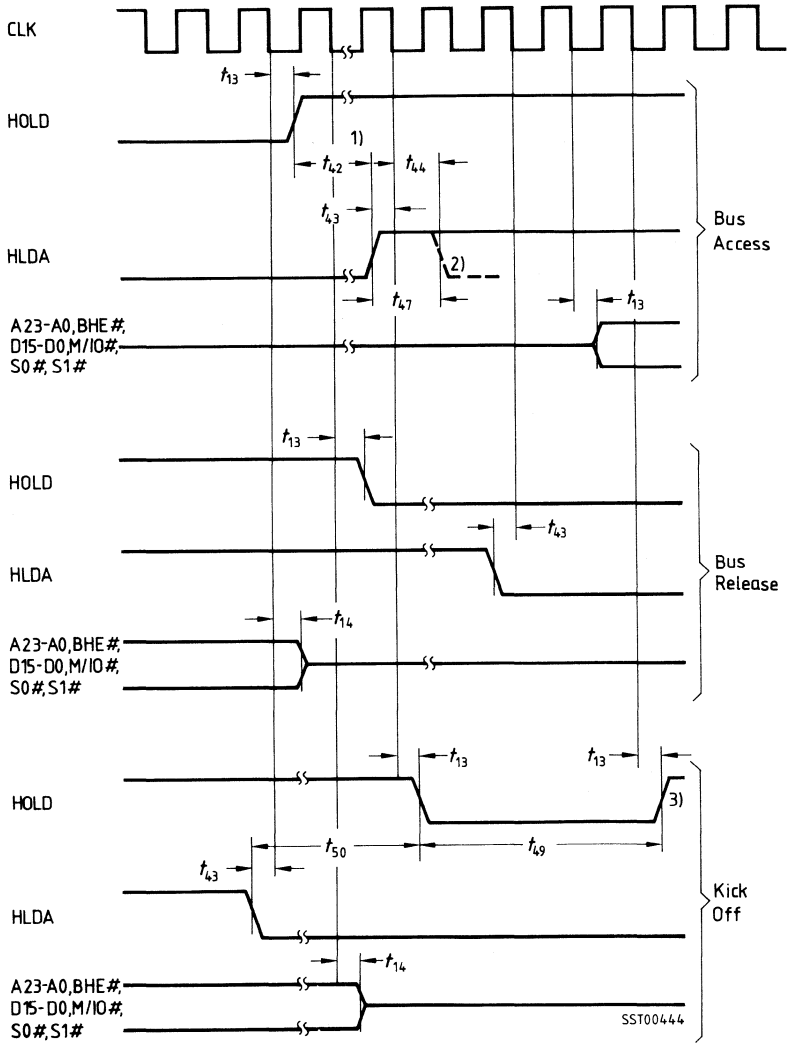
1) Initiated by type 2 command.
2) EOD# input minimum pulse width is 3 CLKs, if the signal is asynchronous.

Access to SAB 8259A (286 mode)



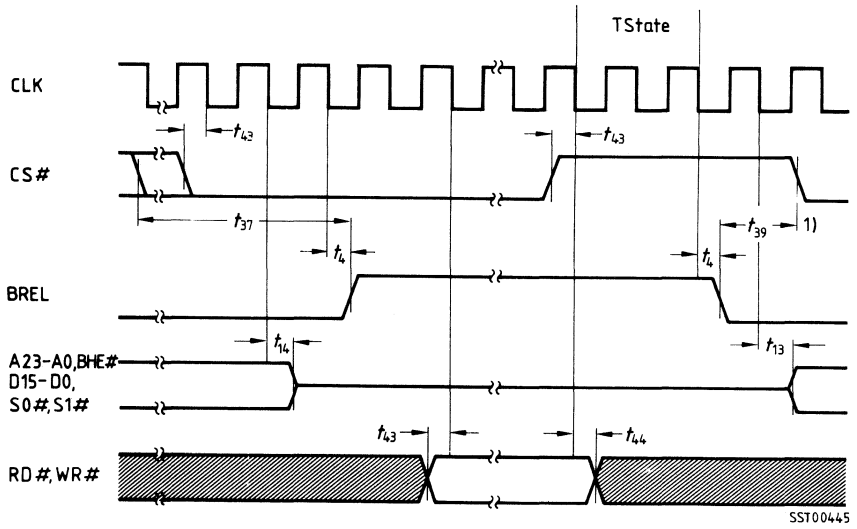
1) These timings are SAB 82288 timings!
2) Additional wait states may be inserted.

Bus Arbitration (286 mode)



1) To avoid arbitration conflicts, HLDA should not become active before HOLD.
2) Minimum HLDA high time before kick-off to respond to HOLD signal.
3) Earliest possible reactivation of HOLD after deactivation of HLDA.

Access in Remote Mode



1) Required to avoid bus conflicts.

This diagram shows the times when the output signals are driven active and input signals are recognized, rather than the exact timing.

AC Characteristics SAB 82C258A-1 (186 mode)

T_C = 0 to 85°C; V_{CC} = +5 V ±5%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Control output delay	t_4	5	44	ns	–
Sync address/data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync control input setup time	t_{10}	18	–	ns	–
Sync control/address input hold time	t_{11}	18	–	ns	–
Data/control delay	t_{13}	–	40	ns	C_L = 100 pF
Data float delay	t_{14}	–	40	ns	–
Write command width	t_{16}	2CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	1CLK + 30	–	ns	–
Async address setup time	t_{18}	20	–	ns	–
Async data access time	t_{19}	–	2CLK + t_{22} + t_{43} + t_{13}	ns	–
CLK cycle period	t_{20}	100	–	ns	–
CLK low time	t_{21}	44	–	ns	at 1.5 V
CLK high time	t_{22}	44	–	ns	at 1.5 V
CLK rise time	t_{23}	–	10	ns	1.0 to 3.5 V
CLK fall time	t_{24}	–	10	ns	3.5 to 1.0 V
AREADY active setup time	t_{25}	15	–	ns	2)
AREADY hold time	t_{26}	15	–	ns	2)
AREADY inactive setup time	t_{27}	25	–	ns	–
Mode select setup time	t_{28}	2CLK + 20	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Address/data output delay	t_{30}	10	40	ns	C_L = 20 to 200 pF
Status output delay	t_{31}	10	44	ns	–
Float delay	t_{32}	10	30	ns	–

AC Characteristics SAB 82C258A-1 (186 mode) cont'd

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Command recovery time	t_{33}	2CLK + t_{43} + t_{44}	–	ns	–
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
ALE output delay	t_{38}	–	30	ns	–
Address/control input hold time	t_{40}	10	–	ns	–
Address input setup time	t_{41}	45	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async control input setup time	t_{43}	20	–	ns	2)
Async control input hold time	t_{44}	20	–	ns	2)
HLDA hold time	t_{45}	5	–	ns	–
Async HLDA high time	t_{46}	1CLK + t_{43} + t_{45}	–	ns	3)
HOLD output delay	t_{48}	5	60	ns	–
HLDA output low time	t_{51}	2CLK − t_{48max}	–	ns	–
HLDA low to HOLD low delay	t_{52}	3CLK	16CLK + t_{43} + t_{48}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	20	–	ns	–
Async access hold time	t_{55}	20	–	ns	–
SREADY hold time	t_{57}	15	–	ns	–
Status setup time	t_{58}	35	–	ns	–
DACK# output delay	t_{60}	–	44	ns	–
Status hold time	t_{61}	0			

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 15 CLK
- normal pointer transfer (3 bus cycles): 12 CLK
- splitted pointer transfer (4 bus cycles): 16 CLK

If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

AC Characteristics SAB 82C258A-12 (186 mode)

T_C = 0 to 85°C; V_{CC} = +5 V ±5%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Control output delay	t_4	5	35	ns	–
Sync address/data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync control input setup time	t_{10}	15	–	ns	–
Sync control/address input hold time	t_{11}	15	–	ns	–
Data/control delay	t_{13}	–	35	ns	C_L = 100 pF
Data float delay	t_{14}	–	32	ns	–
Write command width	t_{16}	2CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	1CLK + 24	–	ns	–
Async address setup time	t_{18}	18	–	ns	–
Async data access time	t_{19}	–	2CLK + t_{22} + t_{43} + t_{13}	ns	–
CLK cycle period	t_{20}	80	–	ns	–
CLK low time	t_{21}	34	–	ns	at 1.5 V
CLK high time	t_{22}	34	–	ns	at 1.5 V
CLK rise time	t_{23}	–	10	ns	1.0 to 3.5 V
CLK fall time	t_{24}	–	10	ns	3.5 to 1.0 V
AREADY active setup time	t_{25}	15	–	ns	2)
AREADY hold time	t_{26}	15	–	ns	2)
AREADY inactive setup time	t_{27}	25	–	ns	–
Mode select setup time	t_{28}	2CLK + 18	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Address/data output delay	t_{30}	8	33	ns	C_L = 20 to 200 pF
Status output delay	t_{31}	8	35	ns	–
Float delay	t_{32}	8	25	ns	–

AC Characteristics SAB 82C258A-12 (186 mode) cont'd

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Command recovery time	t_{33}	2CLK + t_{43} + t_{44}	–	ns	–
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
ALE output delay	t_{38}	–	25	ns	–
Address/control input hold time	t_{40}	8	–	ns	–
Address input setup time	t_{41}	40	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async control input setup time	t_{43}	18	–	ns	2)
Async control input hold time	t_{44}	18	–	ns	2)
HLDA hold time	t_{45}	4	–	ns	–
Async HLDA high time	t_{46}	1CLK + t_{43} + t_{45}	–	ns	3)
HOLD output delay	t_{48}	4	50	ns	–
HLDA output low time	t_{51}	2CLK – t_{48max}	–	ns	–
HLDA low to HOLD low delay	t_{52}	3CLK	16CLK + t_{43} + t_{48}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	18	–	ns	–
Async access hold time	t_{55}	18	–	ns	–
SREADY hold time	t_{57}	15	–	ns	–
Status setup time	t_{58}	30	–	ns	–
DACK# output delay	t_{60}	–	35	ns	–
Status hold time	t_{61}	0			

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 15 CLK
- normal pointer transfer (3 bus cycles): 12 CLK
- splitted pointer transfer (4 bus cycles): 16 CLK

If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

AC Characteristics SAB 82C258A-16 (186 mode)

T_C = 0 to 85°C; V_{CC} = +5 V ±5%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Control output delay	t_4	5	25	ns	–
Sync address/data setup time	t_6	10	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync control input setup time	t_{10}	12	–	ns	–
Sync control/address input hold time	t_{11}	12	–	ns	–
Data/control delay	t_{13}	–	30	ns	C_L = 100 pF
Data float delay	t_{14}	–	28	ns	–
Write command width	t_{16}	2CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	1CLK + 20	–	ns	–
Async address setup time	t_{18}	14	–	ns	–
Async data access time	t_{19}	–	2CLK + t_{22} + t_{43} + t_{13}	ns	–
CLK cycle period	t_{20}	62	–	ns	–
CLK low time	t_{21}	26	–	ns	at 1.5 V
CLK high time	t_{22}	26	–	ns	at 1.5 V
CLK rise time	t_{23}	–	8	ns	1.0 to 3.5 V
CLK fall time	t_{24}	–	8	ns	3.5 to 1.0 V
AREADY active setup time	t_{25}	15	–	ns	2)
AREADY hold time	t_{26}	15	–	ns	2)
AREADY inactive setup time	t_{27}	25	–	ns	–
Mode select setup time	t_{28}	2CLK + 14	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Address/data output delay	t_{30}	5	30	ns	C_L = 20 to 200 pF
Status output delay	t_{31}	5	30	ns	–
Float delay	t_{32}	5	20	ns	–

AC Characteristics SAB 82C258A-16 (186 mode) cont'd

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Command recovery time	t_{33}	2CLK + t_{43} + t_{44}	–	ns	–
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
ALE output delay	t_{38}	–	20	ns	–
Address/control input hold time	t_{40}	5	–	ns	–
Address input setup time	t_{41}	30	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async control input setup time	t_{43}	14	–	ns	2)
Async control input hold time	t_{44}	14	–	ns	2)
HLDA hold time	t_{45}	4	–	ns	–
Async HLDA high time	t_{46}	1CLK + t_{43} + t_{45}	–	ns	3)
HOLD output delay	t_{48}	4	40	ns	–
HLDA output low time	t_{51}	2CLK – t_{48max}	–	ns	–
HLDA low to HOLD low delay	t_{52}	3CLK	16CLK + t_{43} + t_{48}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	14	–	ns	–
Async access hold time	t_{55}	14	–	ns	–
SREADY hold time	t_{57}	15	–	ns	–
Status setup time	t_{58}	25	–	ns	–
DACK# output delay	t_{60}	–	25	ns	–
Status hold time	t_{61}	0			

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 15 CLK
- normal pointer transfer (3 bus cycles): 12 CLK
- splitted pointer transfer (4 bus cycles): 16 CLK

If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

AC Characteristics SAB 82C258A-20 (186 mode)

T_C = 0 to 85°C; V_{CC} = +5 V ±5%
Any output timing is measured at 1.5 V

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Control output delay	t_4	3	21	ns	–
Sync address/data setup time	t_6	8	–	ns	–
Sync data hold time	t_7	5	–	ns	–
Sync control input setup time	t_{10}	8	–	ns	–
Sync control/address input hold time	t_{11}	8	–	ns	–
Data/control delay	t_{13}	–	25	ns	C_L = 100 pF
Data float delay	t_{14}	–	24	ns	–
Write command width	t_{16}	2CLK + t_{43} + t_{44}	–	ns	–
Async data setup time	t_{17}	1CLK + 16	–	ns	–
Async address setup time	t_{18}	11	–	ns	–
Async data access time	t_{19}	–	2CLK + t_{22} + t_{43} + t_{13}	ns	–
CLK cycle period	t_{20}	50	–	ns	–
CLK low time	t_{21}	21	–	ns	at 1.5 V
CLK high time	t_{22}	21	–	ns	at 1.5 V
CLK rise time	t_{23}	–	7	ns	1.0 to 3.5 V
CLK fall time	t_{24}	–	7	ns	3.5 to 1.0 V
AREADY active setup time	t_{25}	12	–	ns	2)
AREADY hold time	t_{26}	12	–	ns	2)
AREADY inactive setup time	t_{27}	20	–	ns	–
Mode select setup time	t_{28}	2CLK + 11	–	ns	–
Mode select hold time	t_{29}	0	–	ns	–
Address/data output delay	t_{30}	4	25	ns	C_L = 20 to 200 pF
Status output delay	t_{31}	4	25	ns	–
Float delay	t_{32}	4	20	ns	–

AC Characteristics SAB 82C258A-20 (186 mode) cont'd

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Command recovery time	t_{33}	2CLK + t_{43} + t_{44}	–	ns	–
DREQ inactive after DACK# active	t_{36}	0	–	ns	–
ALE output delay	t_{38}	–	18	ns	–
Address/control input hold time	t_{40}	4	–	ns	–
Address input setup time	t_{41}	24	–	ns	–
HOLD active to HLDA active	t_{42}	0	–	ns	–
Async control input setup time	t_{43}	11	–	ns	2)
Async control input hold time	t_{44}	11	–	ns	2)
HLDA hold time	t_{45}	3	–	ns	–
Async HLDA high time	t_{46}	1CLK + t_{43} + t_{45}	–	ns	3)
HOLD output delay	t_{48}	3	30	ns	–
HLDA output low time	t_{51}	2CLK – t_{48max}	–	ns	–
HLDA low to HOLD low delay	t_{52}	3CLK	16CLK + t_{43} + t_{48}	ns	1)
Read Command width	t_{53}	t_{19}	–	ns	–
Async access setup time	t_{54}	11	–	ns	–
Async access hold time	t_{55}	11	–	ns	–
SREADY hold time	t_{57}	10	–	ns	–
Status setup time	t_{58}	20	–	ns	–
DACK# output delay	t_{60}	–	21	ns	–
Status hold time	t_{61}	0			

1) The minimum value is due to internal synchronization when no channel is active.
The maximum delay is caused by a sequence of locked bus cycles:
- IOACK sequence on MUX ch. (3 bus cycles): 15 CLK
- normal pointer transfer (3 bus cycles): 12 CLK
- splitted pointer transfer (4 bus cycles): 16 CLK

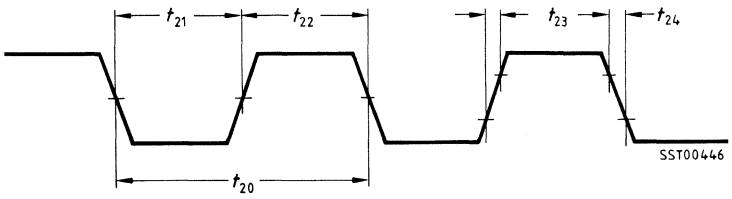
If wait states are used, the time required for the wait states of three or four (splitted pointer) bus cycles has to be added.

2) These specifications are given for testing purposes only to assure recognition at a specific clock edge.

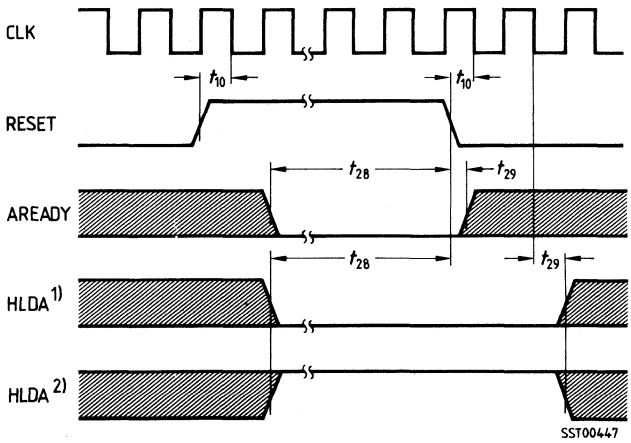
3) This timing is valid, if the signal is not synchronous, i.e. does not meet the specific setup and hold times.

Waveforms

Clock Signal (186 mode)

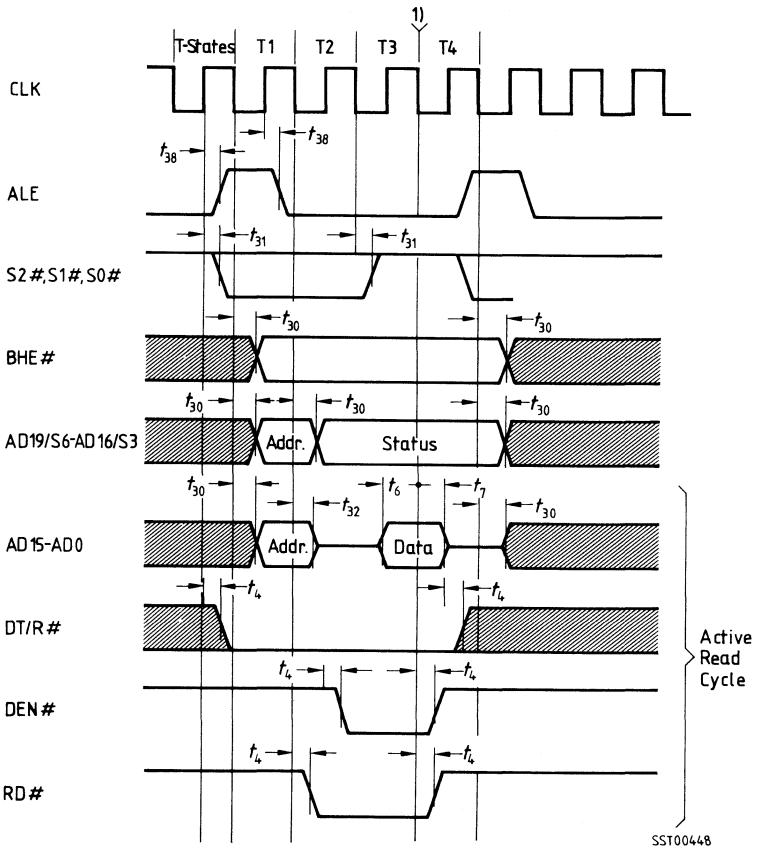


Mode Selection on RESET (186 mode)



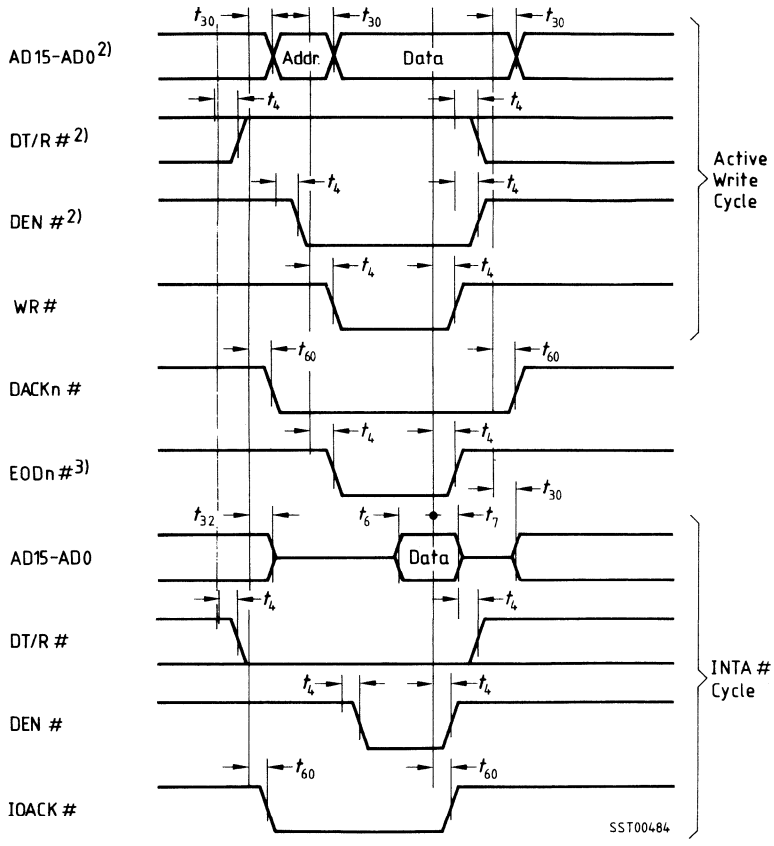
1) To operate in 186 mode with HOLD HLDA protocol.
2) To operate in 8086 mode with RQ#/GT# protocol.

Major Timing for Active Bus Cycle (186 mode) a)



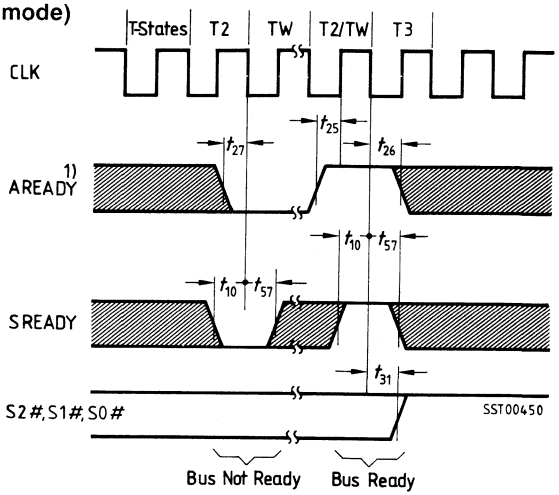
1) A wait state is inserted after T3 or TW, whenever the bus is not ready at the beginning of T3 or TW (see "Bus Cycle Termination"). The status must be valid just prior to T4.

Major Timing for Active Bus Cycle (186 mode) b)



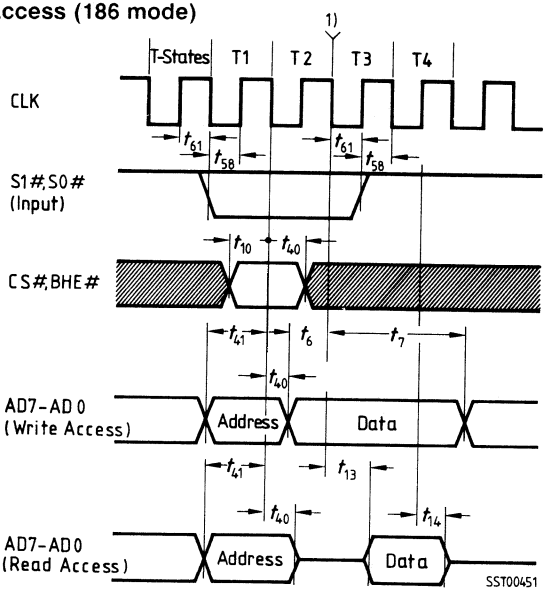
2) For a single-cycle transfer the timing of AD15-AD0,DT R# and DEN# is identical to a read cycle. AD15-AD0 will float as during a read cycle.
3) Initiated by terminal count.

Bus Cycle Termination (186 mode)



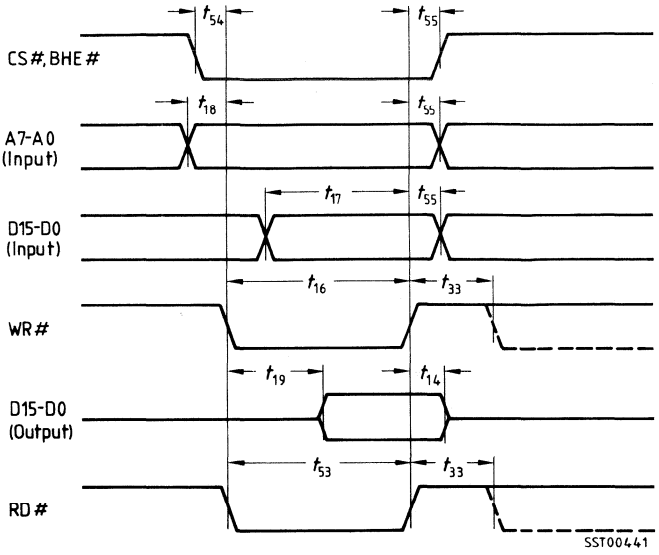
1) Only the rising edge of AREADY is synchronized internally to CLK.
The falling edge must be synchronized externally.

Synchronous Access (186 mode)

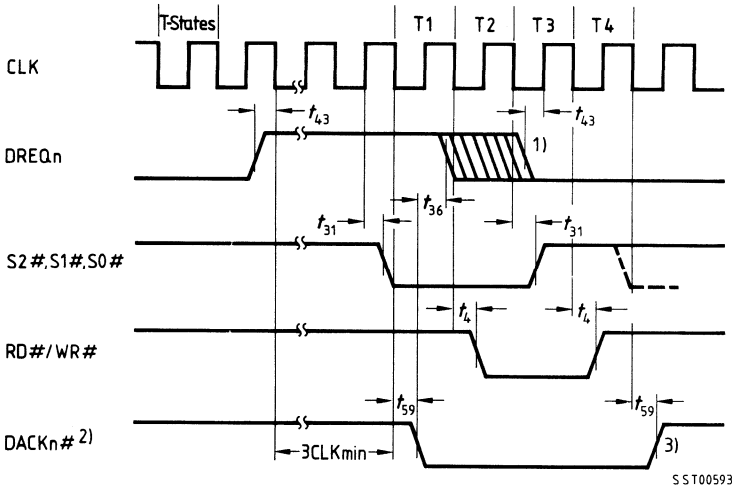


1) Additional wait cycles may be inserted. Status must be valid just prior to T4.

Asynchronous Access (186 mode)

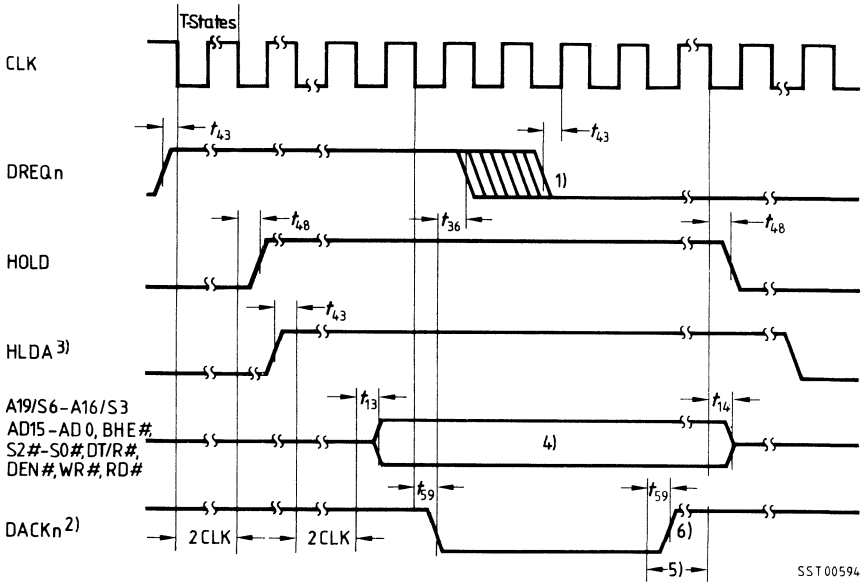


DMA Control Without Bus Arbitration (186 mode)



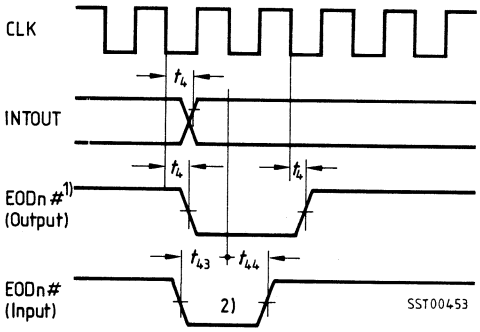
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) If the SAB 82258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

DMA Control With Bus Arbitration (186 mode)



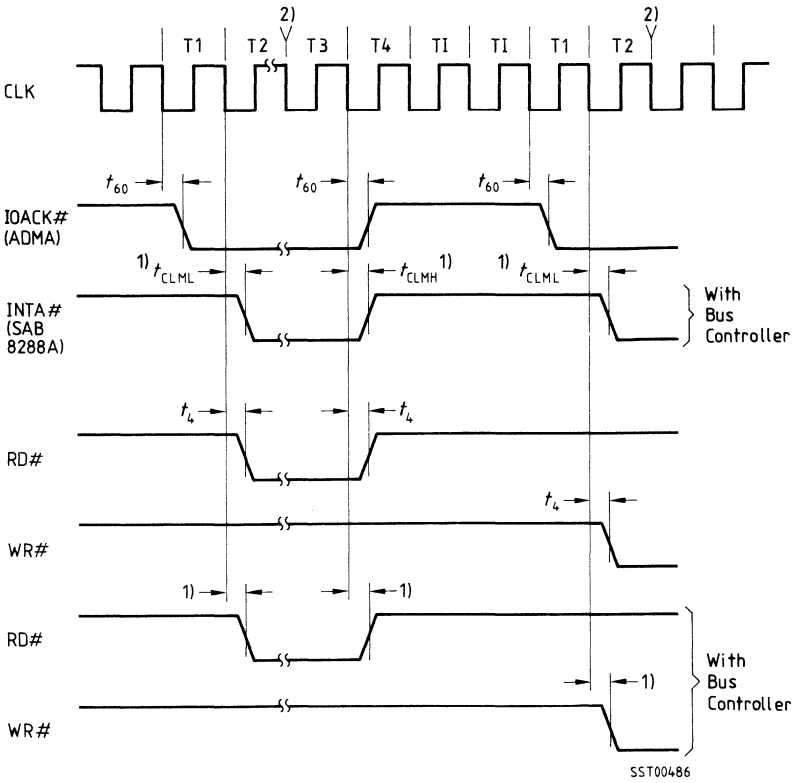
1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.
2) Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.
3) The SAB 82258A can be forced off the bus by driving HDLA inactive (see "Bus Arbitration").
4) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycle".
5) The SAB 82258A may execute additional bus cycles, e.g. for command chaining.
6) If the SAB 82258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn# signal can be prolonged by two T-states.

EOD#/INTOUT Timing (186 mode)



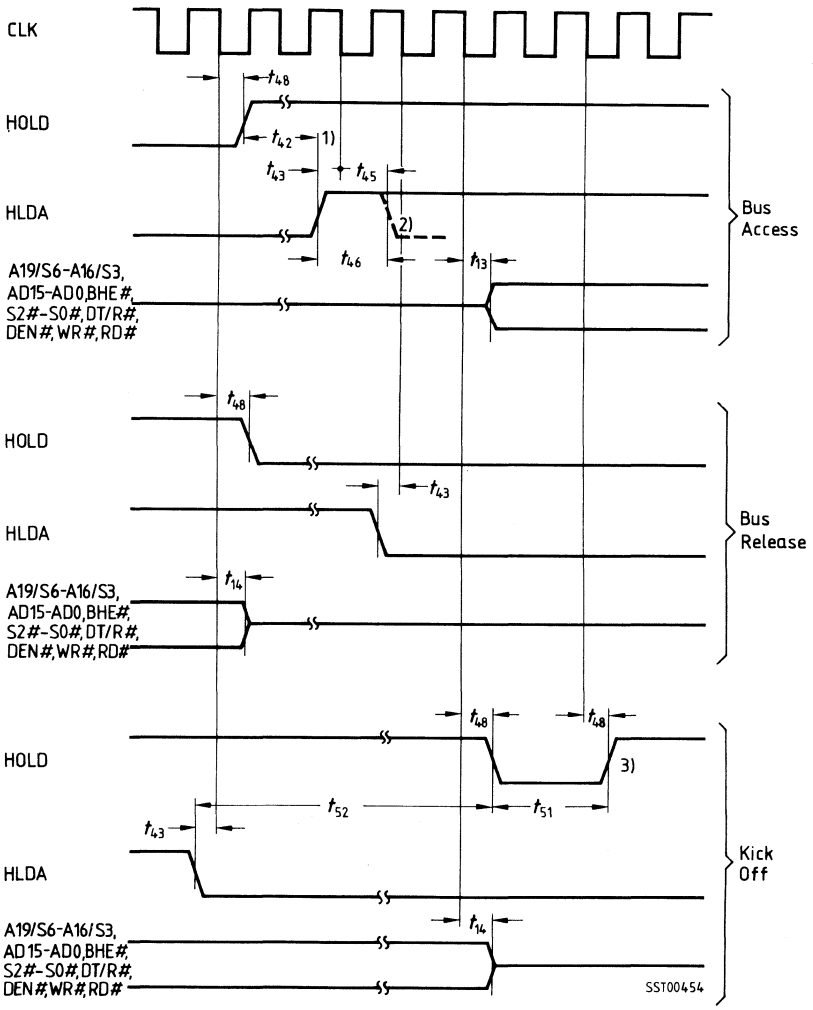
1) Initiated by type 2 command.
2) EOD# input minimum pulse width is 2 CLKs, if the signal is asynchronous.

Access to SAB 8259A (186 mode)



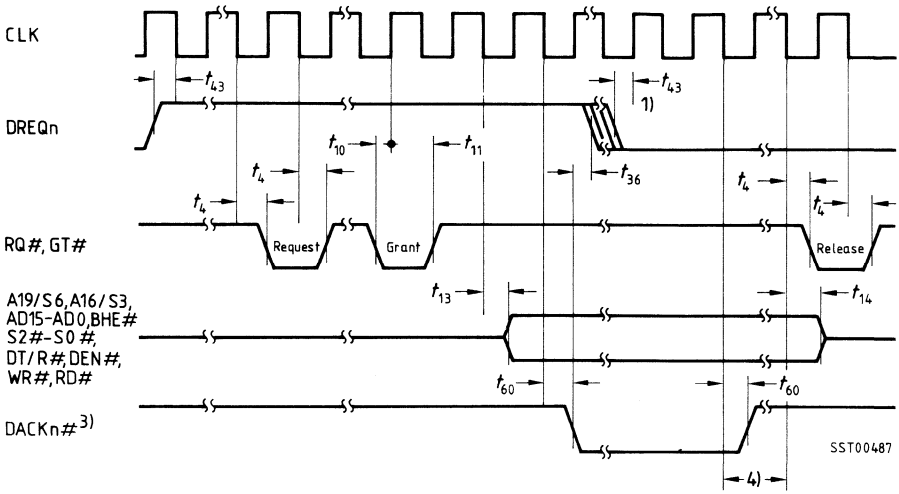
1) These timings are SAB 8288A timings!
2) Additional wait states may be inserted.

Bus Arbitration (186 mode)



1) To avoid arbitration conflicts, HLDA should not become active before HOLD.
2) Minimum HLDA high time before kick-off to respond to HOLD signal.
3) Earliest possible reactivation of HOLD after deactivation of HLDA.

DMA Control with RQ#/GT# Protocol (8086 mode)



1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent bus cycles are executed.
2) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".
3) Refers to the highest priority request. Acknowledge of lower priority requests may be delayed by higher priority requests.
4) The SAB 82258A may execute additional bus cycles, e.g. for command chaining.

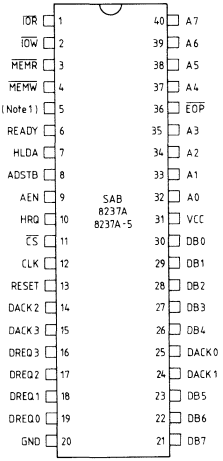
SIEMENS

Preliminary

SAB 8237A, SAB 8237A-5 High Performance Programmable DMA Controller

- Four Independent DMA Channels
- Enable/Disable Control of Individual DMA Requests
- Memory-to-Memory Transfers
- Memory Block Initialization
- Address Increment or Decrement
- Independent Autoinitialization of all Channels
- High performance: Transfers up to 1.6 MBytes/Second with 5 MHz SAB 8237A-5
- Directly Expandable to any Number of Channels
- End of Process Input for Terminating Transfers
- Software DMA Requests
- Independent Polarity Control for DREQ and DACK Signals
- Single +5 V Power Supply
- 40 Pin Dual-In-Line Package
- Fully compatible with the Industry Standard 9517A/8237A

Pin Configuration



1) Pin always tied high

Pin Names

DB7-DB0	Data Bus (bidirectional)
$\overline{IOR}$, $\overline{IOW}$	I/O Read and Write Input/Output
$\overline{MEMR}$, $\overline{MEMW}$	Memory Read and Write Output
A0-A3	Address Input/Output
A4-A7	Adress Output
$\overline{CS}$	Chip Select Input
CLK	Clock Input
READY	Ready Input
HRQ	Hold Request Output
$\overline{HLDA}$	Hold Acknowledge Input
RESET	Reset Input
DREQ0-DREQ3	DMA Request Input
$\overline{DACK0}$-$\overline{DACK3}$	DMA Acknowledge Output
AEN	Address Enable Output
ADSTB	Address Strobe Output
$\overline{EOP}$	End of Process Input/Output

The SAB 8237A Multimode Direct Memory Access (DMA) Controller is designed to improve system performance by allowing external devices to directly transfer information to or from system memory. Memory-to-memory transfer capability is also provided.

The SAB 8237A contains four independent channels, each with a separate register set, and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original state following an End of Process ($\overline{EOP}$). Each channel has a full 64K address and word count capability.

The SAB 8237A is fabricated in +5 V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP. The SAB 8237A-5 is the 5 MHz version of the standard 3 MHz SAB 8237A respectively.

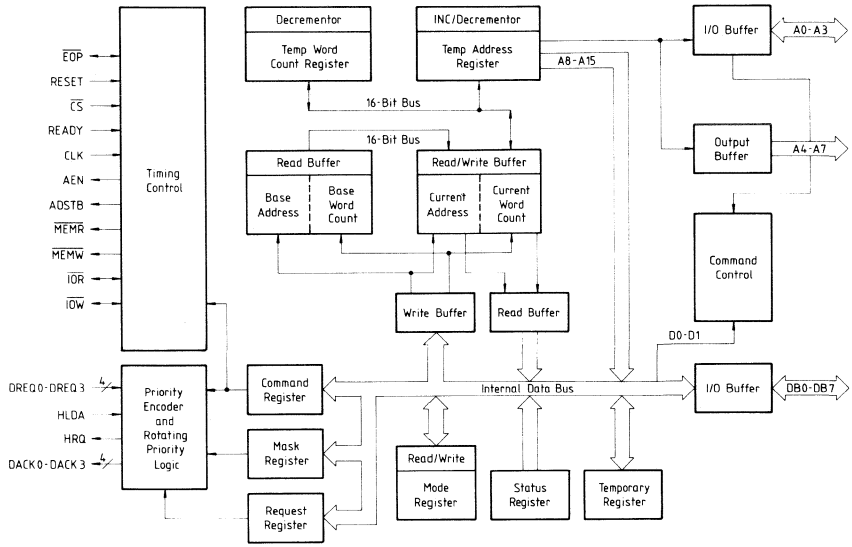
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
$\overline{IOR}$	1	I/O	I/O READ I/O Read is a bidirectional active low three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the SAB 8237A to access data from a peripheral device during a DMA Write transfer.
$\overline{IOW}$	2	I/O	I/O WRITE I/O Write is a bidirectional active low three-state line. In the idle cycle it is an input control signal used by the CPU to load information into the SAB 8237A. In the Active cycle it is an output control signal used by the SAB 8237A to load data to a peripheral device during a DMA Read transfer. Write operations by the CPU to the SAB 8237A require a rising $\overline{IOW}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.
$\overline{MEMR}$	3	0	MEMORY READ The Memory Read signal is an active low three-state output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.
$\overline{MEMW}$	4	0	MEMORY WRITE The Memory Write signal is an active low three-state output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.
–	5	I	Pin 5 must be tied high.
READY	6	I	READY Ready is an input used to extend the memory read and write pulses from the SAB 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
HLDA	7	I	HOLD ACKNOWLEDGE The active high Hold Acknowledge from the CPU indicates that control of the system busses has been relinquished.
ADSTB	8	O	ADDRESS STROBE The active high Address Strobe is used to strobe the upper address byte from DBØ-DB7 into an external latch.
AEN	9	O	ADDRESS ENABLE Address Enable is an active high signal used to disable the system bus during DMA cycles and to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HLDA and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The SAB 8237A automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.

Symbol	Number	Input (I) Output (O)	Function
HRQ	10	O	HOLD REQUEST The Hold Request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the SAB 8237A to issue HRQ.
$\overline{CS}$	11	I	CHIP SELECT Chip Select is an active low input used to select the SAB 8237A as an I/O device during an I/O Read or I/O Write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the SAB 8237A by the host CPU $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.
CLK	12	I	CLOCK This input controls the internal operations of the SAB 8237A and its rate of data transfers. The input may be driven at up to 3 MHZ for the standard SAB8237A and up to 5 MHz for the SAB 8237A-5.
RESET	13	I	RESET Reset is an asynchronous active high input which clears the Command, Status, Request and Temporary register. It also clears the First/Last Flip/Flop and sets the Mask register. Following a Reset the device is in the idle cycle.
DACKØ DACK1 DACK2 DACK3	25 24 14 15	O O O O	DMA ACKNOWLEDGE The DMA Acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.
DREQØ DREQ1 DREQ2 DREQ3	19 18 17 16	I I I I	DMA REQUEST The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service in Fixed Priority, DREQØ has the highest priority and and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. The Polarity of DREQ is programmable. Reset initializes these lines to active high.
DBØ-DB7	30-26, 23-21	I/O	DATA BUS The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled during the I/O Read by the host CPU, permitting the CPU to examine the contents of an Address register, the Status register, the Temporary register or a Word Count register. The Data Bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the SAB 8237A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the SAB 8237A's Temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the Temporary register data into the destination memory location.

Symbol	Number	Input (I) Output (O)	Function
A0–A3	32–35	I/O	ADDRESS 0–3 The four least significant address lines are bidirectional 3-state signals. During DMA idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4-bits of the output address.
A4–A7	37–40	O	ADDRESS 4–7 The four most significant address lines are three-state outputs and provide four bits of address. These lines are enabled only during DMA service.
$\overline{EOP}$	36	I/O	END OF PROCESS $\overline{EOP}$ is an active low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's Word Count goes to zero, the SAB 8237A pulses $\overline{EOP}$ low to provide the peripheral with a completion signal. $\overline{EOP}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{EOP}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the Status register and to reset its request bit. If Autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ always applies to the channel with an active DACK; external $\overline{EOP}$s are disregarded when DACK0-DACK3 are all inactive if the DMA is in state SI. In situations where two or more SAB 8237A DMAs are cascaded, the $\overline{EOP}$ pins should be logically OR'ed (not wire-OR'ed). Because $\overline{EOP}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3 kΩ or 4.7 kΩ are recommanded; the $\overline{EOP}$ pin cannot sink the current passed by a 1 kΩ pullup.
VCC	31	–	POWER SUPPLY (+5 V)
GND	20	–	GROUND (0 V)

Block Diagram



Register Description

Current Address Register
Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer.

Current Word Count Register
Each channel has a 16-bit Current Word Count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated.

Base Address and Base Word Count Registers
Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original values of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes during DMA programming by the microprocessor.

Command Register
This 8-bit register controls the operation of the SAB 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset.

Mode Registers
Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

Request Register
The SAB 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset.

Mask Register
Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset.

Status Register
The Status registers may be read out of the SAB 8237A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests.

Temporary Register
The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition.

Functional Description

DMA Operation
The SAB 8237A is designed to operate in two major cycles. These are called Idle and Activa cycles. Each device cycle is made up of a number of states. State I (SI)is the inactive state. It is entered when the SAB 8237A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The SAB 8237A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted before S4 by the use of the Ready line on the SAB 8237A.
Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for each complete transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23 and S24) for the write-to-memory half of the transfer.

Idle Cycle
When no channel is requesting service, the SAB 8237A will enter the Idle cycle and perform "SI" states. In this cycle the SAB 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the SAB 8237A.

Active Cycle
When the SAB 8237A is in the Idle cycle and a channel requests a DMA service, the device will output a HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode
In Single Transfer mode, the SAB 8237A will make a one-byte transfer during each HRQ/HLDA handshake. When DREQ goes active, HRQ will go active. After the CPU responds by driving HRQ active, a one-byte transfer will take place. Following the transfer, HRQ will go inactive, the word count will be decremented and the address will be either incremented or decremented.

Block Transfer Mode
In Block Transfer mode, the SAB 8237A will continue making transfers until a TC (caused by the word count going to zero) or an external End of Process ($\overline{EOP}$) is encountered.

Demand Transfer Mode
In Demand Transfer mode the device will continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again.

Cascade Mode
This mode is used to cascade more than one SAB 8237A together for simple system expansion. The HRQ and HLDA signals from the additional SAB 8237A are connected to the DREQ and DACK signals of a channel of the initial SAB 8237A.

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{IOR}$ and $\overline{MEMW}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers; the SAB8237A operates as in Read or Write transfers generating addresses, responding to $\overline{EOP}$, etc., however, the memory and I/O control lines remain inactive.

Memory-to-Memory

The SAB8237A includes a block move capability that allows blocks of data to be moved from one memory adress space to another. Channel Ø forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel Ø.

Autoinitialize

By programming a bit in the Mode register a channel may be set up for an Autoinitialize operation. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of that channel following $\overline{EOP}$.

Extended Write

For Flyby Transactions late write is normally used, as this allows sufficient time for the $\overline{IOR}$ signal to get data from the peripheral onto the bus before $\overline{MEMW}$ is activated. In some systems, performance can be improved by starting the write cycle earlier.

Address Generation

In order to reduce pin count, the SAB 8237A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through the 3-state enable control signal of the latch. The lower order address bits are output by the SAB 8237A directly. To save time and speed transfers, the SAB 8237A executes S1 states only when updating of A8–A15 in the latch is necessary.

Compressed Timing

In order to achieve even greater throughput where system characteristics permit, the SAB 8237A can compress the transfer time to two clock cycles. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write.

Priority

The SAB 8237A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel Ø. The second schema is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

Software Commands

There are two special software commands which can be executed in the Program Condition.
Clear First/Last Flip/Flop: This command may be issued prior to writing or reading SAB 8237A address or word count information. This initializes the Flip/Flop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.
Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary and Internal First/Last Flip/Flop registers are cleared and the Mask register is set.

Absolute Maximum Ratings [1]

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to + 150°C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to + 7 V
Power Dissipation	2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = 5 V ± 5%; VSS = 0 V

Symbol	Parameter	Limit Values			Unit	Test Condition	
		Min.	Typ. [2]	Max.			
*V*OH	Output High Voltage	2.4	–	–	V	*I*OH = −200 µA	
		3.3				*I*OH = −100 µA (HRQ only)	
*V*OL	Output Low Voltage	–		0.40		*I*OL = 3.2 mA	
*V*IH	Input High Voltage	2.0		*V*CC+0.5		–	
*V*IL	Input Low Voltage	−0.5		0.8			
*I*LI	Input Load Current	–		±10	µA	0 V ≤ *V*IN ≤ *V*CC	
*I*LO	Output Leakage Current					0.4 V ≤ *V*OUT < *V*CC	
*I*CC	VCC Supply Current		110	130	mA	TA = +25°C	All outputs disconnected
			130	150		TA = 0°C	
CO	Output Capacitance		4	8	pF	fc = 1.0 MHz, Inputs = 0 V	
CI	Input Capacitance		8	15			
CIO	I/O Capacitance		10	18			

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) Typical values are for TA = 25°C, nominal supply voltage and nominal processing parameters.

A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 5%; V_{SS} = 0 V

DMA (Master) Mode

Symbol	Parameter	Limit Values				Unit
		8237A		8237A-5		
		Min.	Max.	Min.	Max.	
TAEL	AEN High from CLK Low (S1) Delay Time	–	300	–	200	ns
TAET	AEN Low from CLK High (S1) Delay Time		200		130	
TAFAB	ADR Active to Float Delay from CLK High		150		90	
TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float from CLK High		150		120	
TAFDB	DB Active to Float Delay from CLK High		250		170	
TAHR	ADR from $\overline{READ}$ High Hold Time	TCY–100	–	TCY–100	–	
TAHS	DB from ADSTB Low Hold Time	50		40		
TAHW	ADR from $\overline{WRITE}$ High Hold Time	TCY –50		TCY –50		
TAK	DACK Valid from CLK Low Delay Time [1]	–	250	–	170	
	$\overline{EOP}$ High from CLK High Delay Time [2]		250		170	
	$\overline{EOP}$ Low to CLK High Delay Time		250		170	
TASM	ADR Stable from CLK High		250		170	
TASS	DB to ADSTB Low Setup Time	100	–	100	ns	
TCH	CLK High Time (transitions ≤ 10 ns)	120		80	–	
TCL	CLK Low Time (transitions ≤ 10 ns)	150		68		
TCY	CLK Cycle Time	320		200		
TDCL	CLK High to $\overline{READ}$ or $\overline{WRITE}$ Low Delay [3]	–	270	–	190	
TDCTR	$\overline{READ}$ High from CLK High (S4) Delay Time [3]		270		190	
TDCTW	$\overline{WRITE}$ High from CLK High (S4) Delay Time [3]		200		130	
TDQ1	HRQ Valid from CLK High Delay Time [4]		160		120	
TDQ2			250		120	
TEPS	$\overline{EOP}$ Low from CLK Low Setup Time	60	–	40	–	
TEPW	$\overline{EOP}$ Pulse Width	300		220		
TFAAB	ADR Float to Active Delay from CLK High	–	250	–	170	
TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK High		200		150	
TFADB	DB Float to Active Delay from CLK High		300		200	

Notes see next page.

Symbol	Parameter	Limit Values				Unit
		8237A		8237A-5		
		Min.	Max.	Min.	Max.	
THS	HLDA Valid to CLK High Setup Time	100		75		
TIDH	Input Data from $\overline{\text{MEMR}}$ High Hold Time	0		0		
TIDS	Input Data to $\overline{\text{MEMR}}$ High Setup Time	250		170		
TODH	Output Data from $\overline{\text{MEMW}}$ High Hold Time	20	–	10	–	ns
TODV	Output Data Valid to $\overline{\text{MEMW}}$ High [5]	200		125		
TQS	DREQ to CLK Low (S1, S4) Setup Time [1]	0		0		
TRH	CLK to READY Low Hold Time	20		20		
TRS	READY to CLK Low Setup Time	100		60		
TSTL	ADSTB High from CLK High Delay Time	–	200	–	130	
TSTT	ADSTB Low from CLK High Delay Time		140		90	
TQH	DREQ from DACK Valid Hold Time	0	–	0	–	
TRQHA	HRQ to HLDA Delay Time	1		1		clk

1) DREQ and DACK signals may be active high or low. Timing diagrams assume the active high mode.

2) $\overline{\text{EOP}}$ is an open collector output. This parameter assumes the presence of a 2.2 kΩ pullup to *VCC*.

3) The net $\overline{\text{IOW}}$ or $\overline{\text{MEMW}}$ pulse width for normal write will be TCY -100 ns and for extended write will be 2TCY -100 ns. The net $\overline{\text{IOR}}$ or $\overline{\text{MEMR}}$ pulse width for normal read will be 2TCY -50 ns and for compressed read will be TCY -50 ns.

4) TDQ is specified for two different output high levels. TDQ1 is measured at 2.0 V. TDQ2 is measured a 3.3 V. The value for TDQ2 assumes an external 3.3 kΩ pull-up resistor connected from HRQ to *VCC*.

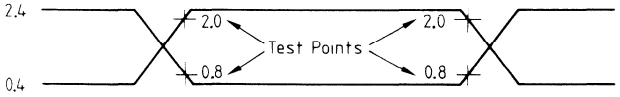
5) If N wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by N (TCY).

Peripheral (Slave) Mode

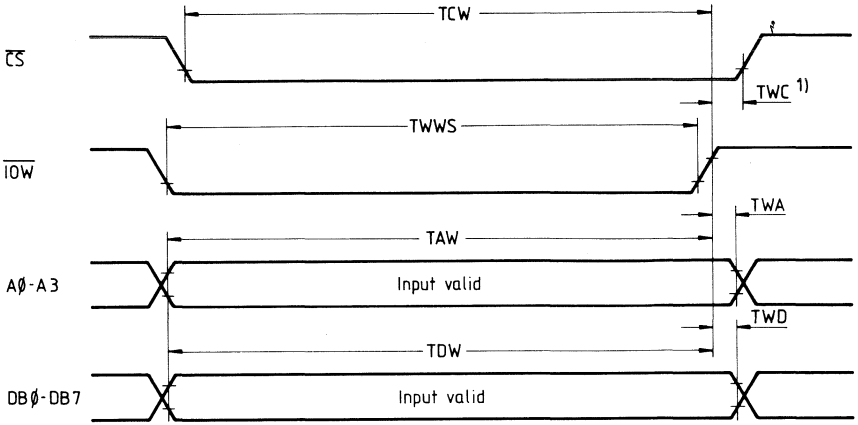
Symbol	Parameter	Limit Values				Unit
		8237A		8237A-5		
		Min.	Max.	Min.	Max.	
TAR	ADR Valid or $\overline{CS}$ Low to $\overline{READ}$ Low	50		50		
TAW	ADR Valid to $\overline{WRITE}$ High Setup Time	200		130		
TCW	$\overline{CS}$ Low to $\overline{WRITE}$ High Setup Time	200	–	130	–	
TDW	Data Valid to $\overline{WRITE}$ High Setup Time	200		130		
TRA	ADR or $\overline{CS}$ Hold from $\overline{READ}$ High	0		0		
TRDE	Data Access from $\overline{READ}$ Low [1]	–	200	–	140	
TRDF	DB Float Delay from $\overline{READ}$ High	20	100	0	70	ns
TRSTD	Power Supply High to RESET Low Setup Time	500		500		
TRSTS	RESET to First $\overline{IOWR}$	2 TCY		2 TCY		
TRSTW	RESET Pulse Width	300		300		
TRW	$\overline{READ}$ Width	300	–	200	–	
TWA	ADR from $\overline{WRITE}$ High Hold Time	20		20		
TWC	$\overline{CS}$ High from $\overline{WRITE}$ High Hold Time	20		20		
TWD	Data from $\overline{WRITE}$ High Hold Time	30		30		
TWWS	$\overline{WRITE}$ Width	200		160		

1) Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.

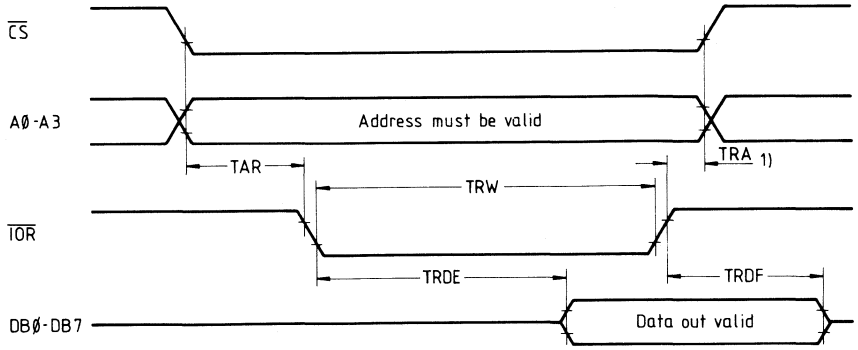
Input Waveforms for AC-Tests



Slave Mode Write Timing

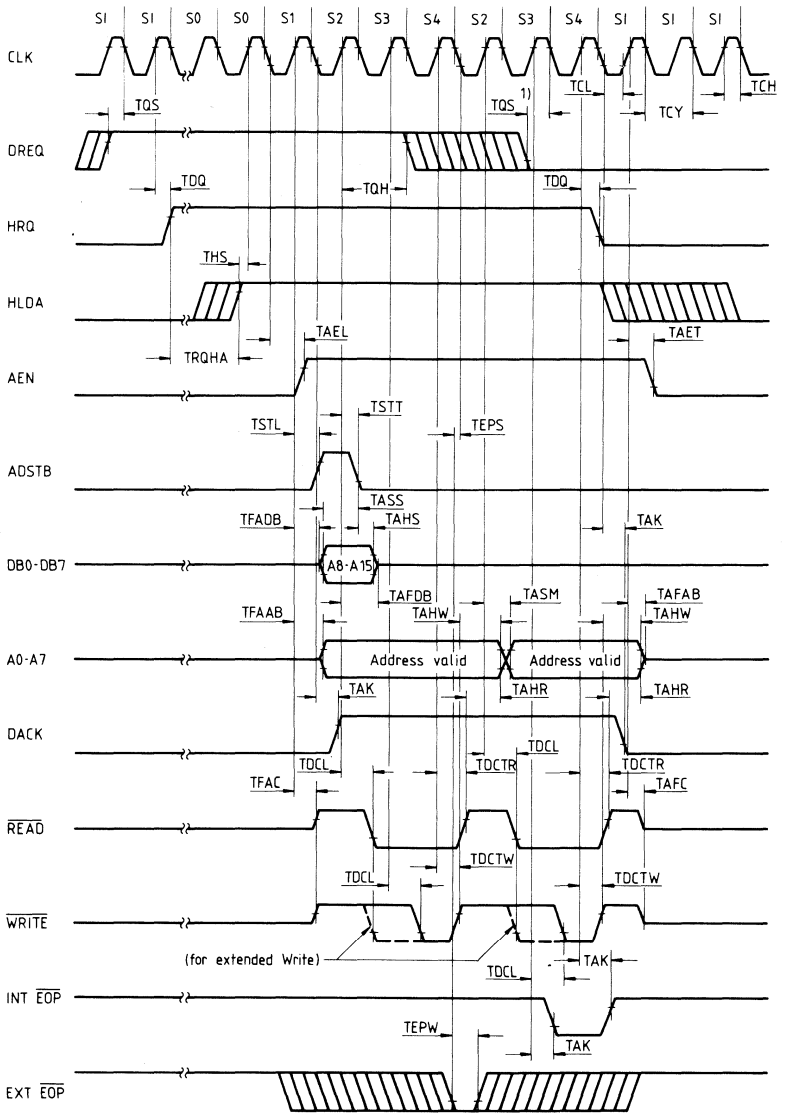


Slave Mode Read Timing



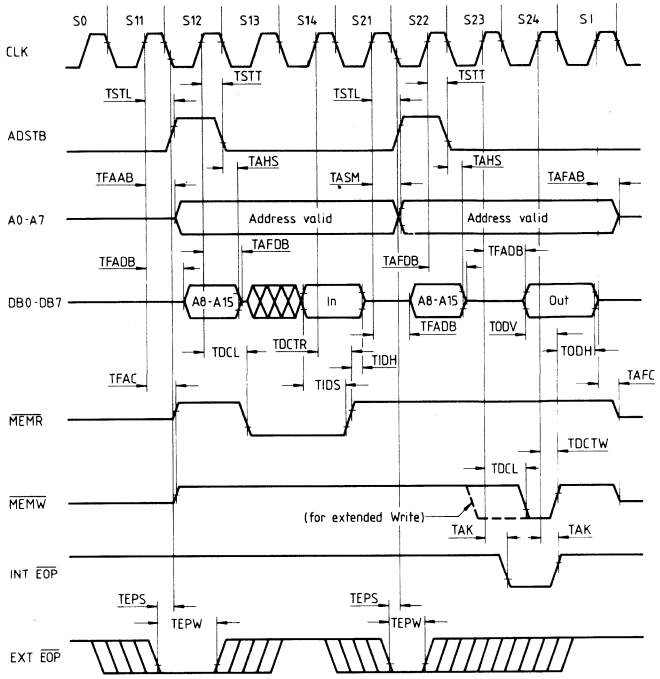
1) Successive read and/or write operation by the CPU to program or examine the controller must be timed to allow at least 600 ns for the SAB 8237A and at least 400 ns for the SAB 8237A-5, as recovery time between active read or write pulses.

DMA Transfer Timing

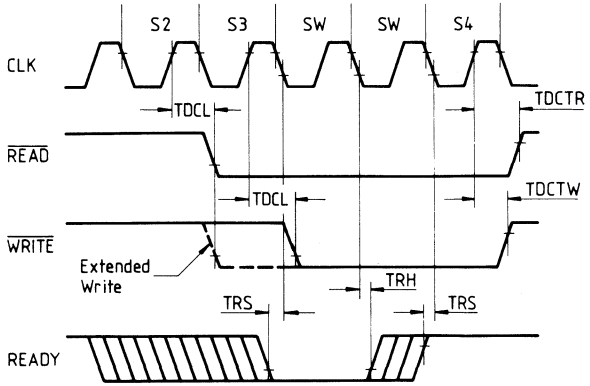


1) DREQ should be held active until DACK is returned.

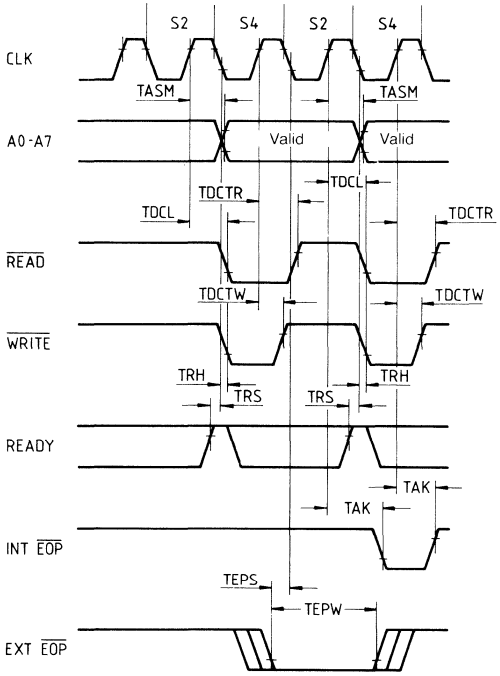
Memory-to-Memory Transfer Timing



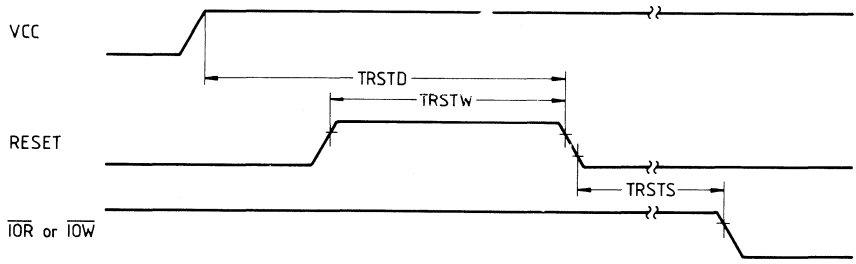
Ready Timing



Compressed Transfer Timing



Reset Timing



Ordering Information

Type	Description	Ordering code
SAB 8237A-P	Programmable DMA Controller 3 MHz (Plastic)	Q 67120-Y49
SAB 8237A-5-P	Programmable DMA Controller 5 MHz (Plastic)	Q 67120-Y72

Preliminary

SAB 82C37A-5/82C37A-8 High-Performance CMOS Programmable DMA Controller

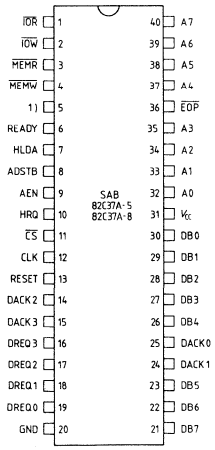
SAB 82C37A-5 5 MHz

- Four independent DMA channels
- Enable/disable control of individual DMA requests
- Memory-to-memory transfers
- Memory block initialization
- Address increment or decrement
- Independent autoinitialization of all channels
- High performance: transfers up to 2.6 Mbytes/s with 8 MHz SAB 82C37A-8

SAB 82C37A-8 8 MHz

- Directly expandable to any number of channels
- End of process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- Fully static design
- Low standby power dissipation
- Compatible with the industry standard NMOS 9517A/8237A

Pin Configuration



1) Pin always tied high

Pin Names

DB7-DB0	Data Bus (bidirectional)
$\overline{IOR}$, $\overline{IOW}$	I/O Read and Write Input/Output
$\overline{MEMR}$, $\overline{MEMW}$	Memory Read and Write Output
A0-A3	Address Input/Output
A4-A7	Adress Output
$\overline{CS}$	Chip Select Input
CLK	Clock Input
READY	Ready Input
HRQ	Hold Request Output
$\overline{HLDA}$	Hold Acknowledge Input
RESET	Reset Input
DREQ0-DREQ3	DMA Request Input
DACK0-DACK3	DMA Acknowledge Output
AEN	Address Enable Output
ADSTB	Address Strobe Output
$\overline{EOP}$	End of Process Input/Output

The SAB 82C37A Multimode Direct Memory Access (DMA) Controller is designed to improve system performance by allowing external devices to directly transfer information to or from system memory. Memory-to-memory transfer capability is also provided.
The SAB 82C37A contains four independent channels, each with a separate register set, and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to autoinitialize to its original state following an end-of-process ($\overline{EOP}$). Each channel has a full 64K address and word count capability.
The SAB 82C37A is fabricated in Siemens ACMOS technology and packaged in a 40-pin DIP. The SAB 82C37A-8 is the 8 MHz version of the 5 MHz SAB 82C37A-5. The SAB 82C37A is compatible with the industry standard 8237A/9517A DMA controllers.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{IOR}$	1	I/O	$\overline{I/O\ READ}$ I/O read is a bidirectional active-low tristate line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the SAB 82C37A to access data from a peripheral device during a DMA write transfer.
$\overline{IOW}$	2	I/O	$\overline{I/O\ WRITE}$ I/O write is a bidirectional active-low tristate line. In the idle cycle it is an input control signal used by the CPU to load information into the SAB 82C37A. In the active cycle it is an output control signal used by the SAB 82C37A to load data to a peripheral device during a DMA read transfer. Write operations by the CPU to the SAB 82C37A require a rising $\overline{IOW}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.
$\overline{MEMR}$	3	O	$\overline{MEMORY\ READ}$ The memory read signal is an active-low tristate output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.
$\overline{MEMW}$	4	O	$\overline{MEMORY\ WRITE}$ The memory write signal is an active-low tristate output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.
–	5	I	Pin 5 must be tied high.
READY	6	I	READY READY is an input used to extend the memory read and write pulses from the SAB 82C37A to accommodate slow memories or I/O peripheral devices. READY must not make transitions during its specified setup/hold time.
HLDA	7	I	HOLD ACKNOWLEDGE The active-high hold acknowledge from the CPU indicates that control of the system buses has been relinquished.
ADSTB	8	O	ADDRESS STROBE The active-high address strobe is used to strobe the upper address byte from DB0-DB7 into an external latch.
AEN	9	O	ADDRESS ENABLE Address enable is an active-high signal used to disable the system bus during DMA cycles and to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HLDA and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The SAB 82C37A automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.

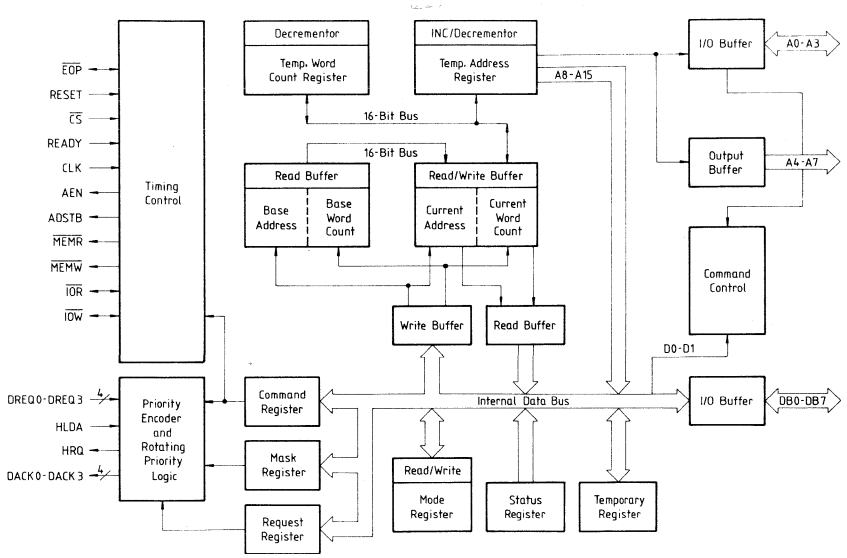
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
HRQ	10	O	HOLD REQUEST The hold request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the SAB 82C37A to issue HRQ.
$\overline{CS}$	11	I	$\overline{CHIP\ SELECT}$ Chip select is an active-low input used to select the SAB 82C37A as an I/O device during an I/O read or I/O write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the SAB 82C37A by the host CPU $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.
CLK	12	I	CLOCK This input controls the internal operations of the SAB 82C37A and its rate of data transfers. The input may be driven at up to 5 MHZ for the standard SAB 82C37A-5 and up to 8 MHz for the SAB 82C37A-8.
RESET	13	I	RESET Reset is an asynchronous active-high input which clears the command, status, request and temporary register. It also clears the first/last flipflop and sets the mask register. Following a reset, the device is in the idle cycle.
DACK0 DACK1 DACK2 DACK3	25 24 14 15	O O O O	DMA ACKNOWLEDGE The DMA acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.
DREQ0 DREQ1 DREQ2 DREQ3	19 18 17 16	I I I I	DMA REQUEST The DMA request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed priority, DREQ0 has the highest priority and and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of a DREQ signal. The polarity of DREQ is programmable. Reset initializes these lines to active high.
DB0-DB7	30-26, 23-21	I/O	DATA BUS The data bus lines are bidirectional tristate signals connected to the system data bus. The outputs are enabled during the I/O read by the host CPU, permitting the CPU to examine the contents of an address register, the status register, the temporary register or a word count register. The data bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the SAB 82C37A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the SAB 82C37A's temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the temporary register data into the destination memory location.

Pin Functions and Definitions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A0–A3	32–35	I/O	ADDRESS 0–3 The four least significant address lines are bidirectional tristate signals. During DMA idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4 bits of the output address.
A4–A7	37–40	O	ADDRESS 4–7 The four most significant address lines are tristate outputs and provide four bits of address. These lines are enabled only during DMA service.
$\overline{EOP}$	36	I/O	$\overline{END\ OF\ PROCESS}$ End of process ($\overline{EOP}$) is an active-low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's word count goes to zero, the SAB 82C37A pulses $\overline{EOP}$ low to provide the peripheral with a completion signal. $\overline{EOP}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{EOP}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the status register and to reset its request bit. If autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ always applies to the channel with an active DACK; external $\overline{EOP}$s are disregarded when DACK0-DACK3 are all inactive if the DMA is in state SI. In situations where two or more SAB 82C37A DMA controllers are cascaded, the $\overline{EOP}$ pins should be logically ORed (not wire-ORed). Because $\overline{EOP}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3 kΩ or 4.7 kΩ are recommended.
V_{CC}	31	–	POWER SUPPLY (+5 V)
GND	20	–	GROUND (0 V)

Block Diagram



Functional Description

DMA Operation
The SAB 82C37A is designed to operate in two major cycles. These are called idle and active cycles. Each device cycle is made up of a number of states. State I (SI) is the inactive state. It is entered when the SAB 82C37A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the program condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The SAB 82C37A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted before S4 by the use of the READY line on the SAB 82C37A.
Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for each complete transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23 and S24) for the write-to-memory half of the transfer.

Idle Cycle
When no channel is requesting service, the SAB 82C37A will enter the idle cycle and perform "SI" states. In this cycle the SAB 82C37A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the SAB 82C37A.

Active Cycle
When the SAB 82C37A is in the idle cycle and a channel requests a DMA service, the device will output a HRQ to the microprocessor and enter the active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode – In single transfer mode, the SAB 82C37A will make a one-byte transfer during each HRQ/HLDA handshake. When DREQ goes active, HRQ will go active. After the CPU responds by driving HRQ active, a one-byte transfer will take place. Following the transfer, HRQ will go inactive, the word count will be decremented and the address will be either incremented or decremented.

Block Transfer Mode – In block transfer mode, the SAB 82C37A will continue making transfers until a TC (caused by the word count going to zero) or an external end-of-process ($\overline{EOP}$) is encountered.

Demand Transfer Mode – In demand transfer mode the device will continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again.

Cascade Mode – This mode is used to cascade more than one SAB 82C37A together for simple system expansion. The HRQ and HLDA signals from the additional SAB 82C37A are connected to the DREQ and DACK signals of a channel of the initial SAB 82C37A.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are read, write and verify. Write transfers move data from an I/O device to the memory by activating $\overline{IOR}$ and $\overline{MEMW}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers; the SAB82C37A operates as in read or write transfers generating addresses, responding to $\overline{EOP}$, etc., however, the memory and I/O control lines remain inactive.

Memory-to-Memory – The SAB 82C37A includes a block move capability that allows blocks of data to be moved from one memory adress space to another. Channel 0 forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel 0.

Autoinitialize – By programming a bit in the mode register a channel may be set up for an autoinitialize operation. During autoinitialization, the original values of the current address and current word count registers are automatically restored from the base address and base word count registers of that channel following $\overline{EOP}$.

Extended Write – For flyby transactions late write is normally used, as this allows sufficient time for the $\overline{IOR}$ signal to get data from the peripheral onto the bus before $\overline{MEMW}$ is activated. In some systems, performance can be improved by starting the write cycle earlier.

Address Generation – In order to reduce pin count, the SAB 82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of address strobe (ADSTB) is used to load these bits from the data lines to the latch. Address enable (AEN) is used to enable the bits onto the address bus through the tristate enable control signal of the latch. The lower order address bits are output by the SAB 82C37A directly. To save time and speed transfers, the SAB 82C37A executes S1 states only when updating of A8–A15 in the latch is necessary.

Compressed Timing – In order to achieve even greater throughput where system characteristics permit, the SAB 82C37A can compress the transfer time to two clock cycles. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write.

Priority – The SAB 82C37A has two types of priority encoding available as software selectable options. The first is fixed priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel 0. The second scheme is rotating priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

Software Commands
There are two special software commands which can be executed in the program condition.
Clear first/last flipflop: This command may be issued prior to writing or reading SAB 82C37A address or word count information. This initializes the flipflop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.
Master clear: This software instruction has the same effect as the hardware reset. The command, status, request, temporary and internal first/last flipflop registers are cleared and the mask register is set.

Register Description

Current Address Register
Each channel has a 16-bit current address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the current address register during the transfer.

Current Word Count Register
Each channel has a 16-bit current word count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred.
The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated.

Base Address and Base Word Count Registers
Each channel has a pair of base address and base word count registers. These 16-bit registers store the original values of their associated current registers. During autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in bytes during DMA programming by the microprocessor.

Command Register
This 8-bit register controls the operation of the SAB 82C37A. It is programmed by the microprocessor in the program condition and is cleared by reset.

Mode Registers
Each channel has a 6-bit mode register associated with it. When the register is being written to by the microprocessor in the program condition, bits 0 and 1 determine which channel mode register is to be written to.

Request Register
The SAB 82C37A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit request register. These are nonmaskable and subject to prioritization by the priority encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a reset.

Mask Register
Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed for autoinitialize. Each bit of the 4-bit mask register may also be set or cleared separately under software control. The entire register is also set by a reset.

Status Register
The status registers may be read out of the SAB 82C37A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests.

Temporary Register
The temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the program condition.

Absolute Maximum Ratings

Ambient temperature under bias	0° to 70°C
Storage temperature	−65° to + 150°C
Supply voltage	−0.5 to + 7.0 V
Voltage on any pin with respect to ground	−0.5 to V_{CC} + 0.5 V
Power dissipation	1 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} − 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input leakage current	–	±1	µA	0 V < V_{IN} < V_{CC}
I_{OFL}	Output leakage current	–	±10	µA	0 V < V_{OUT} < V_{CC}
I_{CC}	V_{CC} supply current	–	2	mA/MHz	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open
I_{CCSB}	V_{CC} supply current – standby	–	10	µA	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open CLK = 0 MHz

Capacitance [1)]

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	f_c = 1 MHz
C_{IO}	I/O capacitance	–	20	pF	Unmeasured pins returned to GND
C_{OUT}	Output capacitance	–	15	pF	

[1)] This parameter is periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

DMA (Master) Mode

Symbol	Parameter	Limit values				Unit
		82C37A-5		82C37A-8		
		min.	max.	min.	max.	
t_{AEL}	AEN high from CLK low (S1) delay time	–	200	–	105	ns
t_{AET}	AEN low from CLK high (S1) delay time	–	130	–	80	ns
t_{AFAB}	Address active to float delay from CLK high	–	90	–	55	ns
t_{AFC}	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ float from CLK high	–	120	–	75	ns
t_{AFDB}	DB active to float delay from CLK high	–	120	–	80	ns
t_{AHR}	Address from $\overline{\text{READ}}$ high hold time	t_{CY}–100	–	t_{CY}–75	–	ns
t_{AHS}	DB from ADSTB low hold time	30	–	25	–	ns
t_{AHW}	Address from $\overline{\text{WRITE}}$ high hold time	t_{CY}–50	–	t_{CY}–50	–	ns
t_{AK}	DACK valid from CLK low delay time [1]	–	170	–	105	ns
	$\overline{\text{EOP}}$ high from CLK high delay time [2]	–	170	–	105	ns
	$\overline{\text{EOP}}$ low to CLK high delay time	–	170	–	60	ns
t_{ASM}	Address stable from CLK high	–	120	–	60	ns
t_{ASS}	DB to ADSTB low setup time	100	–	65	ns	ns
t_{CH}	CLK high time (transitions ≤ 10 ns)	80	–	55	–	ns
t_{CL}	CLK low time (transitions ≤ 10 ns)	68	–	43	–	ns
t_{CY}	CLK cycle time	200	–	125	–	ns
t_{DCL}	CLK high to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ low delay [3]	–	190	–	120	ns
t_{DCTR}	$\overline{\text{READ}}$ high from CLK high (S4) delay time[3]	–	190	–	115	ns
t_{DCTW}	$\overline{\text{WRITE}}$ high from CLK high (S4) delay time[3]	–	130	–	80	ns
t_{DQ}	HRQ valid from CLK high delay time	–	120	–	75	ns
t_{EPS}	$\overline{\text{EOP}}$ low from CLK low setup time	40	–	25	–	ns
t_{EPW}	$\overline{\text{EOP}}$ pulse width	220	–	135	–	ns
t_{FAAB}	Address float to active delay from CLK high	–	120	–	60	ns
t_{FAC}	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ active from CLK high	–	150	–	90	ns
t_{FADB}	DB float to active delay from CLK high	–	120	–	60	ns

Notes see next page.

Symbol	Parameter	Limit values				Unit
		82C37A-5		82C37A-8		
		min.	max.	min.	max.	
t_{HS}	HLDA valid to CLK high setup time	75	–	45	–	ns
t_{IDH}	Input data from $\overline{MEMR}$ high hold time	0	–	0	–	ns
t_{IDS}	Input data to $\overline{MEMR}$ high setup time	170	–	90	–	ns
t_{ODH}	Output data from $\overline{MEMW}$ high hold time	10	–	10	–	ns
t_{ODV}	Output data valid to $\overline{MEMW}$ high [4]	125	–	90	–	ns
t_{QS}	DREQ to CLK low (S1, S4) setup time [1]	0	–	0	–	ns
t_{RH}	CLK to READY low hold time	20	–	20	–	ns
t_{RS}	READY to CLK low setup time	60	–	35	–	ns
t_{STL}	ADSTB high from CLK high delay time	–	130	–	70	ns
t_{CLSL}	ADSTB low from CLK low delay time	–	150	–	70	ns
t_{SHSL}	ADSTB high time	70	–	50	–	ns
t_{QH}	DREQ from DACK valid hold time	0	–	0	–	ns
t_{RQHA}	HRQ to HLDA delay time	1	–	1	–	CLK

[1] DREQ and DACK signals may be active high or low. Timing diagrams assume the active high mode.

[2] $\overline{EOP}$ is an open-drain output. This parameter assumes the presence of a 1.6 kΩ pullup to V_{CC}.

[3] The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be t_{CY}–100 ns and for extended write will be $2t_{CY}$–100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be $2t_{CY}$–50 ns and for compressed read will be t_{CY}–50 ns.

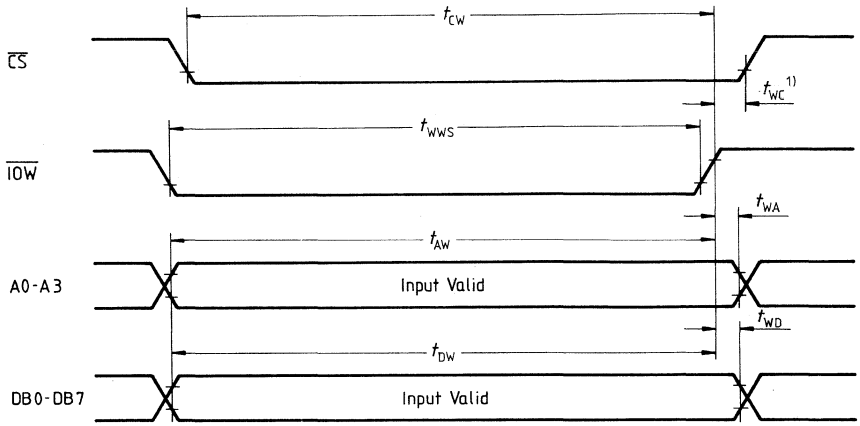
[4] If n wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by n (t_{CY}).

Peripheral (Slave) Mode

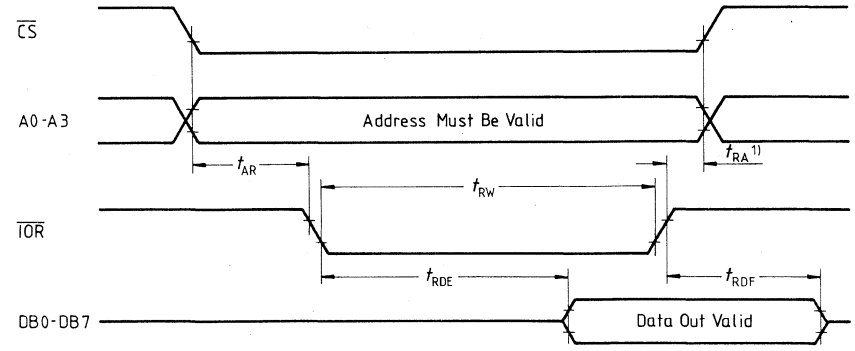
Symbol	Parameter	Limit values				Unit
		82C37A-5		82C37A-8		
		min.	max.	min.	max.	
t_{AR}	Address valid or $\overline{CS}$ low to $\overline{READ}$ low	50	–	10	–	ns
t_{AW}	Address valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{CW}	$\overline{CS}$ low to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{DW}	Data valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{RA}	Address or $\overline{CS}$ hold from $\overline{READ}$ high	0	–	0	–	ns
t_{RDE}	Data access from $\overline{READ}$ low [1]	–	140	–	120	ns
t_{RDF}	DB float delay from $\overline{READ}$ high	0	70	0	55	ns
t_{RSTD}	Power supply high to RESET low setup time	500	–	500	–	µs
t_{RSTS}	RESET to first $\overline{IOWR}$	$2\,t_{CY}$	–	$2\,t_{CY}$	–	ns
t_{RSTW}	RESET pulse width	300	–	300	–	ns
t_{RW}	$\overline{READ}$ width	200	–	155	–	ns
t_{WA}	Address from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WC}	$\overline{CS}$ high from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WD}	Data from $\overline{WRITE}$ high hold time	30	–	10	–	ns
t_{WWS}	$\overline{WRITE}$ width	160	–	100	–	ns

[1] Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.

Slave Mode Write Timing

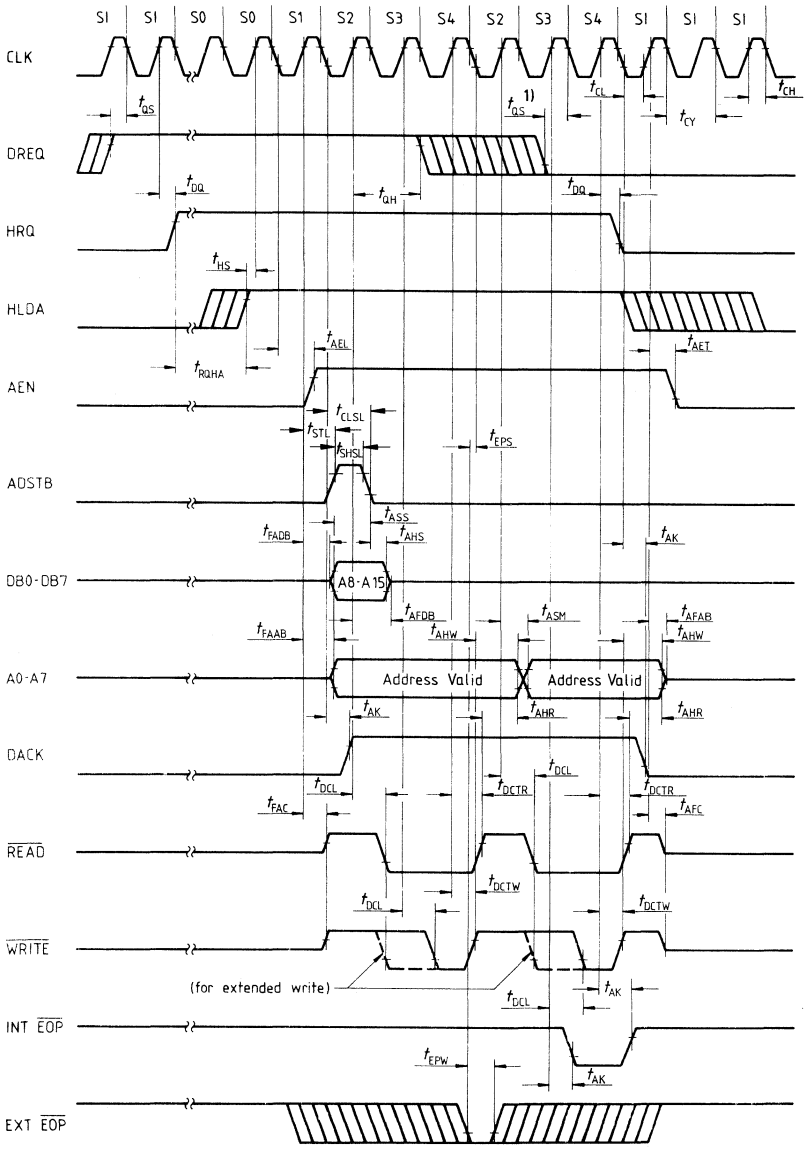


Slave Mode Read Timing



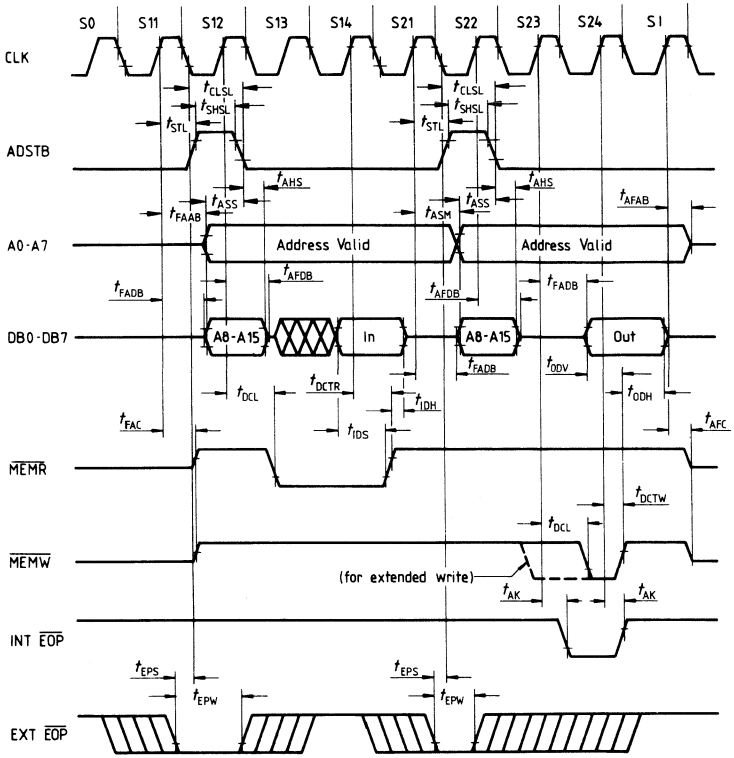
1) Successive read and/or write operation by the CPU to access the SAB 82C37A registers must meet recovery times:
   400 ns at least for the SAB 82C37A-5
   300 ns at least for the SAB 82C37A-8

DMA Transfer Timing

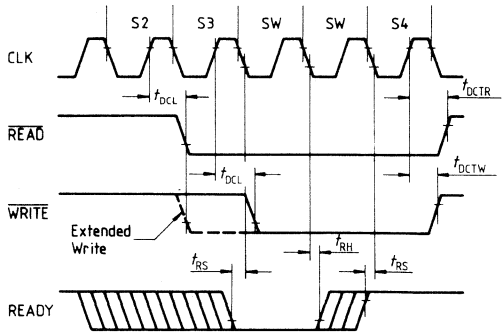


1) DREQ should be held active until DACK is returned.

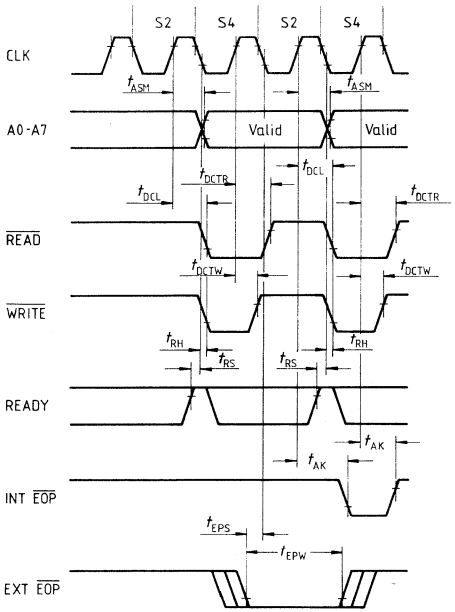
Memory-to-Memory Transfer Timing



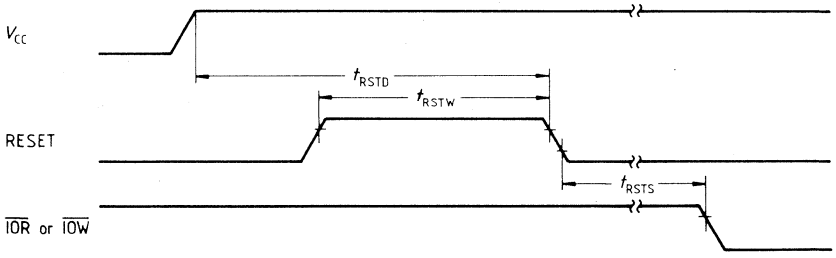
Ready Timing



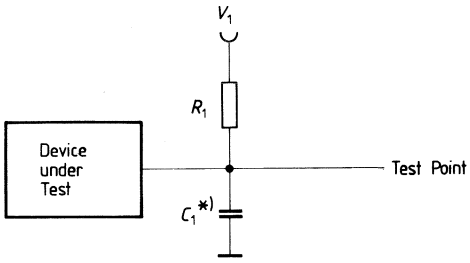
Compressed Transfer Timing



Reset Timing



AC Test Circuits

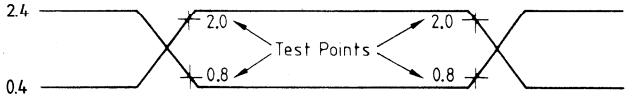


*) Includes stray and jig capacitance

Test Condition Definition

Pins	V_1	R_1	C_1
All Outputs Except $\overline{EOP}$	1.7 V	520 Ω	100 pF
$\overline{EOP}$	V_{CC}	1.6 KΩ	50 pF

Input Waveforms for AC Tests



Ordering Information

Type	Ordering code	Description
SAB 82C37A-5-P	Q 67120-P215	Programmable DMA controller 5 MHz (P-DIP-40)
SAB 82C37A-8-P	Q 67120-P239	Programmable DMA controller 8 MHz (P-DIP-40)

Preliminary

SAB 82C37B-5/82C37B-8 High-Performance CMOS Programmable DMA Controller

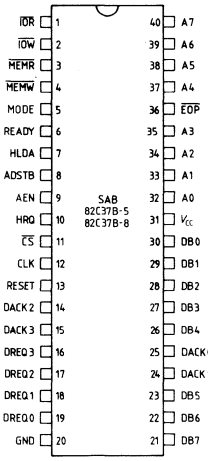
SAB 82C37B-5 5 MHz

- Fully upward-compatible to SAB 82C37A (CMOS) and SAB 8237A (NMOS)
- Two basic operating modes
  Normal mode: 16-bit registers
  Superset mode: 24-bit registers
- Supports 24-bit address and count valves
- Four independent DMA channels
- Address increment or decrement by 1 or 2 (byte or word transfers)

SAB 82C37B-8 8 MHz

- High performance: transfers up to 8 Mbytes/s with 8 MHz SAB 82C37B-8
- Directly expandable to any number of channels
- Independent polarity control for DREQ and DACK signals
- Fully static design
- Low standby power dissipation

Pin Configuration



Pin Names

DB7-DB0	Data Bus (bidirectional)
$\overline{IOR}$, $\overline{IOW}$	I/O Read and Write Input/Output
$\overline{MEMR}$, $\overline{MEMW}$	Memory Read and Write Output
A0-A3	Address Input/Output
A4-A7	Adress Output
$\overline{CS}$	Chip Select Input
CLK	Clock Input
READY	Ready Input
HRQ	Hold Request Output
$\overline{HLDA}$	Hold Acknowledge Input
RESET	Reset Input
DREQ0-DREQ3	DMA Request Inputs
DACK0-DACK3	DMA Acknowledge Outputs
AEN	Address Enable Output
ADSTB	Address Strobe Output
$\overline{EOP}$	End of Process Input/Output
MODE	Mode Select Input

The SAB 82C37B Multimode Direct Memory Access (DMA) Controller improves the system performance by allowing external devices to directly transfer information to or from system memory. A memory-to-memory transfer capability is also provided. The SAB 82C37B may operate in two modes. The normal mode provides direct compatibility to the industry standard 8237A/9517A DMA controllers. In the superset mode, the SAB 82C37B contains 24-bit wide address and count registers for each channel.
The four independent channels with their own register set may be cascaded by additional DMA controller chips.
The SAB 82C37B is fabricated in Siemens ACMOS technology and packaged in a 40-pin DIP. The SAB 82C37B-8 is the 8 MHz version of the 5 MHz SAB 82C37B-5.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{IOR}$	1	I/O	$\overline{I/O\ READ}$ I/O read is a bidirectional active-low tristate line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the SAB 82C37A to access data from a peripheral device during a DMA write transfer.
$\overline{IOW}$	2	I/O	$\overline{I/O\ WRITE}$ I/O write is a bidirectional active-low tristate line. In the idle cycle it is an input control signal used by the CPU to load information into the SAB 82C37B. In the active cycle it is an output control signal used by the SAB 82C37B to load data to a peripheral device during a DMA read transfer. Write operations by the CPU to the SAB 82C37B require a rising $\overline{IOW}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.
$\overline{MEMR}$	3	O	$\overline{MEMORY\ READ}$ The memory read signal is an active-low tristate output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.
$\overline{MEMW}$	4	O	$\overline{MEMORY\ WRITE}$ The memory write signal is an active-low tristate output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.
MODE	5	I	MODE MODE selects the SAB 82C37B operating mode. If MODE = high, normal mode with 16-bit address and count registers is selected. MODE = low selects the superset mode with 24-bit address and count registers and word transfer capability. MODE is a strapping pin and must not be changed dynamically during controller operation.
READY	6	I	READY READY is an input used to extend the memory read and write pulses from the SAB 82C37B to accommodate slow memories or I/O peripheral devices. READY must not make transitions during its specified setup/hold time and is ignored in verify transfer mode.
HLDA	7	I	HOLD ACKNOWLEDGE The active-high hold acknowledge from the CPU indicates that control of the system buses has been relinquished.
ADSTB	8	O	ADDRESS STROBE The active-high address strobe is used to strobe the addresses A8-A15 at DB0-DB7 into an external latch. In the superset mode (MODE = low), ADSTB is also used to strobe A16 to A23 at A0-A7 into an external latch. During block operations, ADSTB will only be issued when the upper addresses A8-A23 must be updated, thus speeding operation by eliminating S1 states.

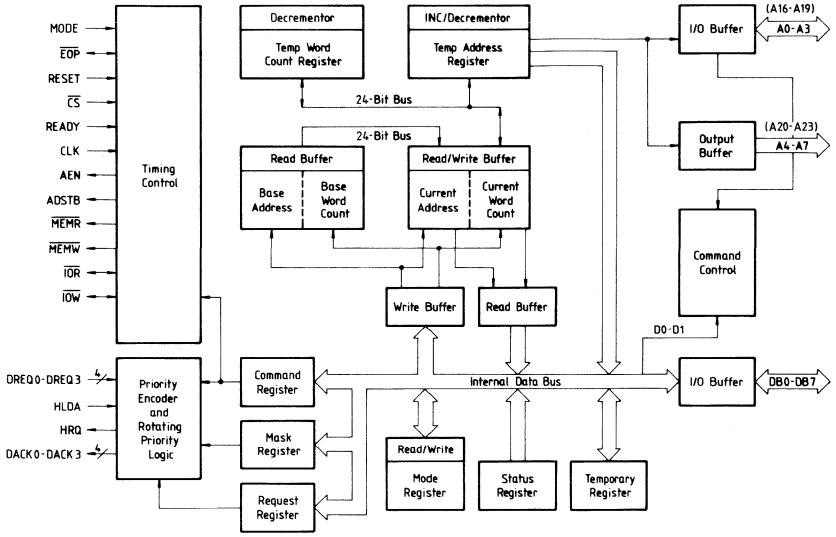
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
AEN	9	O	ADDRESS ENABLE Address enable is an active-high signal used to disable the system bus during DMA cycles and to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HLDA and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The SAB 82C37B automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.
HRQ	10	O	HOLD REQUEST The hold request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the SAB 82C37B to issue HRQ.
$\overline{CS}$	11	I	$\overline{CHIP\ SELECT}$ Chip select is an active-low input used to select the SAB 82C37B as an I/O device during an I/O read or I/O write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the SAB 82C37B by the host CPU $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.
CLK	12	I	CLOCK This input controls the internal operations of the SAB 82C37B and its rate of data transfers. The input may be driven from DC up to 5 MHz for the SAB 82C37B-5 and up to 8 MHz for the SAB 82C37B-8. The clock may be stopped any time for standby operation, even in the middle of a bus operation.
RESET	13	I	RESET Reset is an asynchronous active-high input which clears the command, status, request and temporary register. It also clears the first/last flipflop (normal mode) or the byte pointer counter (superset mode) and sets the mask register. Following a reset the device is performing idle cycles.
DACK0 DACK1 DACK2 DACK3	25 24 14 15	O O O O	DMA ACKNOWLEDGE The DMA acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.
DREQ0 DREQ1 DREQ2 DREQ3	19 18 17 16	I I I I	DMA REQUEST The DMA request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of a DREQ signal. The polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled high or low (inactive) and the corresponding mask bit should be set.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
DB0-DB7	30-26, 23-21	I/O	DATA BUS The data bus lines are bidirectional tristate signals connected to the system data bus. The outputs are enabled during the I/O read by the host CPU, permitting the CPU to examine the contents of a register. The data bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the SAB 82C37B control registers. During DMA cycles the addresses A8-A15 are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the SAB 82C37B's temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the temporary register data into the destination memory location.
A0–A3	32–35	I/O	ADDRESS 0–3 The four least significant address lines are bidirectional tristate signals. During DMA idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the A0-A3 output addresses, and in the superset mode A16 to A19.
A4–A7	37–40	O	ADDRESS 4–7 The four most significant address lines are tristate outputs and provide A4-A7 addresses. In the superset mode A20-A23 are available at these lines during S1 states. These lines are enabled only during the DMA service.
$\overline{EOP}$	36	I/O	$\overline{END\ OF\ PROCESS}$ End of process ($\overline{EOP}$) is an active-low bidirectional signal. Information concerning the completion of DMA services. is available at the bidirectional $\overline{EOP}$ pin. The SAB 82C37B allows an external signal to terminate an active DMA service by pulling the $\overline{EOP}$ pin low. A pulse is generated by the SAB 82C37B when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. The $\overline{EOP}$ pin is driven by an open-drain transistor on-chip, and requires an external pullup resistor. When an $\overline{EOP}$ pulse occurs, whether internally or externally generated, the SAB 82C37B will terminate the service, and if autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for autoinitialize. In that case, the mask bit remains clear.
V_{CC}	31	–	POWER SUPPLY (+5 V)
GND	20	–	GROUND (0 V)

Block Diagram



Functional Description

The SAB 82C37B direct memory access controller is designed to improve the data transfer rate in systems which must transfer data from an I/O device to memory, or move a block memory to an I/O device. It will also perform memory-to-memory block moves, or fill a block of memory with data from a single location. Operating modes are provided to handle single byte transfers as well as discontinuous data streams.
The DMA controller is a state-driven address and control signal generator, which permits data to be transferred directly from an I/O device to memory or vice versa without ever being stored in a temporary register. This can greatly increase the data transfer rate for sequential operations, compared with processor move or repeated string instructions. Memory-to-memory operations require temporary internal storage of the data byte between generation of the source and destination addresses, so memory-to-memory transfers take place at less than half the rate I/O operations, but still much faster than with central processor techniques.

DMA Operation

In a system, the SAB 82C37B address and control outputs and data bus pins are basically connected in parallel with the systems buses. External latches are required for the upper address lines. While inactive, the controller's outputs are in a high-impedance state. When activated by a DMA request and bus control is relinquished by the host, the SAB 82C37B drives the buses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the command, mode, address, and word count registers.

Once initiated, a block DMA transfer will proceed as the controller outputs the data address, simultaneous $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ pulses, and selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the word count register underflows, or an external $\overline{\text{EOP}}$ is applied.

The DMA controller operates in two major cycles, active and idle. After being programmed, the controller is normally idle until a DMA request occurs on an unmasked channel, or a software request is given. The SAB 82C37B will then request control of the system buses and enter the active cycle.

The SAB 82C37B can assume seven separate states, each composed of one full clock period. State I (SI) is the idle state. It is entered when the SAB 82C37B has no valid DMA requests pending, at the end of a transfer sequence, or when a reset or master clear has occurred. While in SI, the DMA controller is inactive but may be in the program condition (being programmed by the processor).

State 0 (S0) is the first state of a DMA service. The SAB 82C37B has requested a hold but the processor has not yet returned an acknowledge. The SAB 82C37B may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the ready line on the SAB 82C37B.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14 are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the SAB 82C37B will enter the idle cycle and perform "SI" states. In this cycle, the SAB 82C37B samples the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored. The device will respond to $\overline{\text{CS}}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the SAB 82C37B. When $\overline{\text{CS}}$ is low and HLDA is low, the SAB 82C37B enters the program condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers.

Active Cycle

When the SAB 82C37B is in the idle cycle, and a software request or an unmasked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode – In single transfer mode, the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a terminal count bit in the status register is set, an $\overline{EOP}$ pulse is generated, and the channel will autoinitialize if this option has been selected. If not programmed to autoinitialize, the mask bit will be set, along with the TC bit and $\overline{EOP}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, unless a higher priority channel takes over.

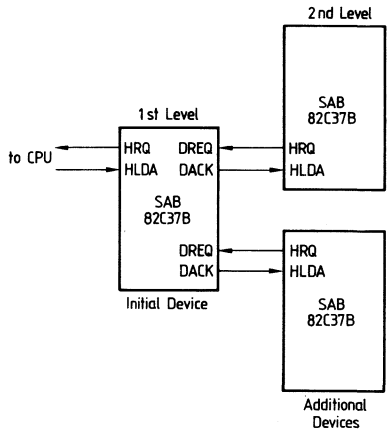
Block Transfer Mode – In block transfer mode, the device is activated by DREQ or software request and continues making transfers during the service until a TC, caused by word count going to FFFFH, or an external end-of-process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, an autoinitialization will occur at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode – In demand transfer mode the device continues making transfers until a TC or external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfers may continue until the I/O device has exhausted its data capacitiy. Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an $\overline{EOP}$ can cause an autoinitialization at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode – This mode is used to cascade more than one SAB 82C37B for simple system expansion. The HRQ and HLDA signals from the additional SAB 82C37B are connected to the DREQ and DACK signals respectively of a channel for the initial SAB 82C37B. This allows the DMA request of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests.

The following figure shows two additional devices cascaded with an initial device using two of the previous channels.

Cascaded SAB 82C37B Devices



When programming cascaded controllers, start with the first level (closest to the microprocessor). After reset, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. Also, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are read, write and verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$.

Verify transfers are pseudo-transfers. The SAB 82C37B operates as in read or write transfers generating addresses and responding to $\overline{EOP}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not permitted for memory-to-memory operation. Ready is ignored during verify transfers.

Autoinitialize – By programming a bit in the mode register, a channel may be set up as an autoinitialize channel. During autoinitialization, the original values of the current address and current word count registers are automatically restored from the base address and base word count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize. Following autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request is made.

Memory-to-Memory – To perform block moves of data from one memory address space to another with minimum of program effort and time, the SAB 82C37B includes a memory-to-memory transfer feature. Programming a bit in the command register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The SAB 82C37B requests a DMA service in the normal manner. After HLDA is true, the device, using four-state transfers in block transfer mode, reads data from the memory. The channel 0 current address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the SAB 82C37B internal temporary register. Another four-state transfer moves the data to memory using the address in channel one's current address register and incrementing or decrementing it in the normal manner. The channel 1 current word count is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output terminating the service. Channel 0 word count decrementing to FFFFH will not set the channel 0 TC bit in the status register or generate an $\overline{EOP}$ in this mode. It will cause an autoinitialization of channel 0, if that option has been selected.

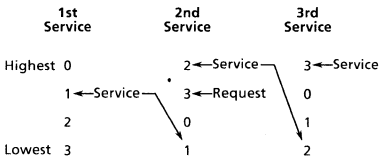
If full autoinitialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set equal before the transfer begins.

In memory-to-memory mode, channel 0 may be programmed to retain the same address for all transfers. This allows a single byte to be written to a block of memory. This channel 0 address hold feature is selected by bit 1 in the command register.

Priority – The SAB 82C37B has two types of priority encoding available as software selectable options. The first is fixed priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interferring with the service until it is completed.

The second scheme is rotating priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. The next lower channel from the channel serviced has highest priority on the following request: Priority rotates every time control of the system buses is returned to the processor.

Rotating Priority



Compressed Timing – In order to achieve even greater throughput where system characteristics permit, the SAB 82C37B can compress the transfer time to two clock cycles. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. $\overline{EOP}$ will be output in S2 if compressed timing is selected. Compressed timing is not allowed for memory-to-memory transfers.

Basic Operating Modes – The SAB 82C37B may work in two basic operating modes: the normal mode and the superset mode. In the normal mode, the SAB 82C37B is compatible with its NMOS SAB 8237A predecessor and provides 16-bit wide address and count registers. In the superset mode address and count registers have a width of 24 bits. In this mode the SAB 82C37B directly supports the full addressing capabilities of the SAB 8086/8088, SAB 80186/80188 and SAB 80286 microprocessor families.

Two additional features ara available in the superset mode. The address increment/decrement of the address registers can be programmed to be one or two. So byte or word transfers may be selected during a DMA operation. Furthermore, the incrementing/decrementing of the address bits A16–A23 may be disabled. In this case, addresses will wrap around within a 64K page and A16–A23 work like a page register.

Thus with the capabilities of the superset mode, external page registers are no longer required for each DMA channel to get a DMA address greater than 16 bits. Instead of external page registers, the SAB 82C37B in superset mode generates the upper address information A16–A23 for DMA cycles needing one external address latch, which may be used by each DMA channel.

The two basic operating modes are selected by the MODE pin. If MODE is tied to V_{CC}, normal mode is selected. The superset mode is selected by connecting the MODE pin to GND. MODE must not be changed dynamically during controller operation.

Address Generation – In order to reduce pin count, the SAB 82C37B multiplexes addresses on data lines and address lines. State S1 is used to output the higher address bits to external address latches. A8–A15 are output at the data bus lines DB0–7. In superset mode additionally A16–A23 appear at the address lines A0–A7. The falling edge of the address strobe (ADSTB) is used to strobe this information into latches. AEN (address enable) is used to enable these latches to drive the address bus. The lower address bits are output by the SAB 82C37B directly (for more details see timing diagrams).

During block and demand transfer mode service, which includes multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the SAB 82C37B executes S1 states only when an updating of A8–A23 in the latch is necessary.

Programming

The SAB 82C37B will accept programming from the host processor anytime that HLDA is inactive, and at least one rising clock edge has occurred after HLDA went low. It is the responsibility of the host processor to assure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the SAB 82C37B is being programmed.

Such problems can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled/unmasked.

Due to the number and size of the internal registers, an internal flipflop (normal mode) or a modulo-3 register pointer (superset mode) are used to generate internally additional address bits for register addressing. This flipflop or byte counter determines which byte of the 16/24-bit address and word count registers is accessed. Flipflop and byte counter are reset through RESET or by software.

Register Description

Current Address Register

Each channel has a 16/24-bit current address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the values of the address are stored in the current address register during the transfer. This register is written or read by the microprocessor in successive bytes. It may also be reinitialized by an autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$.

Current Word Count Register

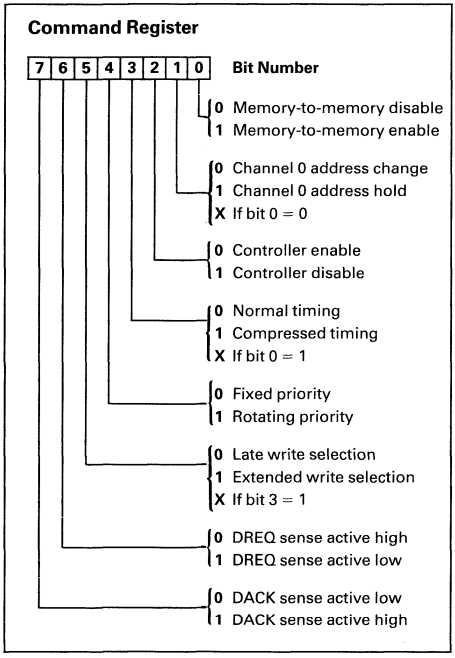
Each channel has a 16/24-bit current word count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the current word count register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. When the value in the register goes from 0 to (FF)FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the program condition. Following the end of a DMA service it may also be reinitialized by an autoinitialization back to its original value. Autoinitialization can occur only when an $\overline{EOP}$ occurs. If it is not autoinitialized, this register will have a count of (FF)FFFFH after TC.

Base Address and Base Word Count Registers

Each channel has a pair of base address and base word count registers. These 16/24-bit registers store the original value of their associated current registers. During autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in bytes in the program condition by the microprocessor. These registers cannot be read by the microprocessor.

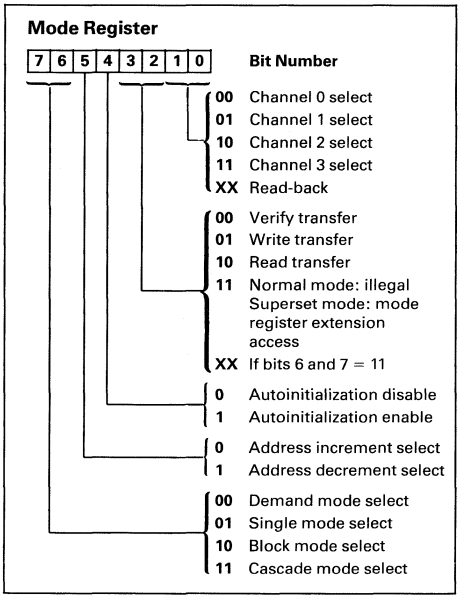
Command Register

This 8-bit register controls the operation of the SAB 82C37B. It is programmed by the microprocessor and is cleared by reset or a master clear instruction.

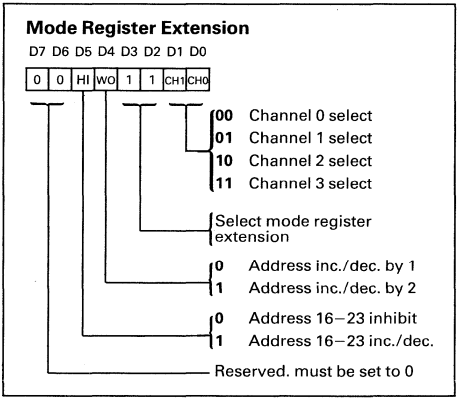


Mode Register

Each channel has a 6-bit mode register associated with it. When the register is being written to by the microprocessor in the program condition, bits 0 and 1 determine which channel mode register is to be written to.



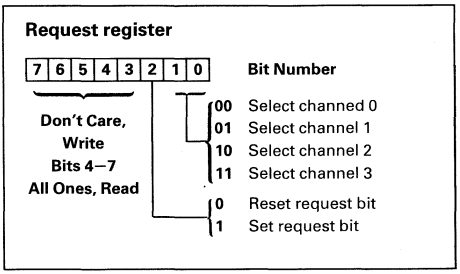
If the bits 2 and 3 of the mode register are set during writing, the mode register extension register will be accessed (only in superset mode!). In normal mode, no mode register extension is available. The mode register extension is used to program the special features of the SAB 82C37B superset mode.



When the processor reads back the mode register, bits 2 to 7 contain the information which was written into the mode register bits 2 to 7. Bit 0 contains the value of W0 of the mode register extension and bit 1 shows the value of HI. In normal mode the value of these two bits is undefined.

Request Register

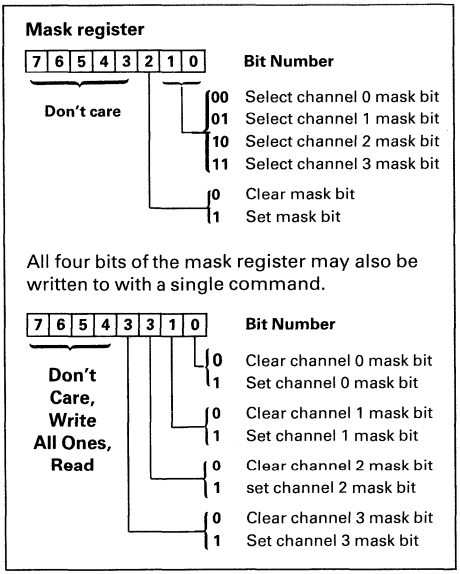
The SAB 82C37B can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit request register. These are non-maskable and subject to prioritization by the priority encoder network. Each register bit is set or reset separately under software control. The entire register is cleared by a reset. A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the request register, bits 4–7 will always read as ones, and bits 0–3 will display the request bits of channels 0–3 respectively.



Mask Register

Each channel has associated with it a mask bit which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to autoinitialize. Each bit of the 4-bit mask register may also be set or cleared separately or simultaneously under software control. The entire register is also set by a reset or master clear.

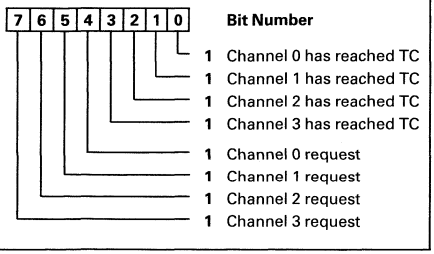
When reading the mask register, bits 4–7 will always read as logical ones, and bits 0–3 will display the mask bits of channel 0–3, respectively. The 4 bits of the mask register may be cleared simultaneously by using the clear mask register command (see software commands section).



Status Register

The status register contains information about the status of the SAB 82C37B. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0–3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. Status bits are cleared upon reset, master clear, and on each status read. Bits 4–7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user-defined service priority.

Status Register



Temporary Register
The temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor. The temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a reset or master clear.

Software Commands
There are special software commands which can be executed by reading or writing to the SAB 82C37B. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. On read-type commands, the data value is not guaranteed. These commands are:

Clear Register Pointer – This command is executed prior to writing or reading a new address or word count information to the SAB 82C37B. In normal mode, this command initializes a byte pointer flipflop to 0 so that subsequent accesses to register contents start by addressing the low byte first. In the superset mode, the modulo-3 register pointer is reset by this command. Thus the following first byte access to address or count registers starts with the lowest byte. The next byte will be the middle byte followed by the highest byte of the 24-bit registers. After this the lowest byte will be addressed again with the next access.

Set Register Pointer – In normal mode, this command will set the register pointer flipflop to select the high byte first on read or write operations to address and count registers. In the superset mode, this command sets the byte pointer to the medium byte. The byte addressed next will be the highest byte.

Master Clear – This software instruction has the same effect as the hardware reset. The command, status, request, and temporary registers, and internal byte pointer and mode register counter are cleared and the mask register is set. The SAB 82C37B will enter the idle cycle.

Software Command Codes and Register Codes

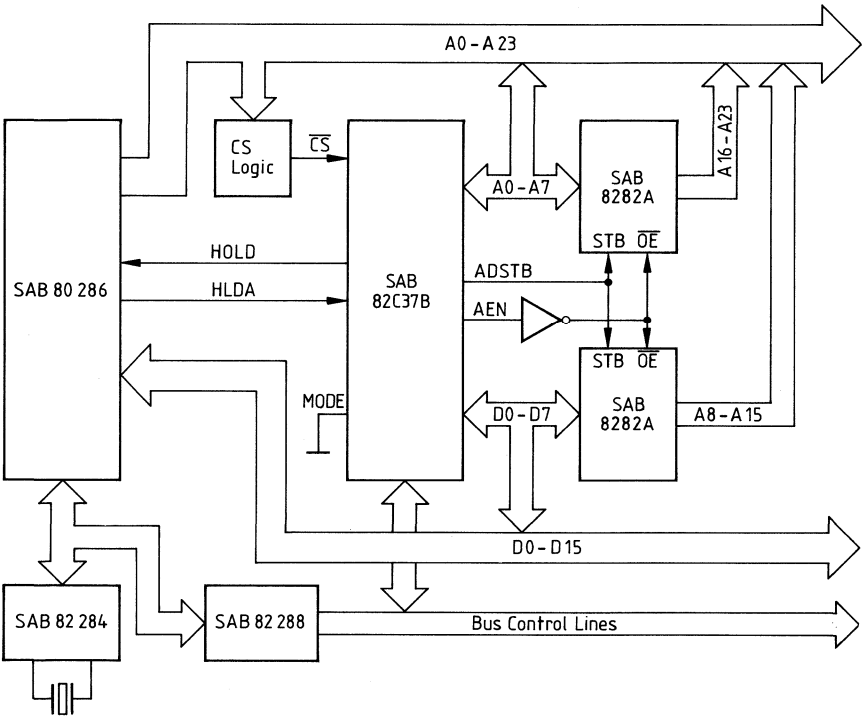
Operation	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer Flipflop	1	1	0	0	0	1
Clear Byte Pointer Flipflop	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Register Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

Clear Mask Register – This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter – Since only one address location is available for reading the mode registers, an internal two-bit counter has been included to select mode registers during read operations. To read the mode registers, first execute the clear mode register counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last.

External EOP Operation
The $\overline{EOP}$ pin is a bidirectional, open-drain pin which may be driven by external signals to terminate DMA operation. It is important to note that the SAB 82C37B will not accept external $\overline{EOP}$ signals when it is an SI (idle) state. The controller must be active to latch EXT $\overline{EOP}$. Once latched, the EXT $\overline{EOP}$ will be acted upon during the next S2 state, unless the SAB 82C37B enters an idle state first. In the latter case, the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses occurring between active DMA transfers in demand mode will not be recognized, since the SAB 82C37B is in an SI state.

Typical SAB 80286/82C37B System Configuration



Absolute Maximum Ratings

Ambient temperature under bias	0° to 70°C
Storage temperature	−65° to + 150°C
Supply voltage	−0.5 to + 7.0 V
Voltage on any pin with respect to ground	−0.5 to V_{CC} + 0.5 V
Power dissipation	1 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} − 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input load current	–	±1	µA	0 V < V_{IN} < V_{CC}
I_{OFL}	Output leakage current	–	±10	µA	0 V < V_{OUT} < V_{CC}
I_{CC}	V_{CC} supply current	–	2	mA/MHz	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open
I_{CCSB}	V_{CC} supply current – standby	–	10	µA	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open CLK = 0 MHz

Capacitance [1)]

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	f_c = 1 MHz
C_{IO}	I/O capacitance	–	20	pF	Unmeasured pins returned to GND
C_{OUT}	Output capacitance	–	15	pF	

[1)] This parameter is periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

DMA (Master) Mode

Symbol	Parameter	Limit values				Unit
		82C37B-5		82C37B-8		
		min.	max.	min.	max.	
t_{AEL}	AEN high from CLK low (S1) delay time	–	200	–	105	ns
t_{AET}	AEN low from CLK high (S1) delay time	–	130	–	80	ns
t_{AFAB}	Address active to float delay from CLK high	–	90	–	55	ns
t_{AFC}	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ float from CLK high	–	120	–	75	ns
t_{AFDB}	DB/Address active to float delay from CLK high	–	120	–	80	ns
t_{AHR}	Address from $\overline{\text{READ}}$ high hold time	t_{CY}–100	–	t_{CY}–75	–	ns
t_{AHS}	DB from ADSTB low hold time	30	–	25	–	ns
t_{AHW}	Address from $\overline{\text{WRITE}}$ high hold time	t_{CY}–50	–	t_{CY}–50	–	ns
t_{AK}	DACK valid from CLK low delay time [1]	–	170	–	105	ns
	$\overline{\text{EOP}}$ high from CLK high delay time [2]	–	170	–	105	ns
	$\overline{\text{EOP}}$ low to CLK high delay time	–	170	–	60	ns
t_{ASM}	Address stable from CLK high	–	120	–	60	ns
t_{ASS}	DB to ADSTB low setup time	100	–	65	–	ns
t_{CH}	CLK high time (transitions ≤ 10 ns)	80	–	55	–	ns
t_{CL}	CLK low time (transitions ≤ 10 ns)	68	–	43	–	ns
t_{CY}	CLK cycle time	200	–	125	–	ns
t_{DCL}	CLK high to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ low delay [3]	–	190	–	120	ns
t_{DCTR}	$\overline{\text{READ}}$ high from CLK high (S4) delay time [3]	–	190	–	115	ns
t_{DCTW}	$\overline{\text{WRITE}}$ high from CLK high (S4) delay time [3]	–	130	–	80	ns
t_{DQ}	HRQ valid from CLK high delay time	–	120	–	75	ns
t_{EPS}	$\overline{\text{EOP}}$ low from CLK low setup time	40	–	25	–	ns
t_{EPW}	$\overline{\text{EOP}}$ pulse width	220	–	135	–	ns
t_{FAAB}	Address float to active delay from CLK high	–	120	–	60	ns
t_{FAC}	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ active from CLK high	–	150	–	90	ns
t_{FADB}	DB float to active delay from CLK high	–	120	–	60	ns

Notes see next page.

Symbol	Parameter	Limit values				Unit
		82C37B-5		82C37B-8		
		min.	max.	min.	max.	
t_{HS}	HLDA valid to CLK high setup time	75	–	45	–	ns
t_{IDH}	Input data from $\overline{MEMR}$ high hold time	0	–	0	–	ns
t_{IDS}	Input data to $\overline{MEMR}$ high setup time	170	–	90	–	ns
t_{ODH}	Output data from $\overline{MEMW}$ high hold time	10	–	10	–	ns
t_{ODV}	Output data valid to $\overline{MEMW}$ high [4]	125	–	90	–	ns
t_{DS}	DREQ to CLK low (S1, S4) setup time [1]	0	–	0	–	ns
t_{RH}	CLK to READY low hold time	20	–	20	–	ns
t_{RS}	READY to CLK low setup time	60	–	35	–	ns
t_{STL}	ADSTB high from CLK high delay time	–	130	–	70	ns
t_{CLSL}	ADSTB low from CLK low delay time	–	150	–	120	ns
t_{SHSL}	ADSTB high time	70	–	50	–	ns
t_{QH}	DREQ from DACK valid hold time	0	–	0	–	ns
t_{RQHA}	HRQ to HLDA delay time	1	–	1	–	CLK

[1] DREQ and DACK signals may be active high or low. Timing diagrams assume the active high mode.

[2] $\overline{EOP}$ is an open-collector output. This parameter assumes the presence of a 1.6 kΩ pullup to V_{CC}.

[3] The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be t_{CY}–100 ns and for extended write will be $2t_{CY}$–100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be $2t_{CY}$–50 ns and for compressed read will be t_{CY}–50 ns.

[4] If n wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by n (t_{CY}).

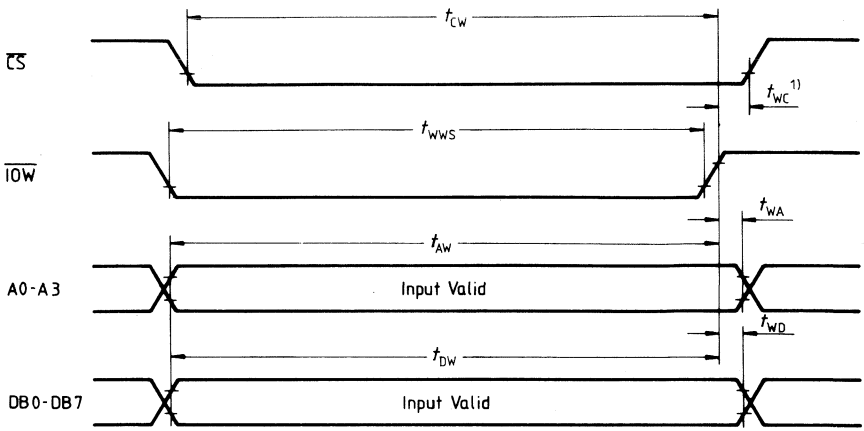
Peripheral (Slave) Mode

Symbol	Parameter	Limit values				Unit
		82C37B-5		82C37B-8		
		min.	max.	min.	max.	
t_{AR}	Address valid or $\overline{CS}$ low to $\overline{READ}$ low	50	–	10	–	ns
t_{AW}	Address valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{CW}	$\overline{CS}$ low to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{DW}	Data valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{RA}	Address or $\overline{CS}$ hold from $\overline{READ}$ high	0	–	0	–	ns
t_{RDE}	Data access from $\overline{READ}$ low [1]	–	140	–	120	ns
t_{RDF}	DB float delay from $\overline{READ}$ high	0	70	0	55	ns
t_{RSTD}	Power supply high to RESET low setup time	500	–	500	–	µs
t_{RSTS}	RESET to first $\overline{IOWR}$	2 t_{CY}	–	2 t_{CY}	–	ns
t_{RSTW}	RESET pulse width	300	–	300	–	ns
t_{RW}	$\overline{READ}$ width	200	–	155	–	ns
t_{WA}	Address from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WC}	$\overline{CS}$ high from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WD}	Data from $\overline{WRITE}$ high hold time	30	–	10	–	ns
t_{WWS}	$\overline{WRITE}$ width	160	–	100	–	ns

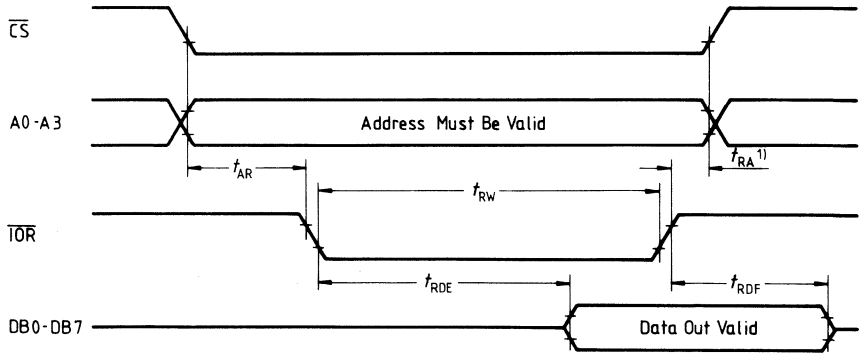
[1] Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.

Waveforms

Slave Mode Write Timing

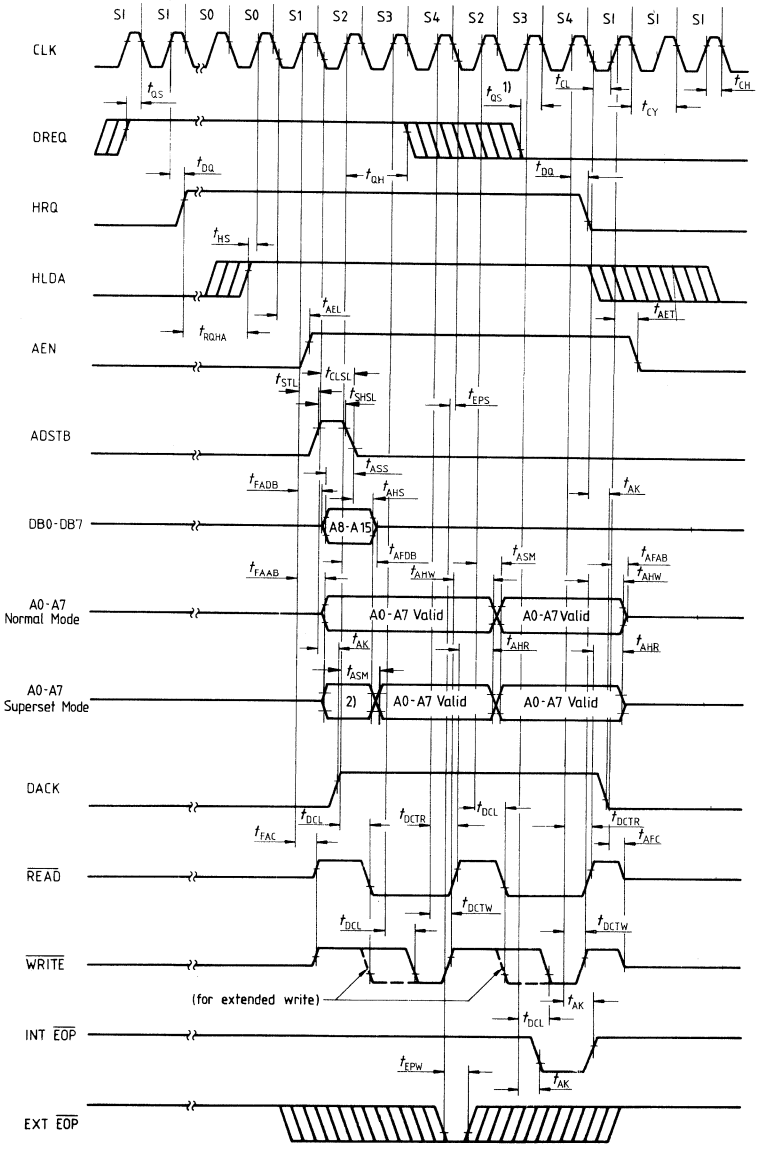


Slave Mode Read Timing



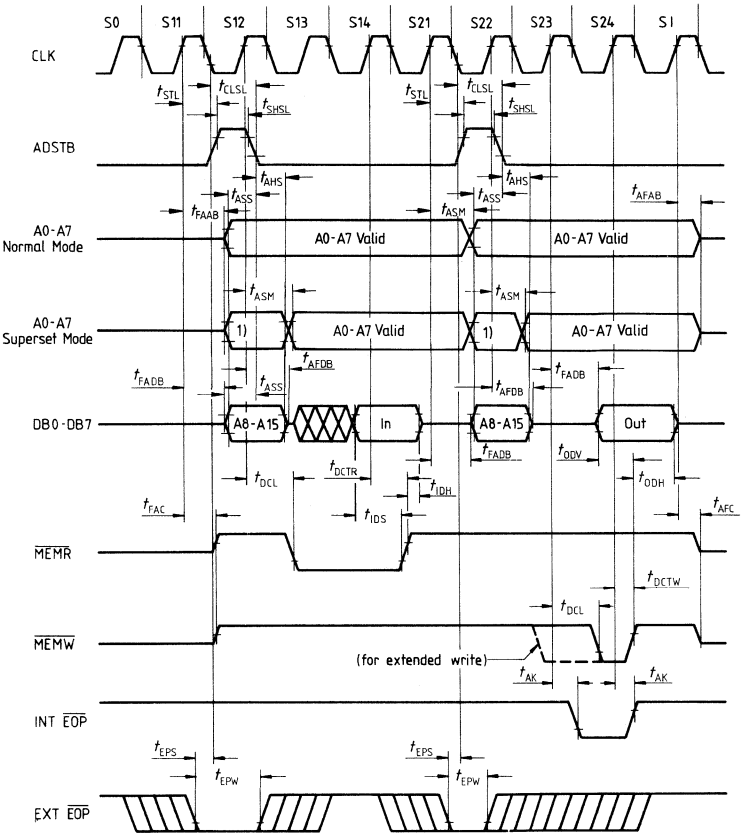
1) Successive read or write operations by the CPU to access the SAB 82C37B registers must meet recovery times:
   400 ns at least for the SAB 82C37B-5
   300 ns at least for the SAB 82C37B-8

DMA Transfer Timing



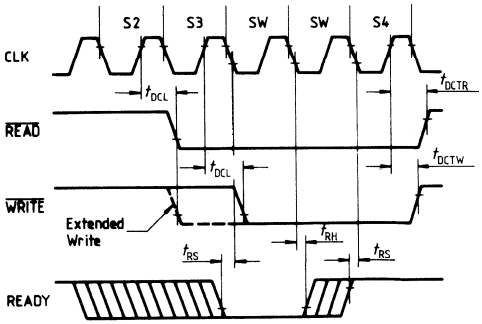
1) DREQ should be held active until DACK is returned.
2) A16-A23 valid

Memory-to-Memory Transfer Timing

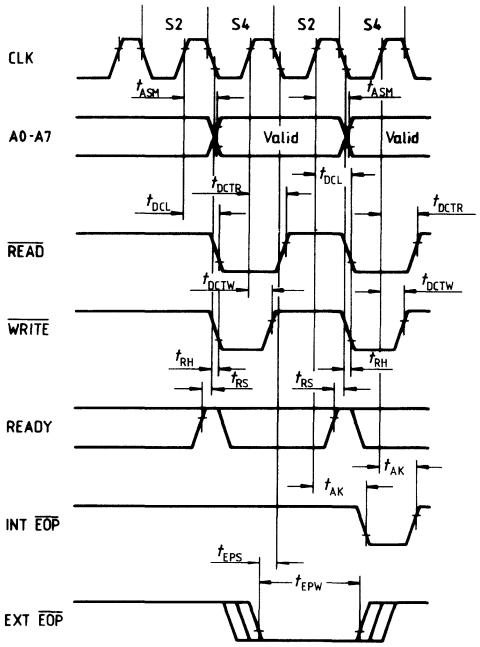


1) A16-A23 valid

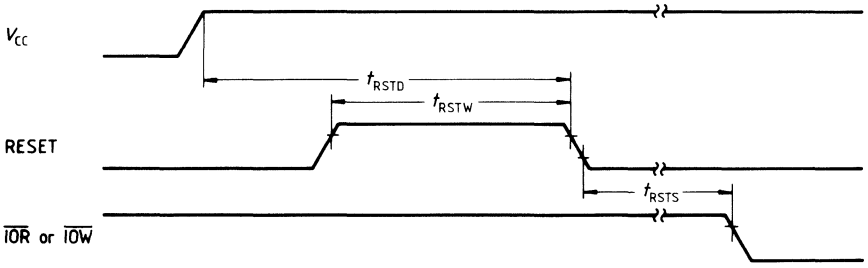
Ready Timing



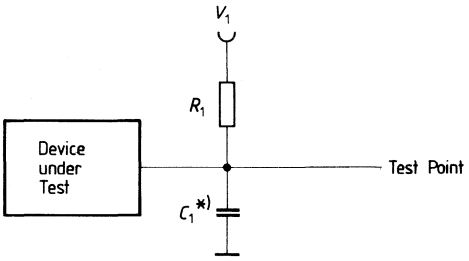
Compressed Transfer Timing



Reset Timing



AC Test Circuits

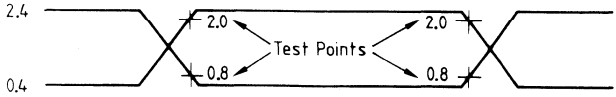


*) Includes stray and jig capacitance

Test Condition Definition

Pins	V_1	R_1	C_1
All Outputs Except $\overline{EOP}$	1.7 V	520 Ω	100 pF
$\overline{EOP}$	V_{CC}	1.6 KΩ	50 pF

Input Waveforms for AC Tests



Ordering Information

Type	Ordering code	Description
SAB 82C37B-5-P	Q 67120-P243	Programmable DMA controller 5 MHz (P-DIP-40)
SAB 82C37B-8-P	Q 67120-P244	Programmable DMA controller 8 MHz (P-DIP-40)

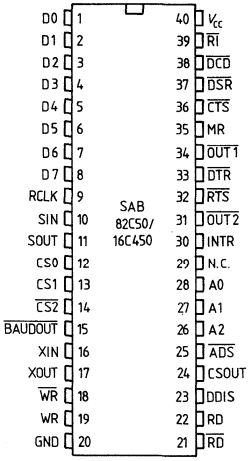
SAB 82C50/SAB 16C450 Universal Asynchronous Receiver/Transmitter

Preliminary

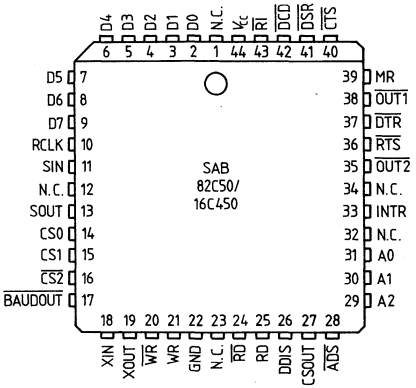
- Easily interfaces to most popular microprocessors
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from a serial data stream
- Holding and shift registers eliminate the need for precise synchronization between the CPU and the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to (2^{16}-1) and generates the internal 16× clock
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD)
- False start bit detection
- Complete status reporting capabilities
- Fully programmable serial interface characteristics:
  - 5/6/7/8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, $1^1/_2$, or 2-stop bit generation
  - Baud rate generation (DC to 512Kbaud)
- Tri-state TTL drive capability for bidirectional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Fully prioritized interrupt system controls
- P-DIP-40 and PL-CC-44 packages

Pin Configurations

P-DIP-40



PL-CC-44



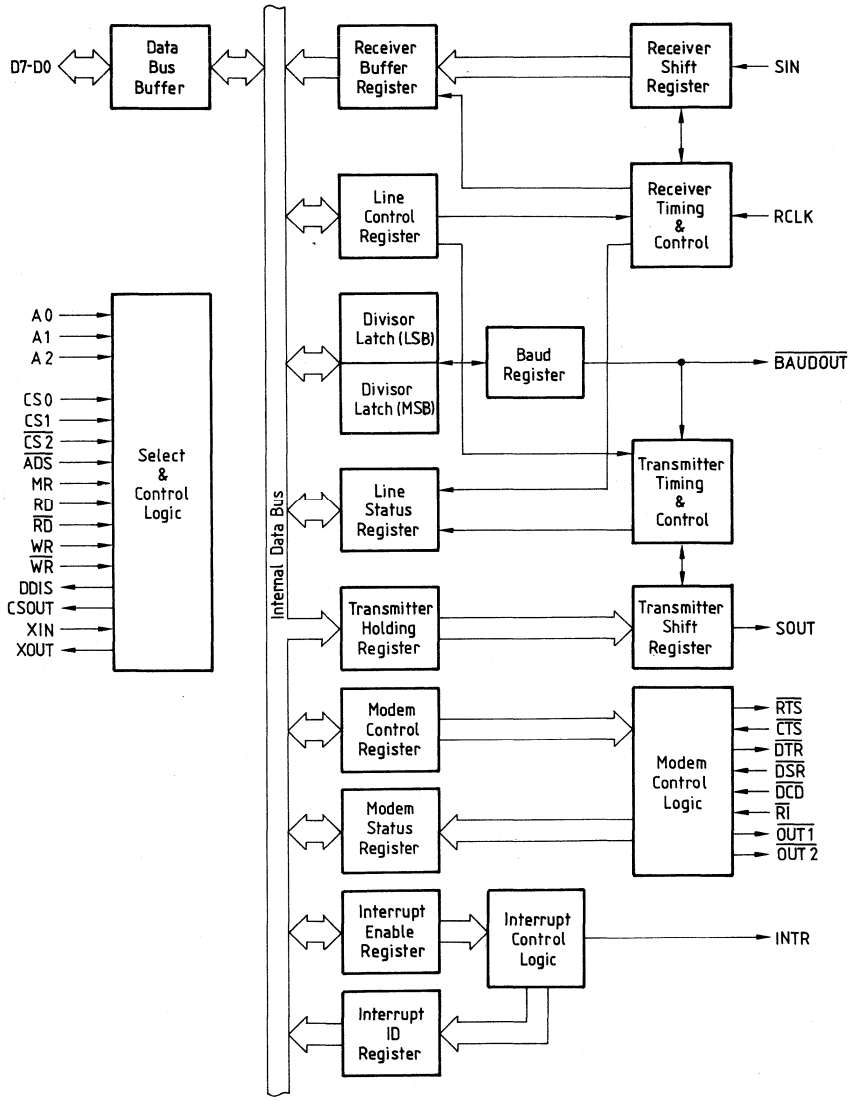
The SAB 82C50/16C450 (UART) performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error condition (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by 1 to (2^{16}-1), and of producing a 16× clock for driving the internal transmitter logic. Provisions have also been made to use this 16× clock for driving the receiver logic.

The UART features full modem-control capability and a processor interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing necessary for handling the communications link.

The SAB 82C50/16C450 is fabricated in Siemens ACMOS technology and comes in a 40-pin plastic dual-in-line package (P-DIP-40) or in a 44-pin plastic leaded chip carrier (PL-CC-44). The SAB 82C50/16C450 is compatible to the industry standard 8250/16450 communication controller.

Block Diagram



Pin Definitions and Functions

Symbol	Pin[1])	Input (I) Output (O)	Function
D0-D7	1-8	I/O	**Data bus** This bus comprises eight tri-state input/output lines. The bus provides bidirectional communication between the UART and the CPU. Data, control words, and status information are transferred via the D0-D7 data bus.
RCLK	9	I	**Receiver clock** This input is the 16× baud rate clock input for the receiver section of the chip.
SIN	10	I	**Serial data in** Serial data input from the communications link (peripheral device, modem, or data set).
SOUT	11	O	**Serial data out** This is the composite serial data output to the communications link (peripheral, modem or data set). The SOUT signal is set to the marking (logic 1) state upon a master reset operation or when the transmitter is idle.
CS0 CS1 $\overline{CS2}$	12 13 14	I I I	**Chip select** When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of an active address strobe signal latches the decoded chip select signals, completing chip selection. If $\overline{ADS}$ is always low, valid chip selects should stabilize according to the t_{CSW} parameter.
$\overline{BAUDOUT}$	15	O	**$\overline{Baud\ rate\ out}$** This is the 16× clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud rate generator divisor latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.
XIN XOUT	16 17	I O	**Oscillator in/out** These two pins connect the main timing reference (crystal or signal clock) to the UART. When a crystal oscillator or a clock signal is provided, it drives the UART via XIN (see typical clock circuits).
$\overline{WR}$ WR	18 19	I I	**Write/$\overline{Write}$** When WR is high or $\overline{WR}$ is low while the chip is selected, the CPU can write control words or data into the selected UART register. **Note:** Only one active WR or $\overline{WR}$ input is required to transfer data to the UART during a write operation. Therefore, tie either the WR input permanently low or the $\overline{WR}$ input permanently high, when it is not used.

[1]) Pin numbers are related to the plastic dual-in-line package (P-DIP-40).

Pin Definitions and Functions (cont'd)

Symbol	Pin[1]	Input (I) Output (O)	Function
$\overline{RD}$ RD	21 22	I I	**Read** When RD is high or $\overline{RD}$ is low while the chip is selected, the CPU can read status information or data from the selected UART register. **Note:** Only one active RD or $\overline{RD}$ input is required to transfer data from the UART during a read operation. Therefore, tie either the RD input permanently low or the $\overline{RD}$ input permanently high, when it is not used.
DDIS	23	O	**Driver disable** This signal goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the UART.
CSOUT	24	O	**Chip select out** When high, this signal indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when the UART is deselected.
$\overline{ADS}$	25	I	**$\overline{Address\ strobe}$** The positive edge of active address strobe ($\overline{ADS}$) signal latches the register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$) signals. **Note:** An active $\overline{ADS}$ input is required when the register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.
A2-A0	26-28	I	**Address 2–0** Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown in the following. Note that the state of the divisor latch access bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the baud rate generator divisor latches.

Register Addresses

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver buffer (read), transmitter holding register (write)
0	0	0	1	Interrupt enable
X	0	1	0	Interrupt identification (read only)
X	0	1	1	Line control
X	1	0	0	Modem control
X	1	0	1	Line status
X	1	1	0	Modem status
X	1	1	1	Scratch
1	0	0	0	Divisor latch (least significant byte)
1	0	0	1	Divisor latch (most significant byte)

[1]) Pin numbers are related to the plastic dual-in-line package (P-DIP-40).

Pin Definitions and Functions (cont'd)

Symbol	Pin[1]	Input (I) Output (O)	Function
INTR	30	O	**Interrupt request** This signal goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: receiver line status; received data available; transmitter holding register empty; and modem status. The INTR signals is reset low upon the appropriate interrupt service or a master reset operation.
$\overline{OUT2}$	31	O	**$\overline{Output\ 2}$** This user-designated output can be set to an active low by programming bit 3 (OUT 2) of the modem control register to a high level. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{RTS}$	32	O	**$\overline{Request\ to\ send}$** When low, this signal informs the modem or data set that the UART is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the modem control register. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{DTR}$	33	O	**$\overline{Data\ terminal\ ready}$** When low, this informs the modem or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the modem control register to a high level. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{OUT1}$	34	O	**$\overline{Output\ 1}$** This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the modem control register to a high level. A master reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
MR	35	I	**Master reset** When this input is high, all the registers (except for the receiver buffer, transmitter holding, and divisor latches) and the control logic of the UART are cleared. The states of various output signals (SOUT, INTR, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to Table 2). This input is buffered with a TTL-compatible Schmitt trigger with 0.5 V typical hysteresis.
$\overline{CTS}$	36	I	**$\overline{Clear\ to\ send}$** When low, this signal indicates that the modem or data set is ready to exchange data. The $\overline{CTS}$ signal is a modem status input whose condition can be tested by the CPU reading bit 4 (CTS) of the modem status register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the modem status register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the modem status register. $\overline{CTS}$ has no effect on the transmitter. **Note:** Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

[1]) Pin numbers are related to the plastic dual-in-line package (P-DIP-40).

Pin Definitions and Functions (cont'd)

Symbol	Pin[1]	Input (I) Output (O)	Function
$\overline{DSR}$			**$\overline{Data\ set\ ready}$** When low, this signal indicates that the modem or data set is ready to establish the communication link with the UART. The $\overline{DSR}$ signal is a modem status input whose condition can be tested by the CPU reading bit 5 (DSR) or the modem status register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the modem status register indicates whether the $\overline{DSR}$ input has changed since the previous reading of the modem status register. **Note:** Whenever the DSR bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.
$\overline{DCD}$	38	I	**$\overline{Data\ carrier\ detect}$** When low, it indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a modem status whose condition can be tested by the CPU reading bit 7 (DCD) of the modem status register. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the modem status register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the modem status register. $\overline{DCD}$ has no effect on the receiver. **Note:** Whenever the DCD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.
$\overline{RI}$	39	I	**$\overline{Ring\ indicator}$** When low, this signal indicates that a telephone ringing signal has been received by the modem or data set. The $\overline{RI}$ signal is a modem status input whose condition can be tested by the CPU reading bit 6 (RI) of the modem status register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the modem status register indicates whether the $\overline{RI}$ input signal has changed from a low to a high state since the previous reading of the modem status register. **Note:** Whenever the RI bit of the modem status register changes from a high to a low state, an interrupt is generated if the modem status interrupt is enabled.
V_{CC}	40	–	**Power supply** (+5V)
GND	20	–	**Ground** (0 V)

[1]) Pin numbers are related to the plastic dual-in-line package (P-DIP-40).

Register Description

Table 1: Summary of Registers

	Register Address				
	0 (DLAB = 0)	0 (DLAB = 0)	1 (DLAB = 0)	2	3
Bit no.	Receiver buffer register (read only)	Transmitter holding register (write only)	Interrupt enable register	Interrupt ident. register (read only)	Line control register
	RBR	THR	IER	IIR	LCR
0	Data bit 0 [1]	Data bit 0 [1]	Received data available	"0" if interrupt is pending	Word length select bit 0 (WLS0)
1	Data bit 1	Data bit 1	Transmitter holding register empty	Interrupt ID bit 0	Word length select bit 1 (WLS1)
2	Data bit 2	Data bit 2	Receiver line status	Interrupt ID bit 1	Number of stop bits (STB)
3	Data bit 3	Data bit 3	Modem status	0	Parity enable (PEN)
4	Data bit 4	Data bit 4	0	0	Even parity select (EPS)
5	Data bit 5	Data bit 5	0	0	Stick parity
6	Data bit 6	Data bit 6	0	0	Set break
7	Data bit 7	Data bit 7	0	0	Divisor latch access bit (DLAB)

[1]) Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Table 1: Summary of Registers (cond't)

	Register Address					
	4	5	6	7	0 (DLAB = 1)	1 (DLAB = 1)
Bit no.	Modem control register	Line status register	Modem status register	Scratch register	Divisor latch (LS)	Divisor latch (MS)
	MCR	LSR	MSR	SCR	DLL	DLM
0	Data terminal ready (DTR)	Data ready (DR)	Delta clear to send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to send (RTS)	Overrun error (OE)	Delta data set ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Out 1	Parity error (PE)	Trailing edge ring indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Out 2	Framing error (FE)	Delta data carrier detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Loop	Break interrupt (BI)	Clear to send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter holding register (THRE)	Data set ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter empty (TEMT)	Ring indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	0	Data carrier detect (DCD)	Bit 7	Bit 7	Bit 15

Table 2: Register Reset Functions

Register/signal	Reset control	Reset state
Interrupt enable register	Master reset	**0000** 0000 [1]
Interrupt identification register	Master reset	**0000 000**1
Line control register	Master reset	0000 0000
Modem control register	Master reset	**000**0 0000
Line status register	Master reset	**0**110 0000
Modem status register	Master reset	XXXX 0000 [2]
SOUT	Master reset	High
INTR (RCVR errors)	Read LSR/MR	Low
INTR (RCVR data ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/write THR/MR	Low
INTR (Modem status changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master reset	High
$\overline{\text{RTS}}$	Master reset	High
$\overline{\text{DTR}}$	Master reset	High
$\overline{\text{OUT 1}}$	Master reset	High

[1]) Boldface bits are permanently low.
[2]) Bits 7-4 are driven by the input signals.

The system programmer may access any of the UART registers summarized in Table 1 via the CPU. These registers control UART operations including transmission and reception of data. Each register bit in Table 1 has its name and reset state shown in Table 2.

Line control register

The system programmer specifies the format of the asynchronous data communication exchange and sets the divisor latch access bit via the line control register (LCR). The programmer can also read the contents of the line control register. The read capability simplifies system programming and eliminates the need for separate storage of the line characteristics in system memory.

Table 1 shows the contents of the LCR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2: This bit specifies the number of stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one stop bit is generated or checked in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, irrespective of the number of stop bits selected.

Bit 3: This bit is the parity enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).

Bit 4: This bit is the even parity select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's is transmitted or checked.

Bit 5: This bit is the stick parity bit. When bits 3, 4 and 5 are logic 1, the parity bit is transmitted and checked as a logic 0. If bits 3 and 5 are 1 and bit 4 is logic 0 then the parity bit is transmitted and checked as a logic 1. If bit 5 is a logic 0 stick parity is disabled.

Bit 6: This bit is the break control bit. It causes a break condition to be transmitted by the UART. When it is set to a logic 1, the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by clearing bit 6 to a logic 0. The break control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all O's pad character in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission is to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the divisor latch access bit (DLAB). It must be set high (logic 1) to access the divisor latches of the baud generator during a read or write operation. It must be set low (logic 0) to access the receiver buffer, the transmitter holding register or the interrupt enable register.

Table 3: Baud Rates Using 1.8432 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 x clock	Percent error difference between desired and actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Programmable Baud Rate Generator

The UART contains a programmable baud rate generator that is capable of taking any clock input from DC to 8.0 MHz (SAB 16C450 only; SAB 82C50 : 3.1 MHz) and dividing it by any divisor from 1 to 2^{16}. The output frequency of the baud rate generator is 16 x the baud rate [divisor = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded.

Tables 3, 4 and 5 provide decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 8 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommendable.

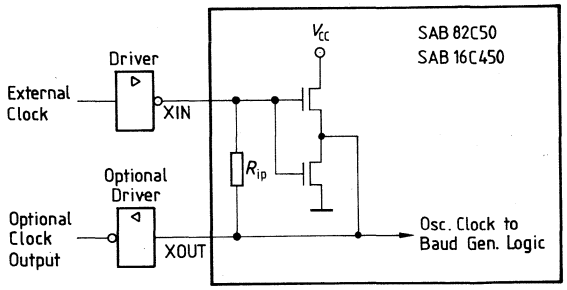
Table 4: Baud Rates Using 3.072 MHz Crystal

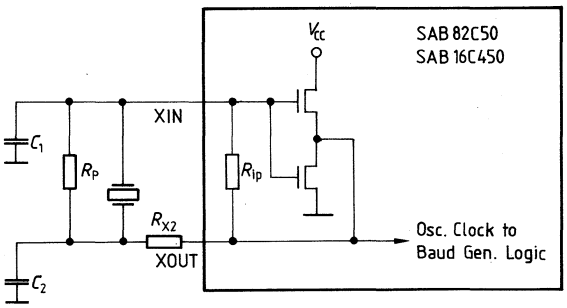
Desired baud rate	Decimal divisor used to generate 16 x clock	Percent error difference between desired and actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Table 5: Baud Rates Using 8 MHz Crystal

Desired baud rate	Decimal divisor used to generate 16 x clock	Percent error difference between desired and actual
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

Typical Clock Circuits





Typical Oscillator Networks

Crystal [1]	R_p [2]	R_{x2}	C_1	C_2
1.8-8.0 MHz	1MΩ	1.5k	10-30 pF	40-60 pF

[1] Crystal > 3.1 MHz SAB 16C450 only.
[2] Due to internal R_{ip} external, R_p may be dropped.

Line Status Register

This 8-bit register provides the CPU with status information concerning the data transfer. Table 1 shows the contents of the line status register. Details on each bit follow:

Bit 0: This bit is the receiver data ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 is reset to a logic 0 reading the data in the receiver buffer register.

Bit 1: This bit is the overrun error (OE) indicator. Bit 1 indicates that data in the receiver buffer register was not read by the CPU **before** the transfer of the next character into the receiver buffer register, thus destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the line status register.

Bit 2: This bit is the parity error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or ood parity, as selected by the even parity select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the line status register.

Bit 3: This bit is the framing error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic 1 whenever the stop bit following the last data bit or parity bit is a logic 0 (spacing level). The FE indicator is reset whenever the CPU reads the contents of the line status register. The UART will try to resynchronize after a framing error. Therefore, it assumes that the framing error was due to the next start bit, samples this "start" bit twice and then takes in the "data".

Bit 4: This bit is the break interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (i.e., the total time of start bit + data bits + parity + stop bits).
The BI indicator is reset whenever the CPU reads the contents of the line status register. Restarting after a break is received requires the SIN pin to be logic 1 for at least ½ bit time.

Note: Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Table 6: Interrupt Control Functions

Interrupt identification register				**Interrupt set and reset functions**		
Bit 2	**Bit 1**	**Bit 0**	**Priority level**	**Interrupt type**	**Interrupt source**	**Interrupt reset control**
0	0	1	–	None	None	–
1	1	0	Highest	Receiver line status	Overrun error or parity error or framing error or break interrupt	Reading the line status register
1	0	0	Second	Received data available	Receive data available	Reading the receiver buffer register
0	1	0	Third	Transmitter holding register empty	Transmitter holding register empty	Reading the IIR register (if source of interrupt) or Writing into the transmitter holding register
0	0	0	Fourth	modem status	Clear to send or data set ready or ring indicator or data carrier detect	Reading the modem status register

Bit 5: This bit is the transmitter holding register empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the transmitter holding register empty interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logic 0 whenever the CPU loads the transmitter holding register.

Bit 6: This bit is the transmitter empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The line status register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

Interrupt Identification Register

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the interrupt identification register. The four levels of interrupt conditions in order of priority are: receiver line status, received data ready, transmitter holding register empty and modem status.
When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table 1 shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 6.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This register enables the four types of UART interrupts. Each interrupt can individually activate the interrupt (INTR) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt enable register (IER). Similarly, setting bits of this register to a logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTR output signal. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. Table 1 shows the contents of the IER. Details on each bit follow:

Bit 0: This bit enables the received data available interrupt when set to logic 1.

Bit 1: This bit enables the transmitter holding register empty interrupt when set to logic 1.

Bit 2: This bit enables the receiver status interrupt when set to logic 1.

Bit 3: This bit enables the modem status interrupt when set to logic 1.

Bit 4 through 7: These four bits are always logic 0.

Modem Control Register

This register controls the interface to the Modem or data set (or a peripheral device emulating a Modem). The contents of the Modem control register (MCR) are indicated in Table 1 and are described below. Details on each bit follow:

Bit 0: This bit controls the data terminal ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Note: The $\overline{DTR}$ output of the UART may be applied to an EIA inverting line driver (such as the 1488) to obtain the proper polarity input at the succeeding Modem or data set.

Bit 1: This bit controls the request to send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the output ($\overline{OUT\ 1}$) signal, which is an auxiliary user-signated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter serial output (SOUT) is set to the marking (logic 1) state; the receiver serial input (SIN) is disconnected; the output of the transmitter shift register is "looped back" into the receiver shift register input; the four Modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; and the four Modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four Modem control inputs. The Modem control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem control interrupts are also operational, but the interrupt's sources are now the lower four bits of the Modem control register instead of the four Modem control inputs. The interrupts are still controlled by the interrupt enable register.

Bits 5 through 7: These bits are permanently set to logic 0.

Modem Status Register

This register provides the current state of the control lines from the Modem (or peripheral device) to the CPU. In addition to this current-state information, four bits of the Modem status register provide change information. These bits are set to a logic 1 whenever a control input from the Modem changes state. They are reset to logic 0 whenever the CPU reads the Modem status register.

Table 1 shows the contents of the MSR. Details on each bit follow:

Bit 0: This bit is the delta clear to send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the delta data set ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the trailing edge of ring indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the delta data carrier detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem status interrupt is generated.

Bit 4: This bit is the complement of the clear to send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the data set ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

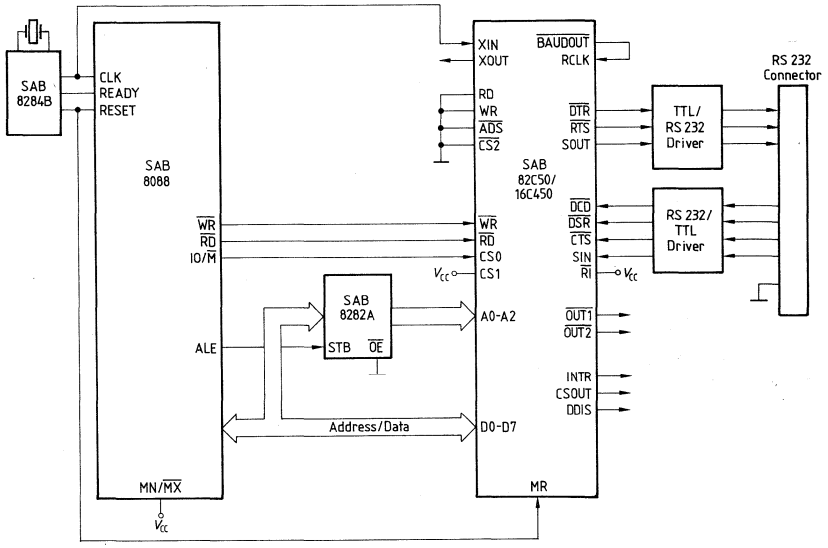
Bit 6: This bit is the complement of the ring indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the data carrier detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 in the MCR.

Scratchpad Register

This 8-bit read/write register does not control the UART in any way. It is intended as a scratch-pad register to be used by the programmer to hold data temporarily.

Typical Application



Absolute Maximum Ratings

Ambient temperature under bias	0° to	70°C
Storage temperature	−65° to	+150°C
Supply voltage	−0.5 to	+ 7.0V
Voltage on any pin with respect to ground	−0.5 to	V_{CC} + 0.5V
Power dissipation		700mW

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5V ± 5%; GND = 0V

Parameter	Symbol	Limit values		Units	Test conditions
		min.	max.		
Input low voltage	V_{IL}	−0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.4	V	I_{OL} = 1.6 mA [1])
Output high voltage	V_{OH}	2.4		V	I_{OH} = −1.0 mA [1])
Avg. power supply current	I_{CC} (AV)	–	10	mA	V_{CC} = 5.25V, T_A = 25°C No loads on output SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2.4V All other inputs = 0.4V Baud rate generator is 4 MHz Baud rate is 50 Kbaud
Input leakage current	I_{IL}	–	± 10	µA	V_{CC} = 5.25V, GND = 0V All other pins floating. V_{IN} = 0V, 5.25V
Clock leakage current	I_{CL}	–	± 20	µA	
Tri-state leakage current	I_{OZ}	–	± 20	µA	V_{CC} = 5.25V, GND = 0V V_{OUT} = 0V, 5.25V 1. Chip deselected 2. WRITE mode, chip selected
MR Schmitt V_{IL}	V_{ILMR}	–	0.8	V	–
MR Schmitt V_{IH}	V_{IHMR}	2.0	–	V	–

Capacitance [2]

$T_A = 25°C$; $V_{CC} = GND = 0V$

Parameter	Symbol	Limit values		Units	Test conditions
		min.	max.		
Clock input capacitance	C_{XIN}	–	20	pF	$f_c = 1$ MHz Unmeasured pins returned to GND
Clock output capacitance	C_{XOUT}	–	30	pF	
Input capacitance	C_{IN}	–	10	pF	
Output capacitance	C_{OUT}	–	20	pF	

[1]) Does not apply to XOUT.
[2]) These parameters are periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5V ± 5%; GND = 0V

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
Address strobe width	t_{ADS}	60	–	90	–	ns	–
Address hold time	t_{AH}	0	–	0	–	ns	–
RD, $\overline{RD}$ delay from address	t_{AR}	30	–	80	–	ns	1)
Address setup time	t_{AS}	60	–	90	–	ns	–
WR, $\overline{WR}$ delay from address	t_{AW}	30	–	80	–	ns	1)
Chip select hold time	t_{CH}	0	–	0	–	ns	–
Chip select setup time	t_{CS}	60	–	90	–	ns	–
Chip select output delay from select	t_{CSC}	–	100	–	125	ns	100 pF loading 1)
RD, $\overline{RD}$ delay from chip select	t_{CSR}	30	–	80	–	ns	1)
WR, $\overline{WR}$ delay from select	t_{CSW}	30	–	80	–	ns	1)
Data hold time	t_{DH}	30	–	60	–	ns	–
Data setup time	t_{DS}	30	–	90	–	ns	–
RD, $\overline{RD}$ to floating data delay	t_{HZ}	0	100	0	100	ns	100 pF loading 2)
Master reset pulse width	t_{MR}	5	–	10	–	µs	–
Address hold time from RD, $\overline{RD}$	t_{RA}	20	–	20	–	ns	1)
Read cycle delay	t_{RC}	125	–	500	–	ns	–
Chip select hold time from RD, $\overline{RD}$	t_{RCS}	20	–	20	–	ns	1)
RD, $\overline{RD}$ strobe width	t_{RD}	125	–	175	–	ns	–
RD, $\overline{RD}$ to driver disable delay	t_{RDD}	–	60	–	75	ns	100 pF loading 2)
Delay from RD, $\overline{RD}$ to data	t_{RVD}	–	125	–	175	ns	100 pF loading
Address hold time from WR, $\overline{WR}$	t_{WA}	20	–	20	–	ns	1)
Write cycle delay	t_{WC}	150	–	500	–	ns	–
Chip select hold time from WR, $\overline{WR}$	t_{WCS}	20	–	20	–	ns	1)

AC Characteristics (cont'd)

T_A = 0 to 70°C; V_{CC} = 5V ± 5%; GND = 0V

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
WR, $\overline{WR}$ strobe width	t_{WR}	100	–	175	–	ns	–
Duration of clock high pulse	t_{XH}	55	–	140	–	ns	3)
Duration of clock low pulse	t_{XL}	55	–	140	–	ns	3)
Read cycle = $t_{AR} + t_{RD} + t_{RC}$	RC	280	–	755	–	ns	–
Write cycle = $t_{AW} + t_{WR} + t_{WC}$	WC	280	–	755	–	ns	–

1) Applicable only when $\overline{ADS}$ is tied low.
2) Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.
3) SAB 82C50: External clock max. 3.1 MHz
SAB 16C450: External clock max. 8.0 MHz

Baud Rate Generator

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
Baud divisor	N	1	2^{16}-1	1	2^{16}-1		–
Baud output positive edge delay	t_{BHD}	–	175	–	250	ns	100 pF load
Baud output negative edge delay	t_{BLD}	–	175	–	250	ns	100 pF load
Baud output up time	t_{HW}	75	–	250	–	ns	1)
Baud output down time	t_{LW}	100	–	425	–	ns	2)

1) SAB 16C450: f_x = 8.0 MHz, ÷ 2, 100 pF load
SAB 82C50: f_x = 3.0 MHz, ÷ 3, 100 pF load

2) SAB 16C450: f_x = 8.0 MHz, ÷ 2, 100 pF load
SAB 82C50: f_x = 2.0 MHz, ÷ 2, 100 pF load

Receiver and Transmitter

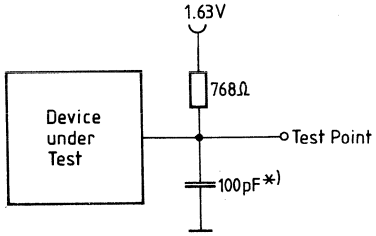
Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
Delay from RD, $\overline{RD}$ (RD RBR or RD LSR) to reset interrupt	t_{RINT}	–	1	–	1	µs	100 pF load
Delay from RCLK to sample time	t_{SCD}	–	2	–	2	µs	–
Delay from stop to set interrupt	t_{SINT}	–	1	–	1	RCLK cycles	[1]
Delay from WR, $\overline{WR}$ (WR THR) to reset interrupt	t_{HR}	–	175	–	1000	ns	100 pF load
Delay from RD, $\overline{RD}$ (RD IIR) to reset interrupt (THRE)	t_{IR}	–	250	–	1000	ns	100 pF load
Delay from initial INTR reset to transmit start	t_{IRS}	24	40	24	40	BAUD-OUT cycles	–
Delay from initial write to interrupt	t_{SI}	32	48	32	48	BAUD-OUT cycles	–
Delay from stop to interrupt (THRE)	t_{STI}	8	8	8	8	BAUD-OUT cycles	–

[1] RCLK is equal to t_{XH} and t_{XL}.

Modem Control

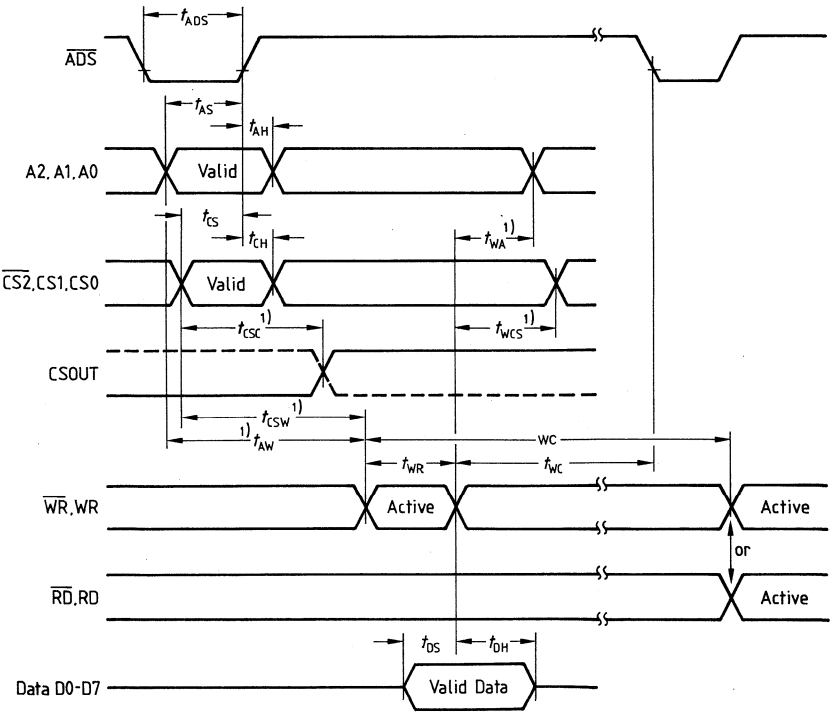
Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 16C450		SAB 82C50			
		min.	max.	min.	max.		
Delay from WR, $\overline{WR}$ (WR MCR) to output	t_{MDO}	–	200	–	1000	ns	100 pF load
Delay to reset interrupt from RD, $\overline{RD}$ (RD MSR)	t_{RIM}	–	250	–	1000	ns	100 pF load
Delay to set interrupt from Modem input	t_{SIM}	–	250	–	1000	ns	100 pF load

AC Test Circuit



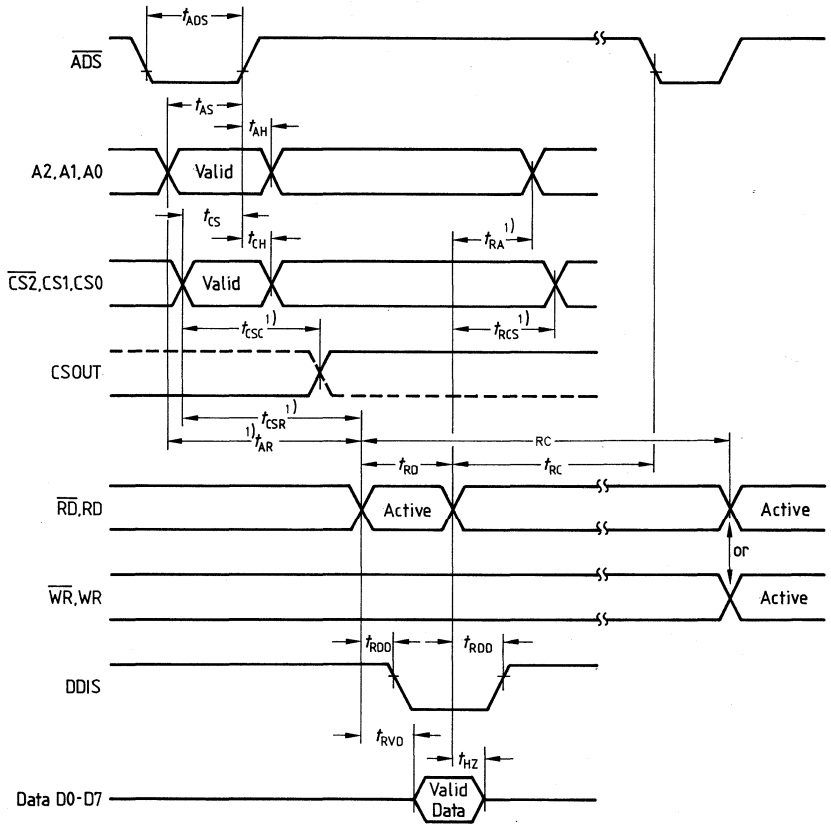
*) Includes stray and jig capacitance

Write Cycle Timing



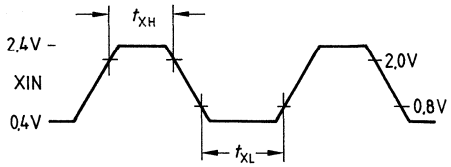
1) Applicable only when ADS is tied low.

Read Cycle Timing

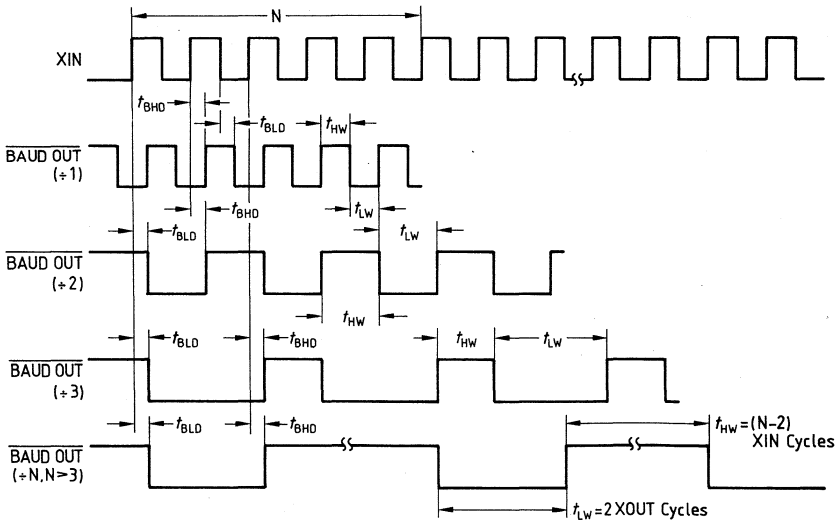


1) Applicable only when $\overline{ADS}$ is tied low.

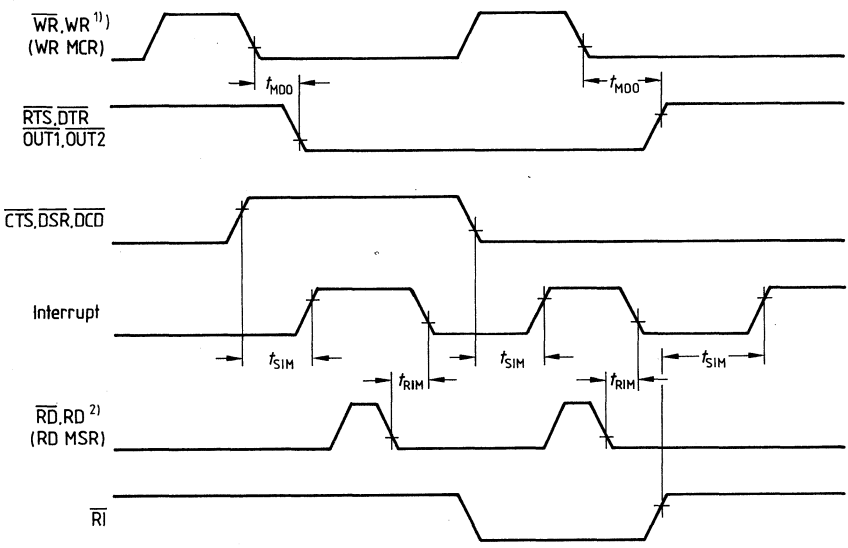
External Clock Input Timing



BAUDOUT Timing

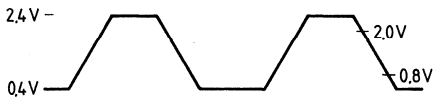


Modem Control Timing

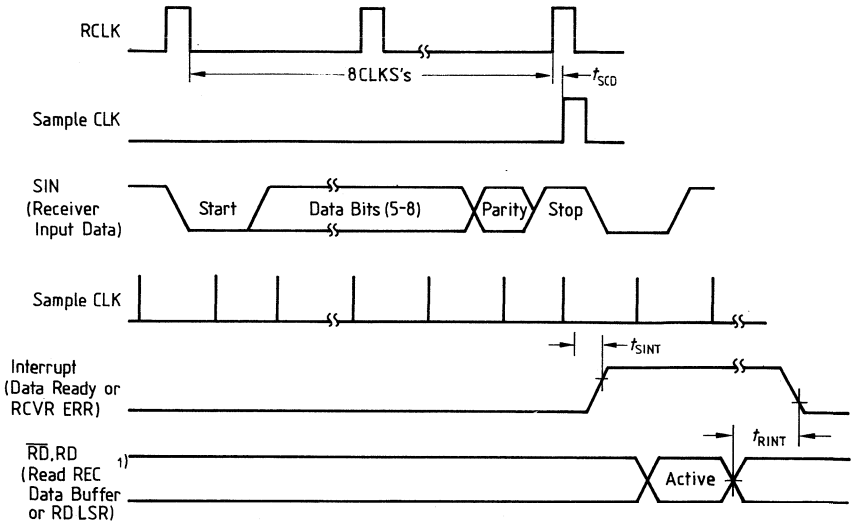


1) See Write Cycle Timing
2) See Read Cycle Timing

AC Test Points

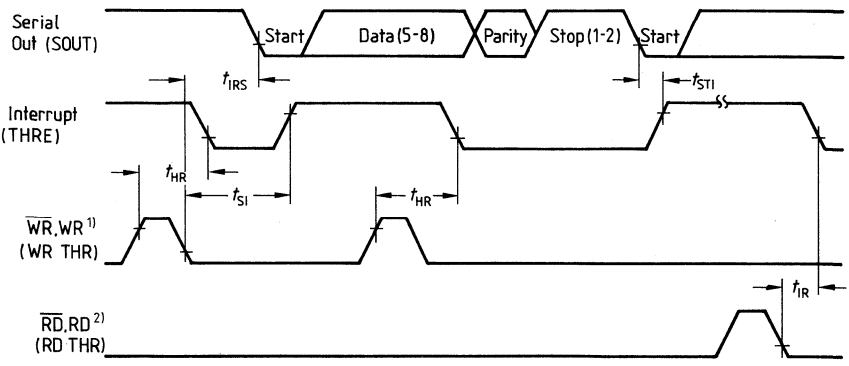


Receiver Timing



1)See Read Cycle Timing

Transmitter Timing



1) See Write Cycle Timing
2) See Read Cycle Timing

Ordering Information

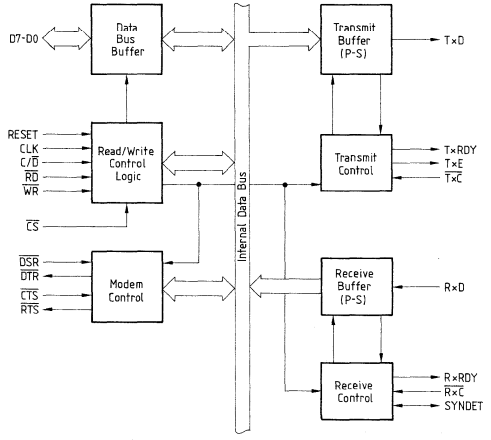
Type	Ordering code	Function
SAB 82C50-P	Q67120-P282	Programmable communication interface (P-DIP-40)
SAB 82C50-N	Q67120-P283	Programmable communication interface (PL-CC-44)
SAB 16C450-P	Q67120-P284	Programmable communication interface (P-DIP-40)
SAB 16C450-N	Q67120-P285	Programmable communication interface (PL-CC-44)

Advance Information

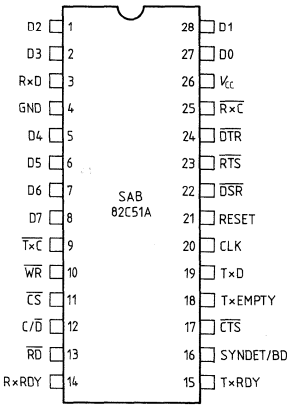
SAB 82C51A Programmable Communications Interface

- Synchronous and asynchronous operation
- Synchronous 5-bit to 8-bit characters; internal or external character synchronization; automatic sync insertion
- Asynchronous 5-bit to 8-bit characters; clock rate 1, 16 or 64 times baud rate; break character generation; 1, 1½ or 2 stop bits; false start bit detection; automatic break detect and handling
- Synchronous baud rate DC to 240 Kbaud
- Asynchronous baud rate DC to 96 Kbaud
- Full-duplex, double-buffered transmitter and receiver
- Error detection parity, overrun and framing
- Compatible with an extended range of Siemens microprocessors
- CMOS technology
- 28-pin plastic dual-in-line package, P-DIP-28
- All inputs and outputs are TTL-compatible

Block Diagram



Pin Configuration



The Siemens SAB 82C51A is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Siemens microprocessor families such as SAB 8048/8051/8085 and SAB 8086/8088. The SAB 82C51A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using Siemens high-performance CMOS technology.

Pin Definitions and Functions

System Bus Interface

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>D0-D7</td><td>1, 2, 5, 6, 7,
8, 27, 28</td><td>I/O</td><td>DATA 0 TO 7
Bidirectional tristate data bus lines.</td></tr>
<tr><td>$\overline{WR}$</td><td>10</td><td>I</td><td>$\overline{WRITE}$
A low on this input informs the SAB 82C51A that the CPU is writing data or control words to the SAB 82C51A.</td></tr>
<tr><td>$\overline{CS}$</td><td>11</td><td>I</td><td>$\overline{CHIP\ SELECT}$
A low on this input selects the SAB 82C51A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the data bus is in the float state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chip.</td></tr>
<tr><td>C/$\overline{D}$</td><td>12</td><td>I</td><td>CONTROL/$\overline{DATA}$
This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the SAB 82C51A that the word on the data bus is either a data character, control word or status information.
1 = Control/Status; 0 = Data.
<table>
<tr><th>C/$\overline{D}$</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th></th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>SAB 82C51A Data → Data Bus</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus → SAB 82C51A Data</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Status → Data Bus</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus → Control</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>0</td><td>Data Bus → Tristate</td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>1</td><td>Data Bus → Tristate</td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$</td><td>13</td><td>I</td><td>$\overline{READ}$
A low on this input informs the SAB 82C51A that the CPU is reading data or status information from the SAB 82C51A.</td></tr>
<tr><td>CLK</td><td>20</td><td>I</td><td>CLOCK
The CLK input is used to generate internal device timing and is normally connected to the phase 2 (TTL) output of the clock generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the receiver or transmitter data bit rates.</td></tr>
<tr><td>RESET</td><td>21</td><td>I</td><td>RESET
A high on this input forces the SAB 82C51A into an idle mode. The device will remain idle until a new set of control words is written into the SAB 82C51A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).
A command reset operation also puts the device into the idle state.</td></tr>
</table>

Modem Control

Symbol	Pin	Input (I) Output (O)	Function
$\overline{CTS}$	17	I	**$\overline{CLEAR\ TO\ SEND}$** A low on this input enables the SAB 82C51A to transmit serial data if the TxEnable bit in the command byte is set to a "one". If either a TxEnable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to TxDisable command before shutting down.
$\overline{DSR}$	22	I	**$\overline{DATA\ SET\ READY}$** The $\overline{DSR}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a status read operation. The $\overline{DSR}$ input is normally used to test modern conditions such as data set ready.
$\overline{RTS}$	23	O	**$\overline{REQUEST\ TO\ SEND}$** The $\overline{RTS}$ output signal is a general-purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the command instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as request to send.
$\overline{DTR}$	24	O	**$\overline{DATA\ TERMINAL\ READY}$** The $\overline{DTR}$ output signal is a general-purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the command instruction word. The $\overline{DTR}$ output signal is normally used for modem control such as data terminal ready.

Transmit Control

Symbol	Pin	Input (I) Output (O)	Function
$\overline{TxC}$	9	I	**$\overline{TRANSMITTER\ CLOCK}$** The transmitter clock controls the rate at which the character is to be transmitted. In the synchronous transmission mode, the baud rate (1x) is equal to the $\overline{TxC}$ frequency. In asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$. For example: If the baud rate equals 110 baud, $\overline{TxC}$ equals 110 Hz in the 1x mode, $\overline{TxC}$ equals 1.72 kHz in the 16x mode, $\overline{TxC}$ equals 7.04 kHz in the 64x mode. The falling edge of $\overline{TxC}$ shifts the serial data out of the SAB 82C51A.
TxRDY	15	O	**TRANSMITTER READY** This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by TxEnable; or, for polled operation, the CPU can check TxRDY using a status read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU. Note that when using the polled operation, the TxRDY status bit is *not* masked by TxEnable, but will only indicate the empty/full status of the Tx data input register.
TxEMPTY	18	O	**TRANSMITTER EMPTY** When the SAB 82C51A has no characters to send, the TxEMPTY output will go high. It resets upon receiving a character from CPU if the transmitter is enabled. TxEMPTY remains high when the transmitter is disabled. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplex operational mode. In the synchronous mode, a high on this output indicates that a character has not been loaded and the sync character or characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go low when the sync characters are being shifted out.
TxD	19	O	**TRANSMIT DATA** This pin is used to transmit the serial data. Serial output data on TxD is changed from parallel data to serial data. In accordance with this, the TxD line will be held in the marking state ('1' level) upon one of the following events: – master reset – CTS signal is high ($\overline{CTS}$ = 1) – TxDisable (TxEN = 0) – TxEMPTY signal is high (TxEMPTY = 1)

Receive Control

Symbol	Pin	Input (I) Output (O)	Function
RxD	3	I	**RECEIVE DATA** This pin is used to receive the serial data. Serial input data on this line is changed to parallel data according to the format specified by the control words, and then transferred to the receive data buffer.
RxRDY	14	O	**RECEIVER READY** This output indicates that the SAB 82C51A contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a status read operation. RxEnable, when off, holds RxRDY in the reset condition. For asynchronous mode, to set RxRDY, the receiver must be enabled to sense a start bit and a complete character must be assembled and transferred to the data output register. For synchronous mode, to set RxRDY, the receiver must be enabled and a character must finish assembly and be transferred to the data output register. Failure to read the character received from the Rx data output register prior to the assembly of the next Rx data character will set overrun condition error and the previous character will be written over and lost. If the Rx data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.
SYNDET/BD	16	I/O	**SYNC DETECT/BREAK DETECT** This pin is used for SYNDET in synchronous mode and may be used as either input or output, programmable through the control word. It is reset to output mode low upon RESET. When used as an output (internal sync mode), the SYNDET pin will go high to indicate that the SAB 82C51A has located the sync character in the receive mode. If the SAB 82C51A is programmed to use double sync characters then SYDET will go high in the middle of the last bit of the second sync character. SYNDET is automatically reset upon a status read operation. When used as an input (external sync mode), a positive going signal will cause the SAB 82C51A to start assembling data characters on the rising edge of the next $\overline{RxC}$. In asynchronous mode this pin is used for BD. This output will go high whenever the receiver remains low through two consecutive stop bit sequences (including the start bits, data bits, and parity bits). Break detect may also be read as a status bit. It is reset only upon a master chip reset or RxD returning to a "one" state.

Receive Control (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{RxC}$	25	I	**$\overline{RECEIVER\ CLOCK}$** The receiver clock controls the rate at which the character is to be received. In synchronous mode, the baud rate (1x) is equal to the actual frequency of $\overline{RxC}$. In asynchronous mode, the baud rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 the $\overline{RxC}$. For example: The baud rate equals 2400 baud, if $\overline{RxC}$ equals 2400 Hz in the 1x mode, $\overline{RxC}$ equals 38.4 kHz in the 16x mode, $\overline{RxC}$ equals 153.6 kHz in the 64x mode. Data is sampled into the SAB 82C51A on the rising edge of $\overline{RxC}$.

Power Supply

Symbol	Pin	Function
GND	4	**GROUND** (0 V)
V_{CC}	26	**POWER SUPPLY** (+5 V)

Operational Description

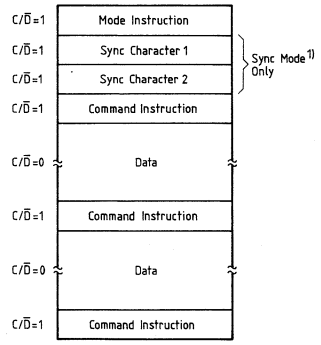
General

The complete functional definition of the SAB 82C51A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the SAB 82C51A to support the desired communications format. These control words will program the baud rate, character length, number of stop bits, synchronous or asynchronous operation, even/odd/off parity, etc. In the synchronous mode, options are also provided to select either internal or external character synchronization.

Once programmed, the SAB 82C51A is ready to perform its communication functions. The TxRDY output is raised high to signal the CPU that the SAB 82C51A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the SAB 82C51A. On the other hand, the SAB 82C51A receives serial data from the modem or I/O device. Upon receiving an entire character, the RxRDY output is raised high to signal the CPU that the SAB 82C51A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The SAB 82C51A cannot begin transmission until the TxEnable (transmitter enable) bit is set in the command instruction and it has received a clear-to-send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon reset.

Typical Data Block



1) The second sync character is skipped if mode instruction has programmed the SAB 82C51A to single character sync mode. Both sync characters are skipped if mode instruction has programmed the SAB 82C51A to async mode.

Programming the SAB 82C51A

Prior to starting data transmission or reception, the SAB 82C51A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the SAB 82C51A and must immediately follow a reset operation (internal or external).

The control words are split into two formats:

1. Mode instruction
2. Command instruction

Mode Instruction

This instruction defines the general operational characteristics of the SAB 82C51A. It must follow a reset operation (internal or external). Once the mode instruction has been written into the SAB 82C51A by the CPU, sync characters or command instructions may be written.

Command Instruction

This instruction defines a word that is used to control the actual operation of the SAB 82C51A.

Both the mode and command instructions must conform to a specified sequence for proper device operation (see figure Typical Data Block). The mode instruction must be written immediately following a reset operation, prior to using the SAB 82C51A for data communication.

All control words written into the SAB 82C51A after the mode instruction will load the command instruction. Command instructions can be written into the SAB 82C51A at any time in the data block during the operation of the SAB 82C51A. To return to the mode instruction format, the master reset bit in the command instruction word can be set to initiate an internal reset operation which automatically places the SAB 82C51A back into the mode instruction format. Command instructions must follow the mode instruction or sync characters.

Mode Instruction Definition

The SAB 82C51A can be used for either asynchronous or synchronous data communication. To understand how the mode instruction defines the functional operation of the SAB 82C51A, the designer can best view the device as two separate components, one asynchronous and the other synchronous, sharing the same package. The format definition can be changed only after a master chip reset. For explanation purposes the two formats will be isolated.

Note:
When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx data line cannot be read on the data bus. In the case of a programmed character length of less than 8 bits, the least significant data bus bits will hold the data; unused bits are "don't care" when writing data to the SAB 82C51A, and will be "zeros" when reading the data from the SAB 82C51A.

Asynchronous Mode (transmit)

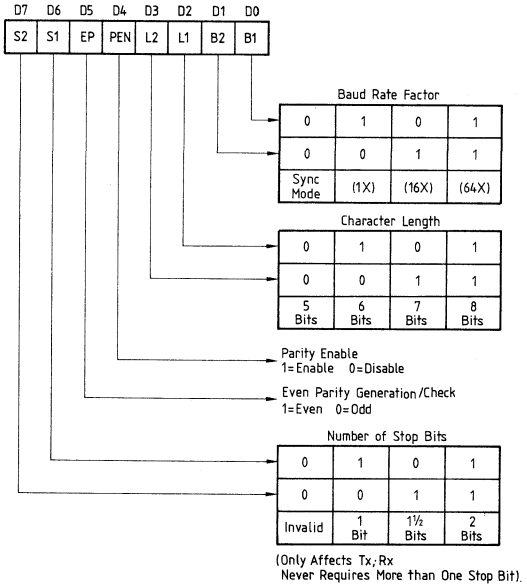
Whenever a data character is sent by the CPU the SAB 82C51A automatically adds a start bit (low level) followed by the data bits (least significant bit first), and the programmed number of stop bits to each character. Also, an even or odd parity bit is inserted prior to the stop bit(s), as defined by the mode instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, $1/16$ or $1/64$ that of the $\overline{TxC}$, as defined by the mode instruction. Break characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the SAB 82C51A the TxD output remains "high" (marking) unless a break (continuously low) has been programmed.

Asynchronous Mode (receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a start bit. The validity of this start bit is checked by again strobing this bit at its nominal center (16x or 64x mode only). If a low is detected again, it is a valid start bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of the $\overline{RxC}$. If a low level is detected as the stop bit the framing error flag will be set. The stop bit signals the end of a character. Note that the receiver requires only one stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the SAB 82C51A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the overrun error

Mode Instruction Format, Asynchronous Mode



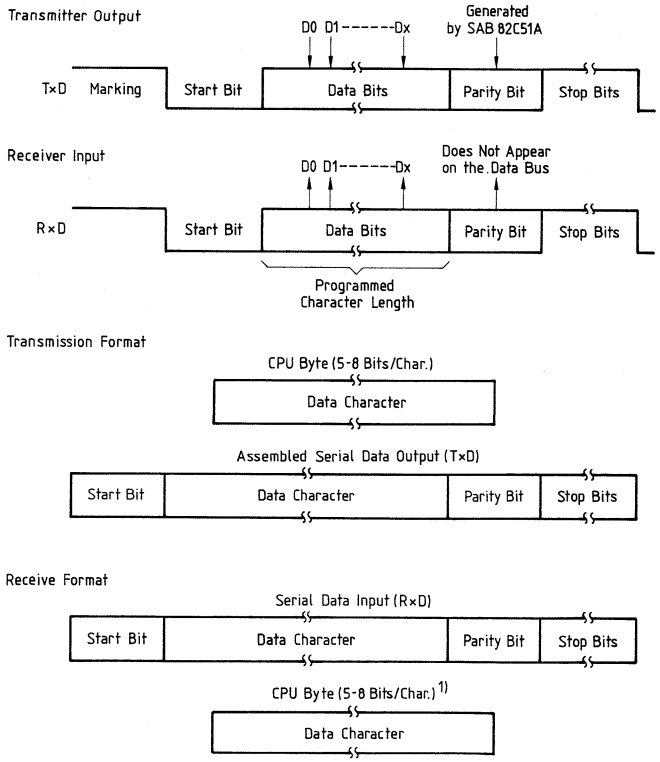
flag is raised (thus the previous character is lost). All of the error flags can be reset by an error reset instruction. The occurrence of any of these errors will not affect the operation of the SAB 82C51A.

Synchronous Mode (transmit)

The TxD output is continuously high until the CPU sends its first character to the SAB 82C51A which usually is a sync character. When the $\overline{CTS}$ line goes low, the first character is transmitted serially. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

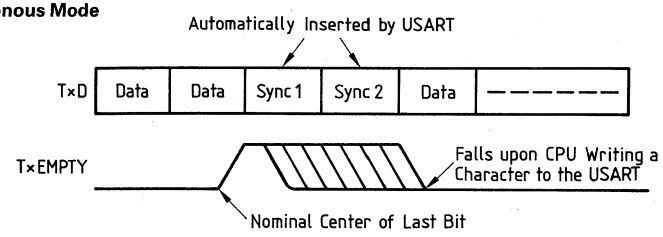
Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the SAB 82C51A with a data character before the SAB 82C51A's transmitter buffers become empty, the sync characters (or character if in single sync character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the SAB 82C51A is empty and sync characters are being sent out. TxEMPTY does not go low when the sync is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the SAB 82C51A.

Asynchronous Mode



1) If character length is defined as 5, 6 or 7 bits the unused bits are set to "zero".

Synchronous Mode

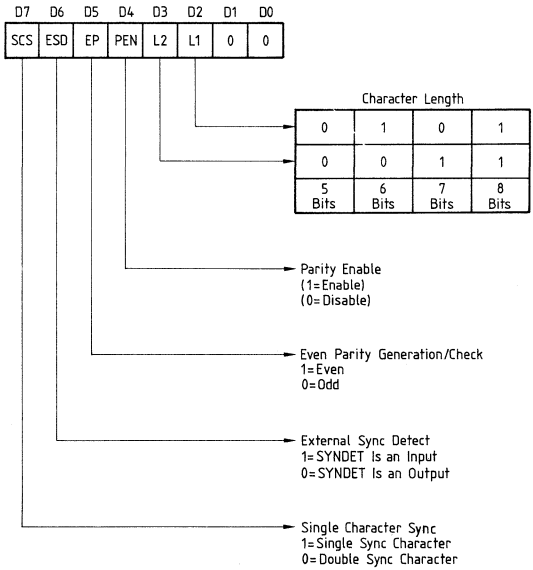


Synchronous Mode (receive)

In this mode, character synchronization can be achieved internally or externally. If the sync mode has been programmed, "enter hunt" command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of $\overline{RxC}$. The contents of the Rx buffer is compared at every bit boundary with the first sync character until a match occurs. If the SAB 82C51A has been programmed for two sync characters, the subsequently received character is also compared; when both sync characters have been detected, the USART ends the hunt mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a "status read". If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external sync mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the SAB 82C51A out of the hunt mode. The high level can be removed after one $\overline{RxC}$ cycle. An "enter hunt" command has no effect in the asynchronous mode of operation.

Mode Instruction Format, Synchronous Mode



Note:
In external sync mode, programming double character sync will affect only the Tx.

Parity error and overrun are both checked in the same way as in the asynchronous Rx mode. Parity is checked when not in hunt, regardless of whether the receiver is enabled or not.

The CPU can command the receiver to enter the hunt mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one", thus preventing a possible false SYNDET caused by data that happens to be in the Rx buffer at "enter hunt" time. Note that the SYNDET flipflop is reset at each status read, regardless of whether internal or external sync has been programmed. This does not cause the SAB 82C51A to return to the hunt mode. When in sync mode, but not in hunt, sync detection is still functional, but only occurs at the "known" word boundaries. Thus, if one status read indicates SYNDET and a second status read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous status read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication). When external SYNDET mode is selected, internal sync detect is disabled, and the SYNDET flipflop may be set at any bit boundary.

Command Instruction Definition

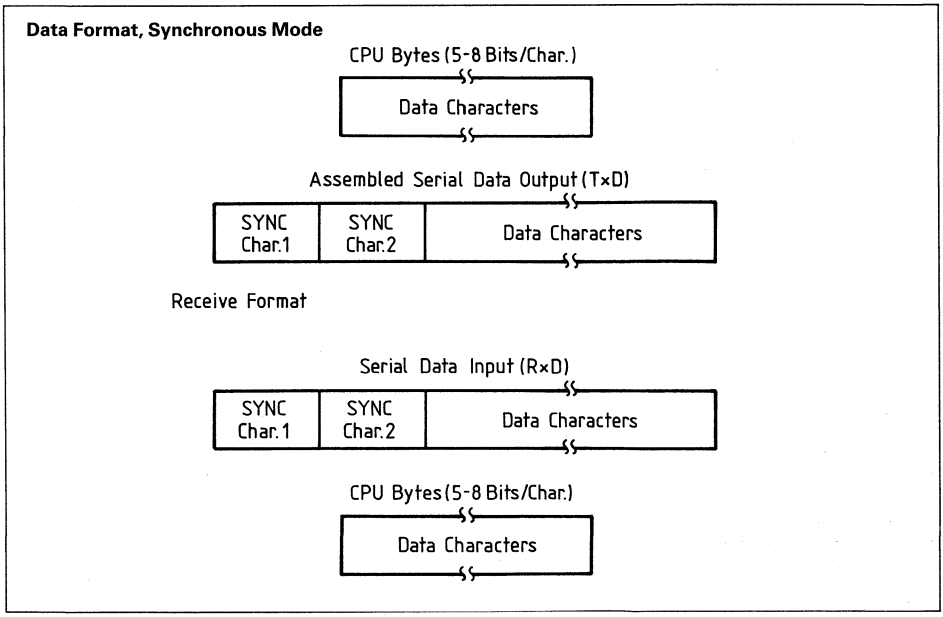
Once the functional definition of the SAB 82C51A has been programmed by the mode instruction and the sync characters are loaded (if in sync mode) then the device is ready to be used for data communication. The command instruction controls the actual operation of the selected format. Functions such as: enable transmit/receive, error reset and modem controls are provided by the command instruction.

Once the mode instruction has been written into the SAB 82C51A and sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D} = 1$) will load a command instruction. A reset operation (internal or external) will return the SAB 82C51A to the mode instruction format.

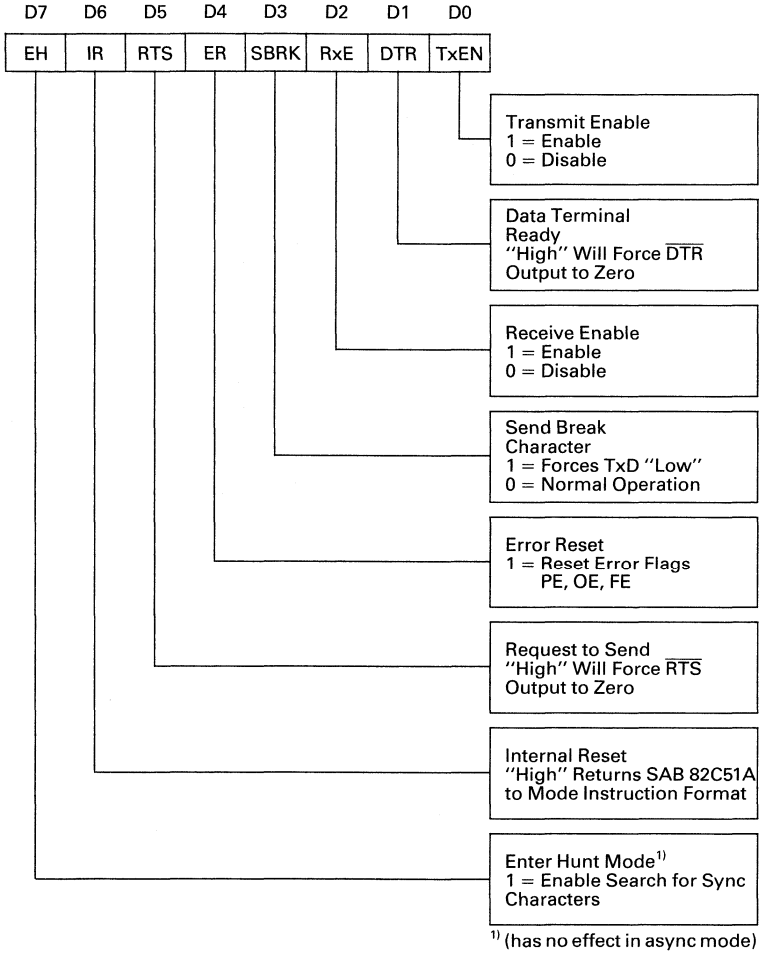
Note:
Internal reset on power-up:

When power is first applied, the SAB 82C51A may come up in the mode, sync character or command format. To guarantee that the device is in the command instruction format before the reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00Hs consecutively into the device with $C/\overline{D} = 1$ configures sync operation and writes two dummy 00H sync characters. An internal reset command (40H) may then be issued to return the device to the "idle" state.

Data Format, Synchronous Mode



Command Instruction Format



1) (has no effect in async mode)

Note: Error reset must be performed whenever RxEnable and "enter hunt" are programmed.

Status Read Definition

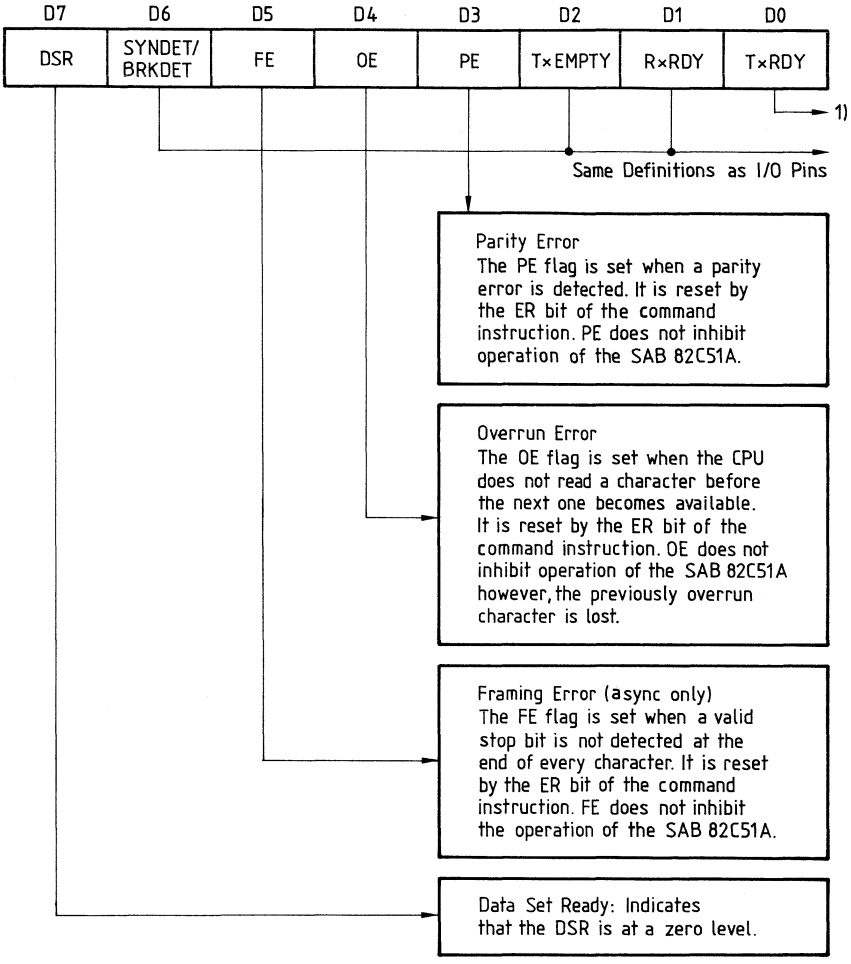
In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The SAB 82C51A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (Status update is inhibited during status read).

A normal "read" command is issued by the CPU with C/$\overline{D}$ = 1 to accomplish this function.

Some of the bits in the status read format have identical meanings to external output pins so that the SAB 82C51A can be used in a completely polled or interrupt-driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.

Status Read Format



Note:
TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN; the latter is conditioned by both $\overline{CTS}$ and TxEN.
i.e. TxRDY status bit = DB buffer empty

TxRDY pin out = DB buffer empty · ($\overline{CTS}$ = 0) · (TxEN = 1)

Absolute Maximum Ratings

Ambient temperature under bias	0°C to +70°C
Storage temperature	−65°C to +150°C
Supply voltage	−0.5 to +8.0 V
Operating voltage	4 V to 7 V
Voltage on any input	V_{SS} − 2 V to V_{CC} + 0.5 V
Voltage on any output	V_{SS} − 0.5 V to V_{CC} + 0.5 V
Power dissipation	1 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage	V_{IL}	−0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.4	V	I_{OL} = 2.5 mA
Output high voltage	V_{OH}	3.0 V_{CC} + 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
Output float leakage	I_{OFL}	–	±10	µA	V_{OUT} = V_{CC} to 0 V
Input leakage	I_{IL}	–	±1	µA	V_{IN} = V_{CC} to 0 V
Operating supply current	I_{CCO}	–	5	mA	Asynchronous x64 during transmitting/ receiving; outputs open
Standby supply current	I_{CCS}	–	100	µA	Input voltage at V_{CC} or GND level; outputs open

Capacitance

T_A = 25°C, V_{CC} = GND = 0 V

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input capacitance	C_{IN}	–	5	pF	f_C = 1 MHz
I/O capacitance	C_{IO}	–	20	pF	Unmeasured pins returned to GND

AC Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0V ±10%, GND = 0V

Bus Parameters [1]

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Read Cycle					
Address stable before $\overline{\text{READ}}$ ($\overline{\text{CS}}$, C/$\overline{\text{D}}$)	t_{AR}	0	–	ns	[2]
Address hold time for $\overline{\text{READ}}$ ($\overline{\text{CS}}$, C/$\overline{\text{D}}$)	t_{RA}	0	–	ns	[2]
$\overline{\text{READ}}$ pulse width	t_{RR}	150	–	ns	–
Data delay from $\overline{\text{READ}}$	t_{RD}	–	140	ns	[3] C_L = 150 pF
$\overline{\text{READ}}$ to data floating	t_{DF}	10	50	ns	–
Write Cycle					
Address stable before $\overline{\text{WRITE}}$	t_{AW}	0	–	ns	–
Address hold time for $\overline{\text{WRITE}}$	t_{WA}	0	–	ns	–
$\overline{\text{WRITE}}$ pulse width	t_{WW}	150	–	ns	–
Data setup time for $\overline{\text{WRITE}}$	t_{DW}	80	–	ns	–
Data hold time for $\overline{\text{WRITE}}$	t_{WD}	10	–	ns	–
Recovery time between writes	t_{RV}	6	–	t_{CY}	[4]
Reset pulse width	t_{RESW}	6	–	t_{CY}	[6]

[1] AC timings are measured at V_{OH} = 2.0 V and V_{OL} = 0.8 V with 150 pF capacitance load.

[2] Chip select ($\overline{\text{CS}}$) and command/data (C/$\overline{\text{D}}$) are considered as addresses.

[3] Assumes that address is valid before $\overline{\text{RD}}\downarrow$.

[4] This recovery time is for mode initialization only. Write data is allowed only when TxRDY = 1. Recovery time between writes for asynchronous mode is 8 t_{CY} and for synchronous mode is 16 t_{CY}.

[5] The TxC and RxC frequencies have the following limitations with respect to CLK: For 1x baud rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$. For 16x and 64x baud rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$.

[6] System clock must be running during reset.

[7] Status update can have a maximum delay of 28 clock periods from the event affecting the status.

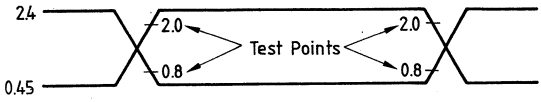
Other Timings

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Clock period	t_{CY}	125	–	ns	5) 6)
Clock high pulse width	t_{CH}	50	–	ns	–
Clock low pulse width	t_{CL}	35	–	ns	–
Clock rise and fall time	t_R, t_F	–	20	ns	–
TxD delay from falling edge of $\overline{TxC}$	t_{DTx}	–	0.5	µs	–
Transmitter input clock frequency 1x baud rate 16x baud rate 64x baud rate	f_{Tx}	 DC DC DC	 240 1536 1536	 kHz kHz kHz	–
Transmitter input clock pulse width 1x baud rate 16x and 64x baud rate	t_{TPW}	 12 1	 – –	 t_{CY} t_{CY}	 – –
Transmitter input clock pulse delay 1x baud rate 16x and 64x baud rate	t_{TPD}	 15 3	 – –	 t_{CY} t_{CY}	 – –
Receiver input clock frequency 1x baud rate 16x baud rate 64x baud rate	f_{Rx}	 DC DC DC	 240 1536 1536	 kHz kHz kHz	 – – –
Receiver input clock pulse width 1x baud rate 16x and 64x baud rate	t_{RPW}	 12 1	 – –	 t_{CY} t_{CY}	 – –
Receiver input clock pulse delay 1x baud rate 16x and 64x baud rate	t_{RPD}	 15 3	 – –	 t_{CY} t_{CY}	 – –
TxRDY pin delay from center of last bit	t_{TxRDY}	–	8	t_{CY}	7)
TxRDY ↓ from leading edge of $\overline{WR}$	$t_{xRDY\ CLEAR}$	–	400	ns	7)
RxRDY pin delay from center of last bit	t_{RxRDY}	–	26	t_{CY}	7)
RxRDY ↓ from leading edge of $\overline{RD}$	$t_{RxRDY\ CLEAR}$	–	200	ns	7)
Internal SYNDET delay from rising edge of $\overline{RxC}$	t_{IS}	–	26	t_{CY}	7)
External SYNDET setup time after rising edge of $\overline{RxC}$	t_{ES}	16	–	t_{CY}	7)
TxEMPTY delay from center of last bit	$t_{TxEMPTY}$	–	20	t_{CY}	7)
Control delay from rising edge of write (TxEn, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}	–	8	t_{CY}	7)
Control to read setup time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	20	–	t_{CY}	7)
RxD setup time for rising edge of $\overline{RxC}$ (1x baud)	t_{RxDS}	11	–	t_{CY}	–
RxD hold time for falling edge of $\overline{RxC}$ (1x baud)	t_{RxDH}	17	–	t_{CY}	–

For notes refer to page 15.

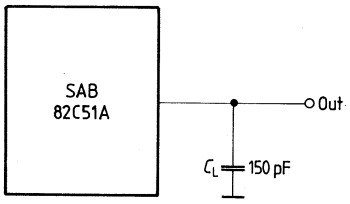
AC Testing

Input/Output Waveform



AC testing: Inputs are driven at 2.4V for a logic "1" and at 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and at 0.8V for a logic "0".

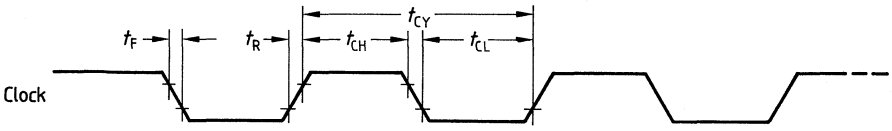
Load Circuit



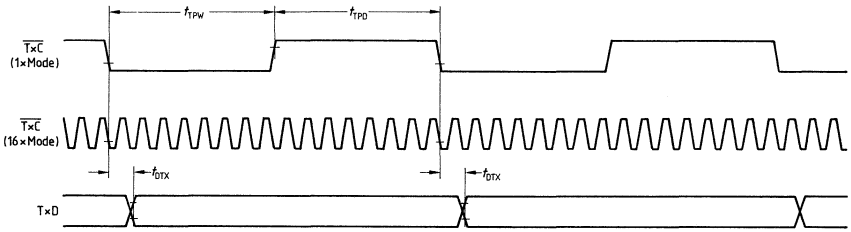
C_L = 150 pF

Waveforms

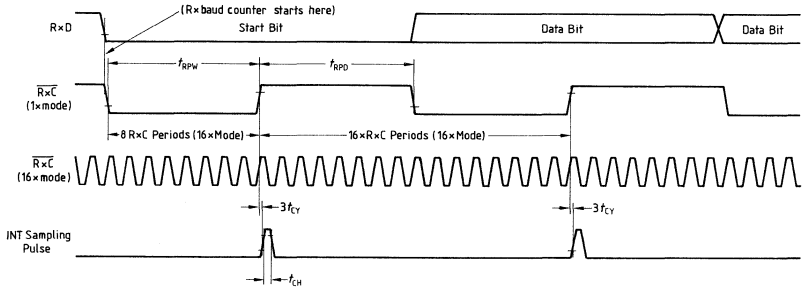
System Clock Input



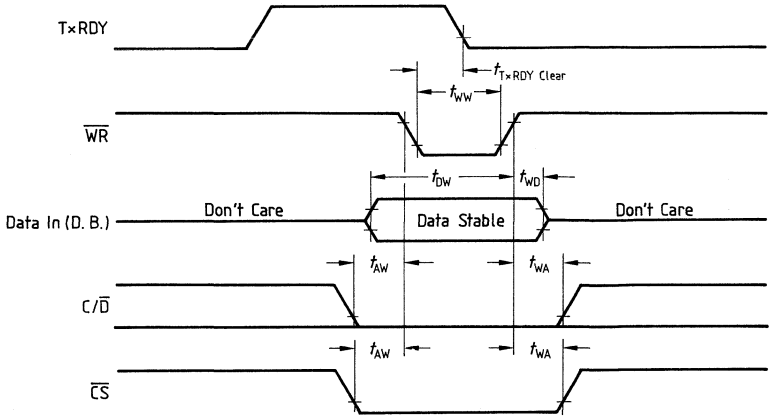
Transmitter Clock and Data



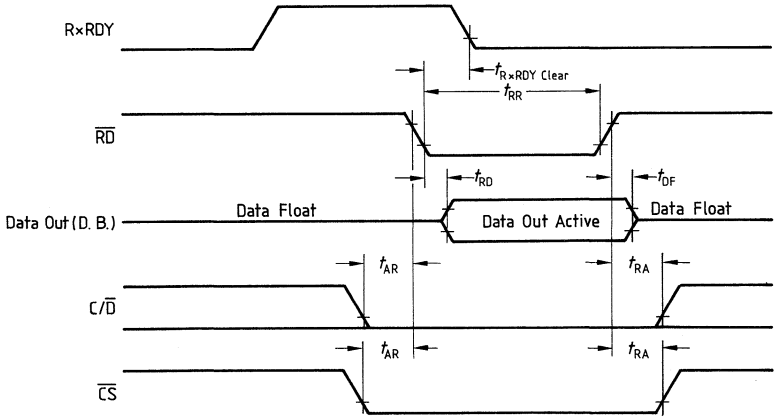
Receiver Clock and Data



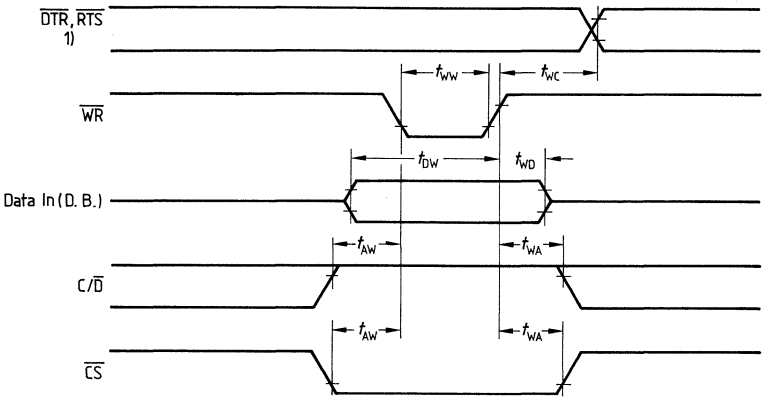
Write Data Cycle (CPU → USART)



Read Data Cycle (CPU ← USART)

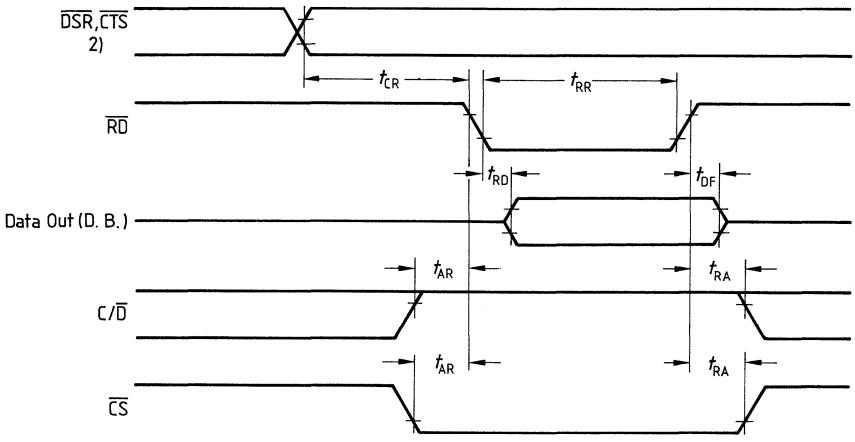


Write Control or Output Port Cycle (CPU → USART)



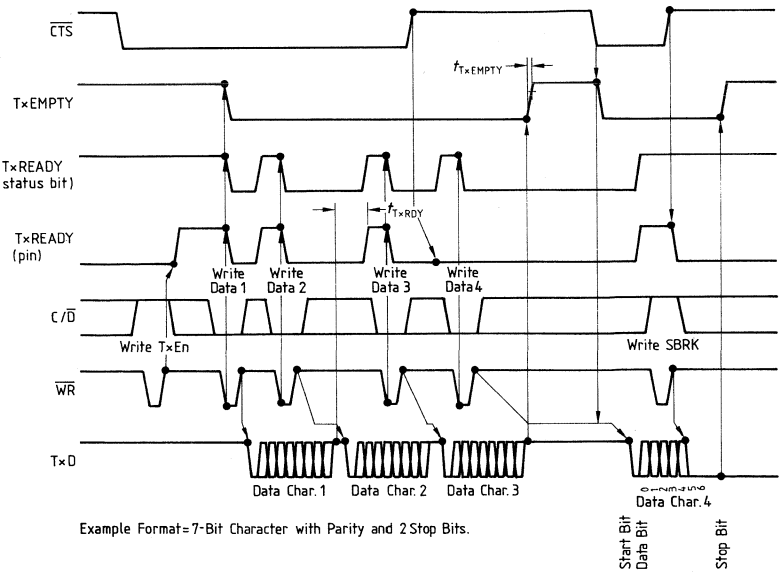
1) t_{WC} Includes the Response Timing of a Control Byte.

Read Control or Input Port (CPU ← USART)



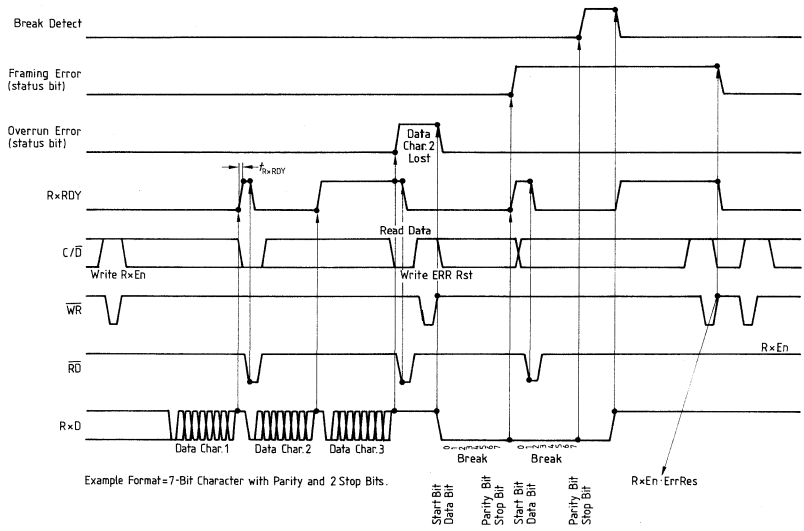
2) t_{CR} Includes the Effect of CTS on the T×ENBL Circuitry.

Transmitter Control and Flag Timing (Async Mode)

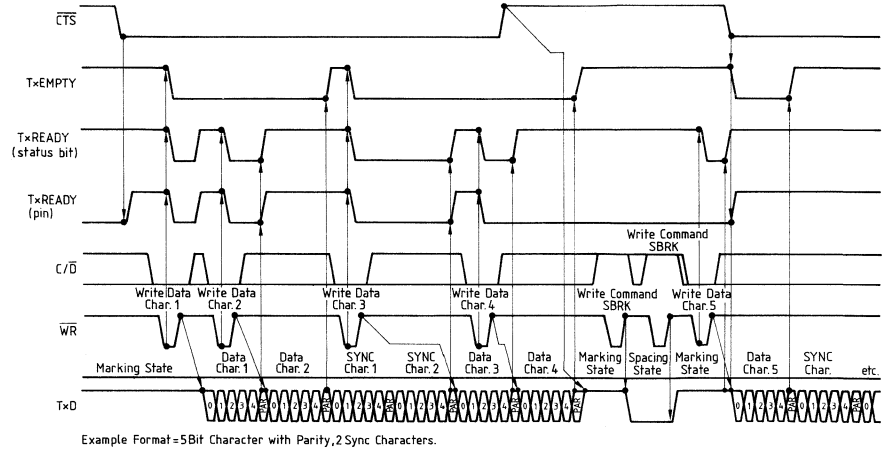


Example Format = 7-Bit Character with Parity and 2 Stop Bits.

Receiver Control and Flag Timing (Async Mode)

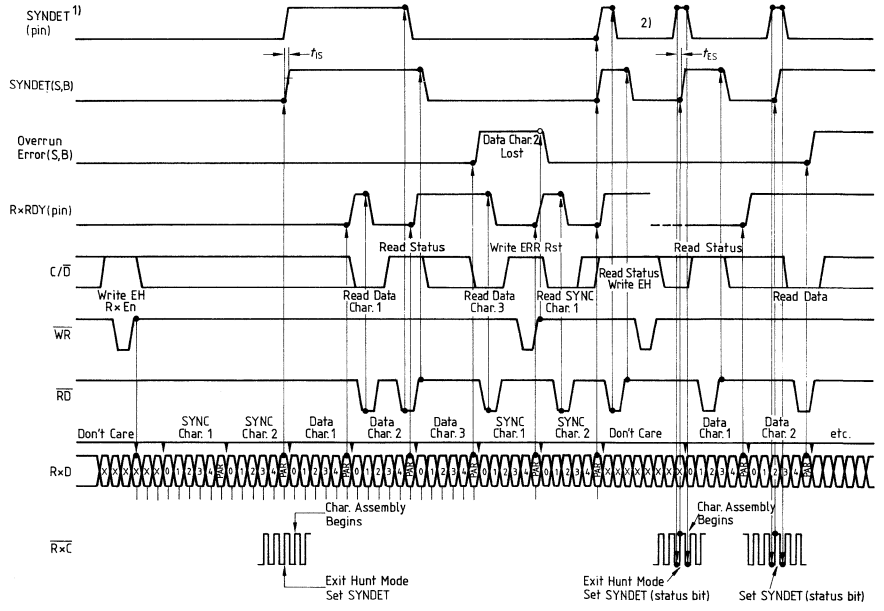


Transmitter Control and Flag Timing (Sync Mode)



Example Format = 5 Bit Character with Parity, 2 Sync Characters.

Receiver Control and Flag Timing (Sync Mode)



Ordering Information

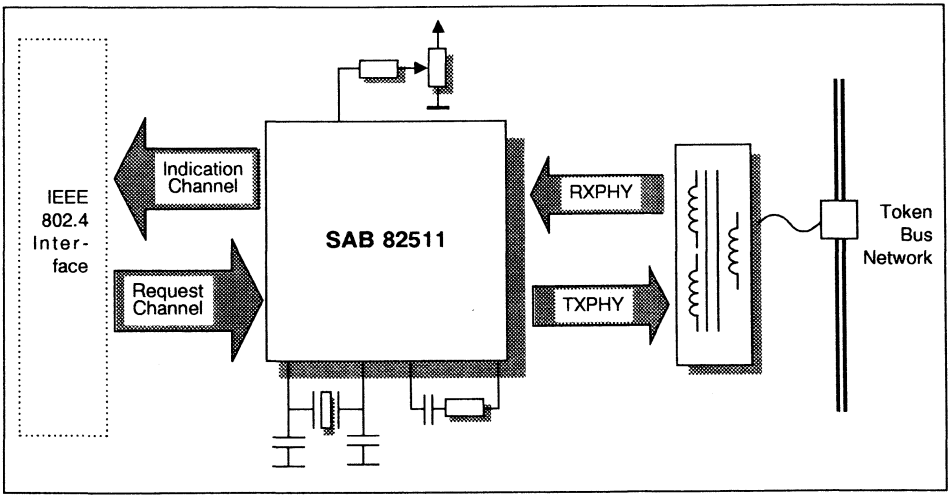
Type	Ordering code	Description
SAB 82C51A-P	Q67120-P216	Programmable communications interface

SIEMENS

Token Bus Modem (TBM) SAB 82511

Advanced Information

- Carrier-band modem fully compatible with IEEE 802.4 and MAP Standard
- 5 and 10 Mbit/s data rate using phase-coherent FSK modulation
- Digital PLL and digital demodulation
- Diagnostic loop-back for test purposes
- Provides physical station management
- Jabber inhibit timer (watchdog)
- Differential input/output drivers to serial line
- No active external components
- Advanced Siemens oxid-isolated bipolar technology
- Single +5 V power supply



The token bus modem is designed to work directly with a token bus controller in IEEE 802.4 token bus applications. It uses phase-coherent frequency shift keying modulation at a data rate of 5 Mbit/s and 10 Mbit/s.
The major functions of the modem are to generate the receive and transmit clock, modulate and demodulate (frequency shift keying) and provide the electrical interface to the transceiver cable.

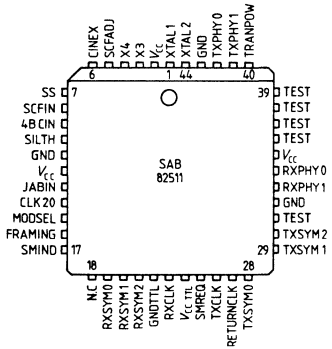
Diagnostic loop-back control enables the modem to route the signal to be transmitted from the token bus controller through the encoding and decoding circuitry and back to the token bus controller. The combined loop-back capabilities of the token bus controller and the token bus modem result in efficient fault detection. An on-chip failsafe watchdog timer circuit prevents the station from locking up in continuous transmit mode.

Ordering Information

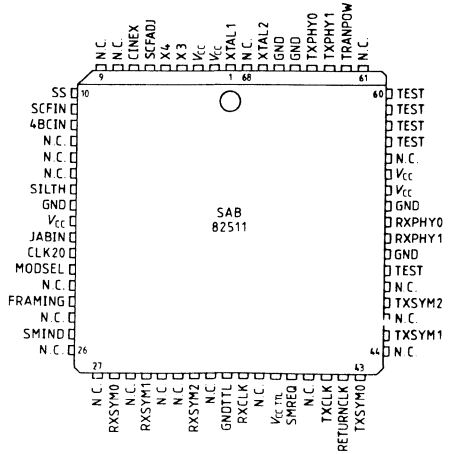
Type	Ordering code	Package	Description
SAB 82511-5-N	Q67020-P51	PL-CC-44	Token bus modem
SAB 82511-1-N	Q67020-P55	PL-CC-44	Token bus modem
SAB 82511-5-NE	Q67020-P57	PL-CC-68	Token bus modem
SAB 82511-1-NE	Q67020-P58	PL-CC-68	Token bus modem

Pin Configurations

PL-CC-44



PL-CC-68



Pin Definitions and Functions

The modem pins are divided into six functional groups:

- Request Channel
- Indication Channel
- Medium Interface
- Operational Mode Selection
- External Clocking
- Power Supply and External Components

All TTL inputs are driven high by internal pullups if not connected.

Symbol	Pin PL-CC-44	Pin PL-CC-68	Input (I) Output (O)	Function
Request Channel				
SMREQ	25	39	I	Selects either MAC mode or Station Management mode (MAC mode = 1)
TXSYM2 TXSYM1 TXSYM0	30 29 28	47 45 43	I	Encoded MAC-symbols for transmission or Station Management requests
TXCLK	26	41	O	Transmit clock provided by the modem (5 MHz or 10 MHz)
RETURNCLK	27	42	I	Transmit clock derived from TXCLK
Indication Channel				
SMIND	17	25	O	Indicates either MAC mode or Station Management mode (MAC mode = 1)
RXSYM2 RXSYM1 RXSYM0	21 20 19	33 30 28	O	Encoded MAC-symbols for reception or Station Management indications and confirmations
RXCLK	23	36	O	Receive clock provided by the modem (5 MHz or 10 MHz)
Medium Interface				
RXPHY0 RXPHY1	34 33	52 51	I	Differential receiver input lines from the medium transformer
TXPHY0 TXPHY1	42 41	64 63	O	Differential transmitter output lines to the medium transformer

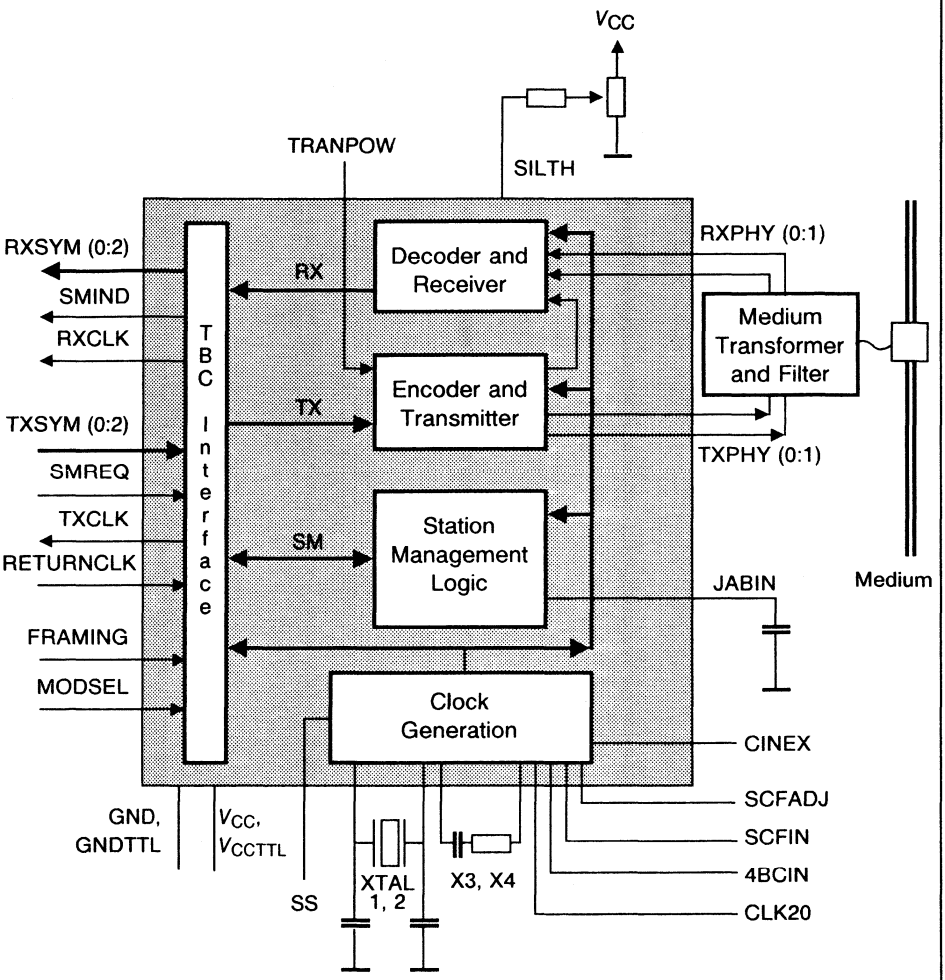
Pin Definitions and Functions (cont'd)

Symbol	Pin PL-CC-44	Pin PL-CC-68	Input (I) Output (O)	Function
Operational Mode Selection				
MODSEL	15	21	I	Enables modem to react to MAC and Station Management requests (Enable: MODSEL = 1). If the modem is disabled (MODSEL = 0) it transmits silence. The indication channel is not influenced by the MODSEL-pin
SS	7	10	I	Selects data rate (10 MHz : SS = 1)
FRAMING	16	23	I	If FRAMING is low the modem will react to MAC and Station Management requests. If FRAMING is high the modem will transmit and indicate silence whatever is requested or received
External Clocking				
CINEX	6	7	I	Selects internal or external clock generator. If CINEX is high, the external clock must be supplied at SCFIN and 4BCIN. If low, the internal clock generator is used, and the SCFIN and 4BCIN-pin should be left open
SCFADJ	5	6	I	Adjusts the asynchronous internal clock, if CINEX is low
SCFIN	8	11	I	External asynchronous clock must be supplied, if CINEX is high. The clock frequency has to be between 16.016 and 16.080 times of the wanted bit frequency
CLK20	14	20	O	20 MHz TTL output of internal clock generator
4BCIN	9	12	I	External clock of 4 times the wanted bit frequency must be supplied, if CINEX is high (tolerance ± 0.01 %)

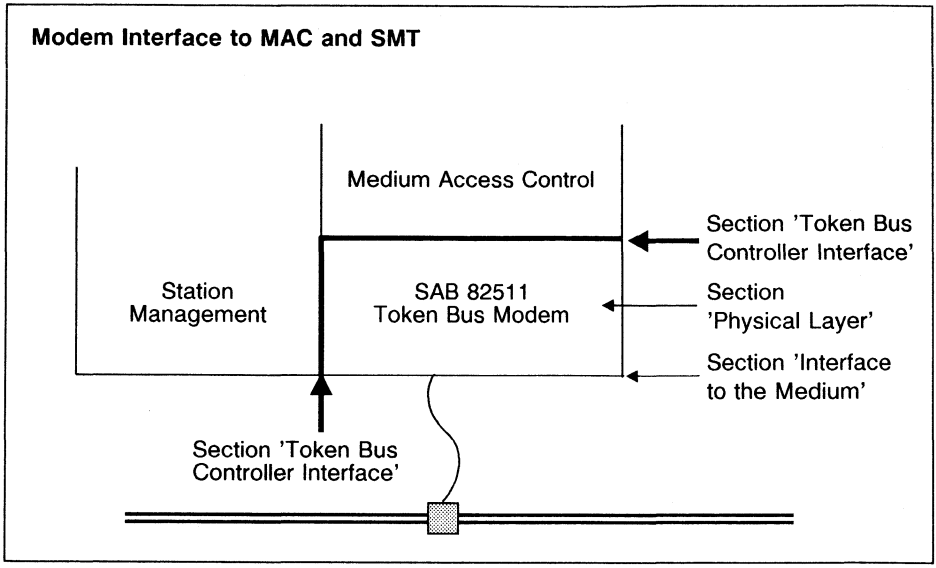
Pin Definitions and Functions (cont'd)

Symbol	Pin PL-CC-44	Pin PL-CC-68	Input (I) Output (O)	Function
Power Supply and External Components				
SILTH	10	16	I	Silence Threshold. This pin isused to adjust the threshold of silence recognition with a resistor
XTAL1 XTAL2	1 44	1 67	I	Connect 20 MHz crystal to use internal clock generator. Instead an external 20 MHz clock can be AC-coupled to XTAL2
X3 X4	3 4	4 5	I	Connect external capacitor and resistor for internal clock generator operation
JABIN	13	19	I	Connect external capacitor to ground to define JABBER INHIBIT time
TRANPOW	40	62	I	Adjusts transmitter output level
V_{CC}	2, 12, 35	2, 3, 18, 54, 55	–	+5 V power supply for digital logic and output drivers
V_{CCTTL}	24	38	–	+5 V power supply for TTL logic
GND	11, 32, 43	17, 50, 53, 65, 66	–	Circuit ground
GNDTTL	22	35	–	TTL ground potential
TEST	31, 36, 37, 38, 39	49, 57,58, 59, 60	–	These pins are reserved an must be left open. No connections are allowed
NC	18	8, 9, 13, 14, 15, 22, 24, 26, 27, 29, 31, 32, 34, 37, 40, 44, 46, 48, 56, 61, 68	–	Not connected internal

Block Diagram



Token Bus Controller Interface



The interface (see figure above) provides the means for transferring information between the modem and the medium access control (MAC) and between the modem and the station management. In the interest of minimizing the number of signal lines, the station management uses the same lines as the MAC to access the modem. The interface supports three primary functions as described below:

Request Channel MAC Mode

The MAC mode is selected when SMREQ = 1 and is considered "normal" operation. The MAC defines 5 symbols for transmission: silence, non-data, one, zero and pad-idle (see next table). The MAC sends these symbols on lines TXSYM0, TXSYM1 and TXSYM2 to the modem. The modem modulates its transmit carrier signal accordingly. These requests are synchronized to RETURNCLK.

MAC request symbol encoding

	SMREQ	TXSYM2	TXSYM1	TXSYM0
Silence	1	1	1	Don't Care
Non-Data	1	1	0	Don't Care
Pad-Idle	1	0	1	Don't Care
One	1	0	0	1
Zero	1	0	0	0

Indication Channel MAC Mode

The MAC mode is indicated by SMIND = 1. The MAC defines 5 symbols for data reception: silence, non-data, bad-signal, one and zero (see next table). The modem reports these symbols on lines RXSYM0 – RXSYM2 to the MAC, synchronized to RXCLK.

MAC indication symbol encoding

	SMIND	RXSYM2	RXSYM1	RXSYM0
Silence	1	1	1	X
Non-Data	1	1	0	X
Bad-Signal	1	0	1	X
One	1	0	0	1
Zero	1	0	0	0

X = either 0 or 1

Physical Layer Management

The request channel and the indication channel serve a second purpose which is to pass station management requests to the modem and to pass station management confirmations and indications to the station management.
Serial commands are not supported.

Management Request

The management mode is selected by SMREQ = 0. The request channel is used by the station management to send station management requests to the modem (for encoding see table below).
The modem must be enabled by MODSEL. All unused commands are not supported.

Note: The transmitter is disabled whenever the modem is in management mode.

Management request encoding

	SMREQ	TXSYM2	TXSYM1	TXSYM0
RESET	0	1	1	1
LOOP-BACK DISABLE	0	1	0	1
ENABLE TRANSMITTER	0	0	1	1
IDLE/SERIAL DATA	0	0	0	*)

*) TXSYM0 contains a start bit, eight data bits and a stop bit, when the MAC issues a SERIAL DATA command. Otherwise, TXSYM0 = 1.

RESET initiates the modem, disables the transmitter and enables the loop-back.

LOOP-BACK DISABLE disables the loop-back at the point closest to the cable between TXPHY and RXPHY.

ENABLE TRANSMITTER switches the transmission path from TXSYM0 – TXSYM2 to the differential output lines to the medium.

IDLE indicates that the MAC layer is waiting.

Management Indication/Confirmation

The management mode is indicated by SMIND = 0. The indication channel is used by the modem to send responses (confirmations) to management commands and to indicate modem fault (PHYSICAL ERROR indication).

The table below shows the encoding for the indication channel management mode. Use of the signal lines is described below.

Management indication/confirmation encoding

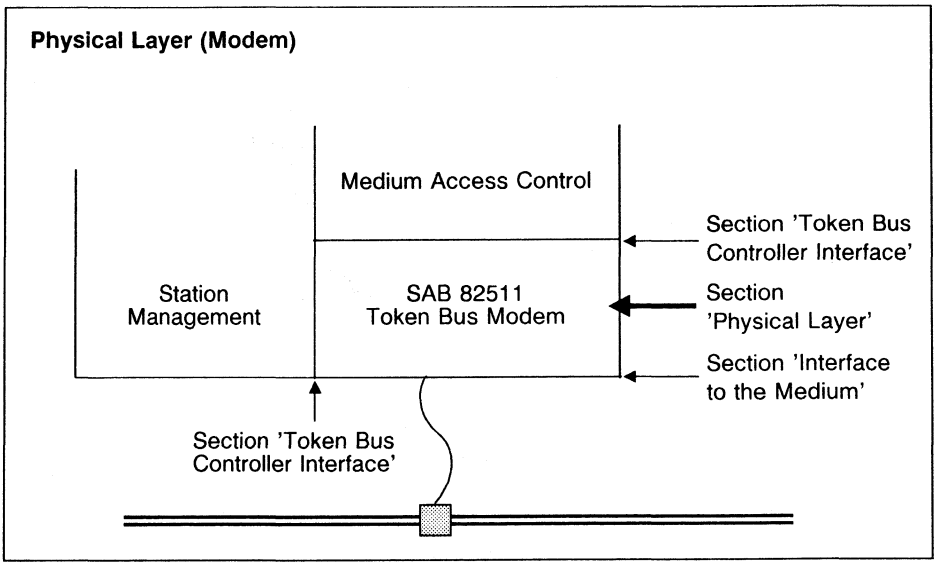
	SMIND	RXSYM2	RXSYM1	RXSYM0
NAK (non-acknowledgement)	0	1	0	*)
ACK (acknowledgement)	0	0	1	1
IDLE	0	0	0	1
PHYSICAL ERROR	0	1	1	1

*) RXSYM0 contains a start bit, "don't care" data and a stop bit, when responding to a serial data command. Otherwise, RXSYM0 = 1.

Management mode (SMIND = 0) is entered in response to SMREQ = 0 as confirmation that the modem has gone to management mode.

Management mode is also entered as a result of a PHYSICAL ERROR condition (indication). For the first case, the modem will enter the management mode (SMIND = 0) after SMREQ goes low and will leave the management mode when SMREQ goes high. For the second case, the modem will enter the management mode and stay there until the station management corrects the error and leaves the management mode.

Physical Layer



Symbol Encoding

When in the MAC mode, the modem transmits symbols received at its MAC interface to the medium. Each of these MAC symbols is encoded into a pair of PHY symbols out of a three-symbol (H), (L), (off) code and then transmitted. The encoding for each of the input MAC symbols is:

(1) Silence Each silence symbol is encoded as the sequence (off off).

(2) Pad-Idle Successive pad-idle symbols are encoded as an alternating series of (LL) and (HH).

(3) Zero Each zero symbol is encoded as the sequence (HH).

(4) One Each one symbol is encoded as the sequence (LL).

(5) Non-Data Non-Data symbols are transmitted by the MAC in pairs. Each such pair of consecutive non-data symbols is encoded as the sequence (HL, LH).

Line Signal (at the line output of the modem)

The PHY symbols resulting from the symbol encoding are converted directly to their line representation, as described below, and the resulting signaling is AC-coupled to the single channel phase-coherent FSK bus medium. The modem is able to receive signals of either polarity.

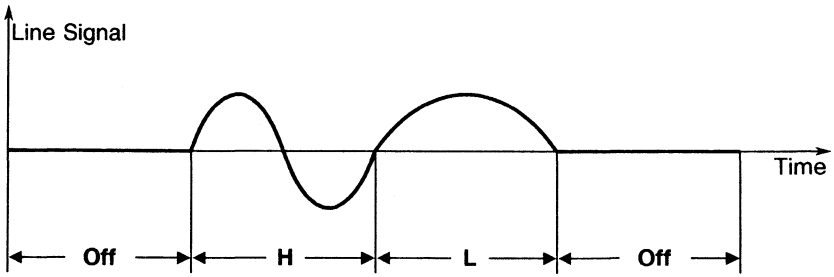
The line signal representation of the (H), (L) and (off) PHY symbols is as follows (see also figure below):

(1) An (H) is represented as one full cycle of a signal starting and ending with a nominal zero amplitude, the period of which is equal to half the period of MAC symbol delivery to the MAC entity at the MAC interface.

(2) An (L) is represented as one half cycle of a signal, starting and ending with a nominal zero amplitude, the period of which is equal to the period of MAC symbol delivery to the MAC entity at the MAC interface, with the phase of the representing half cycle changing at each successive (L).

(3) An (off) is represented by no signal for a period equal to one half of the period of MAC symbol delivery to the MAC entity at the MAC interface.

Symbolic Line Signal Representation

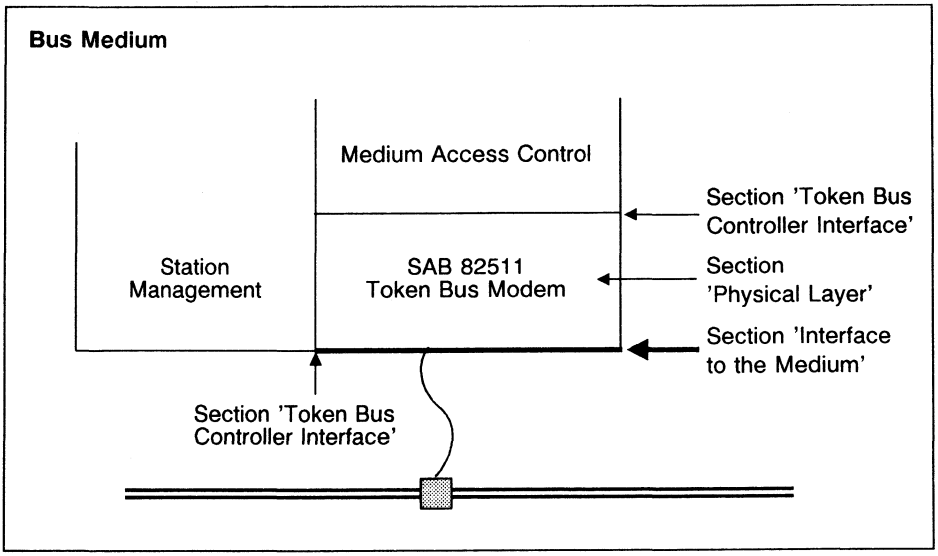


The maximum jitter in the period of any (L) or half-cycle of any (H) is not more than ±1 percent of the MAC symbol period.
The next table summarizes the relationship of data rate and signaling frequencies.

Data Rate vs. Signaling Frequencies

Data Rate (Mbps)	Frequency of Lower Tone (MHz)	Frequency of Higher Tone (MHz)
5	5.0	10.0
10	10.0	20.0

Interface to the Medium



All measurements specified in the following paragraphs are to be made at the point of station or regenerative repeater connection to the medium. Unless otherwise stated, all voltage and power levels specified are in rms and dB (1 mV, 75 Ω) [dBmV] rms, respectively, based on measuring the fundamental signal content of continuous transmissions of all 'one' or all 'zero' symbols.

Coupling to the Medium

The connection of the single-channel phase-coherent FSK bus medium to the station should be a flexible 75 Ω drop cable terminated in a male F-series 75 Ω connector; this combination shall match with a female F-series 75 Ω connector mounted on the station. In addition to this coupling, the shield(s) of the coaxial drop cable medium shall be connected to the shell of the terminating male connector and the DC impedance of that connection shall be less than 0.1 Ω. Also the DC impedance of a connection between the shell of that male connector and the outer barrel of a mated female connector shall be less than 0.1 Ω.

Characteristic Impedance

The characteristic impedance of the single-channel phase-coherent FSK bus medium shall be 75 ± 3 Ω. The physical medium shall present an impedance to the station resulting in a VSWR of 1.5:1 or less when driven from a 75 Ω source over the operating frequency range.

Signal Level

When receiving the signal of a single station or regenerative repeater the single channel phase-coherent FSK bus medium shall present that signaling to the connected station or regenerative repeater at an amplitude between +10 dB and +66 dB (1 mV, 75 Ω) [dBmV] for a 5 Mbit/s data rate and a 10 Mbit/s data rate.
The signal strength of the two fundamental signaling frequencies due to media attenuation (corresponding to the data rate and twice the data rate) at any receiving station shall vary by no more than 3.5 dB.

Note: This is equivalent to the cable tilt found on 600 meters of foam dielectric RG-11 type cable with 2 dB / 100 m of attenuation at 10 MHz.

Absolute Maximum Ratings

Ambient temperature under bias	PL-CC-44 (static air)	0 to 55 °C
	PL-CC-44 (moving air 1 m/s)	0 to 70 °C
	PL-CC-68 (static air)	0 to 70 °C
	PL-CC-68 (moving air 1 m/s)	0 to 85 °C
Storage temperature under bias		– 65 to + 150 °C
All TTL output and supply voltages		– 0.5 to V_{CC} + 0.5 V
All Input voltages		– 0.5 to + 5.5 V

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

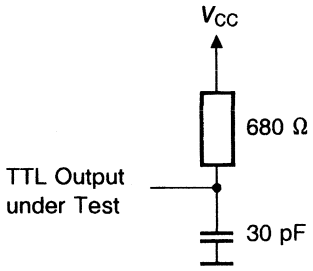
DC Characteristics for TTL Voltages

V_{CC} = + 5 V ± 5 %

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage	V_{IL}	–	0.8	V	
Input high voltage	V_{IH}	2.0	–	V	
Output low voltage	V_{OL}	–	0.5	V	at 8 mA 1)
Output high voltage	V_{OH}	2.5	–	V	at – 1.0 mA
Output low current	I_{OL}	–	4	mA	1)
Input clamp voltage	V_C	– 1.0	–	V	I_C = – 5 mA
Input low current	I_{IL}	–	– 2	mA	at V_{IL} = 0.5 V
Input high current	I_{IH}	–	50	µA	at V_{IH} = 2.7 V
Power supply current Transmitter off	I_{CC}	–	370	mA	
Foreward input current	I_F	–	– 2	mA	V_F = 0.45 V
Reverse input current	I_R	–	50	µA	V_R = V_{CC} + 0.3 V
Output off current	I_{OFF}	–	I_F	–	V_{OFF} = 0.45 V
Output off current	I_{OFF}	–	I_R	–	V_{OFF} = V_{CC} + 0.3 V
Input capacitance	C_{IN}	–	10	pF	f = 1 MHz V_{CC} = 5 V T_A = 25 °C V_{BIAS} = 2.5 V

1) Pin CLK20 at 2 mA.

TTL Output Test Load Circuit



AC Characteristics

V_{CC} = +5 V ±5 %

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCE / DTE Interface (5 Mbit/s)					
RXCLK period	t_{60a}	180	200	220	ns
TXCLK period	t_{60b}	180	200	220	ns
RXCLK sum of 3 periods	t_{61}	540	600	660	ns
RXCLK/TXCLK low time	t_{62}	80	100	120	ns
RXCLK/TXCLK high time	t_{63}	80	100	120	ns
RXCLK/TXCLK rise/fall time (10 % - 90 %)	t_{64}	–	–	10	ns
RETURNCLK/TXSYM/SMREQ setup time	t_{65}	70	–	–	ns
RETURNCLK/TXSYM/SMREQ hold time	t_{66}	10	–	–	ns
RXSYM/SMIND setup time to RXCLK	t_{67}	80	–	–	ns
RXSYM/SMIND hold time from RXCLK	t_{68}	10	–	–	ns
RXCLK period when reporting silence or bad signal	t_{60}	180	–	420	ns
RXCLK sum of 3 periods during synchronization	t_{61}	540	–	860	ns
RXCLK low time during synchronization	t_{62}	80	–	340	ns
RXCLK high time during synchronization	t_{63}	80	–	340	ns

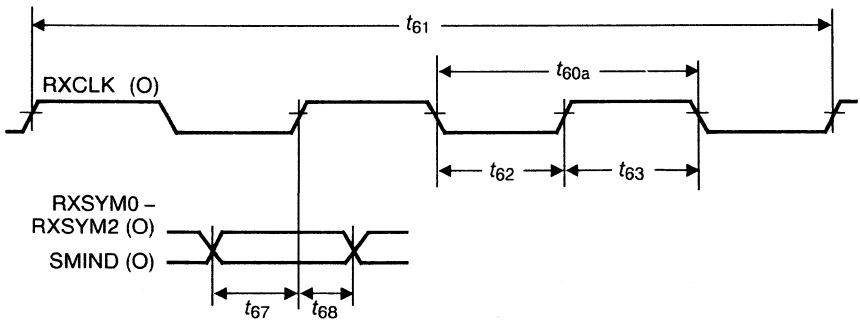
AC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCE / DTE Interface (10 Mbit/s)					
RXCLK period	t_{60a}	90	100	110	ns
TXCLK period	t_{60b}	90	100	110	ns
RXCLK sum of 3 periods	t_{61}	270	300	330	ns
RXCLK/TXCLK low time	t_{62}	40	50	60	ns
RXCLK/TXCLK high time	t_{63}	40	50	60	ns
RXCLK/TXCLK rise/fall time (10 % - 90 %)	t_{64}	–	–	10	ns
RETURNCLK/TXSYM/SMREQ setup time	t_{65}	35	–	–	ns
RETURNCLK/TXSYM/SMREQ hold time	t_{66}	10	–	–	ns
RXSYM/SMIND setup time to RXCLK	t_{67}	40	–	–	ns
RXSYM/SMIND hold time from RXCLK	t_{68}	10	–	–	ns
RXCLK period when reporting silence or bad signal	t_{60}	90	–	210	ns
RXCLK sum of 3 periods during synchronization	t_{61}	270	–	430	ns
RXCLK low time during synchronization	t_{62}	40	–	170	ns
RXCLK high time during synchronization	t_{63}	40	–	170	ns

Receiver Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input voltage at RXPHY0 and RXPHY1	V_I	GND	–	V_{CC}	–
Input power for normal receive operation	P_I	10	–	67.5	dBmV
Receiver input capacitance	C_I	–	–	5	pF
Receiver input impedance (within receive band)	$\|Z_I\|$	–	1	–	kΩ
Transmitter output capacitance	C_T	–	–	12	pF
Signal/noise ratio for normal receive operation	SNR	20	–	–	dB

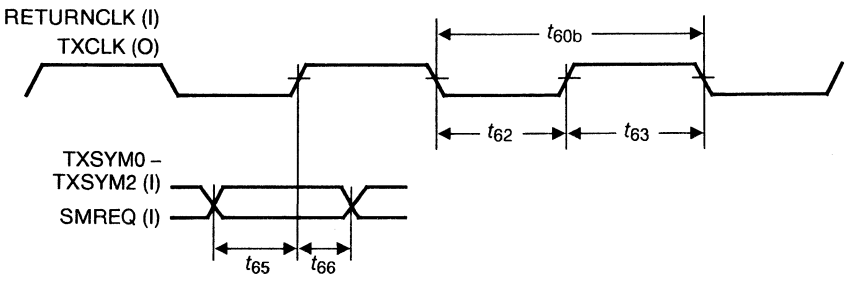
Receive Timing



Transmitter Characteristics

Parameter		Symbol	Limit Values			Unit
			min.	typ.	max.	
Output voltage at TXPHY0 and TXPHY1		V_O	V_{CC} – 2.8	–	V_{CC} + 2.8	V
Output current for transmit operation		I_O	52	–	70	mA
Output power for transmit operation	2)	P_O	63	–	67.5	dBmV
Output current rise time (10 % - 90 %)	3)	t_r	4	–	–	ns
Output current fall time (10 % - 90 %)	3)	t_f	4	–	–	ns

Transmit Timing



2) Adjustable with TRANPOW pin.

3) Thus value is measured at a transmitter output pin, with an ohmic load of 37,5 Ω to V_{CC}. The value will be increased by the use of a transformer and the filters circuitry.

Preliminary

SAB 82C53 Programmable CMOS Interval Timer

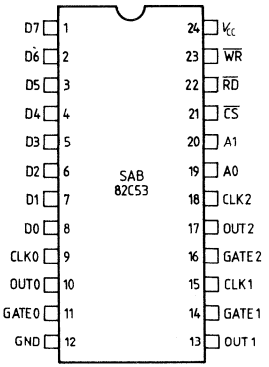
SAB 82C53: Command Width 400 ns

- Compatible with all Siemens and most other microprocessors
- Three independent 16-bit counters
- Handles inputs from DC to 2.6 MHz
- Low-power CMOS (I_{CC} = 10 mA at max. count frequency)

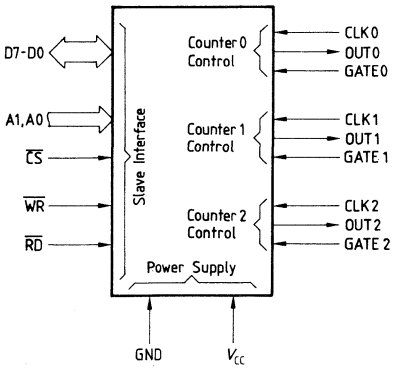
SAB 82C53-5: Command Width 300 ns

- Completely TTL compatible
- Six programmable counter modes
- Binary or BCD counting
- 24-pin plastic dual-in-line package, P-DIP-24

Pin Configuration



Logic Symbol



The SAB 82C53 is a high-performance, CMOS version of the industry standard 8253 timer/counter which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 2.6 MHz. All modes are software-programmable. The SAB 82C53 is pin-compatible with the NMOS 8253, and is a subset of the SAB 82C54.

Six programmable timer modes allow the SAB 82C53 to be used as an event counter, elapsed time indicator, programmable monoflop, and in many other applications.

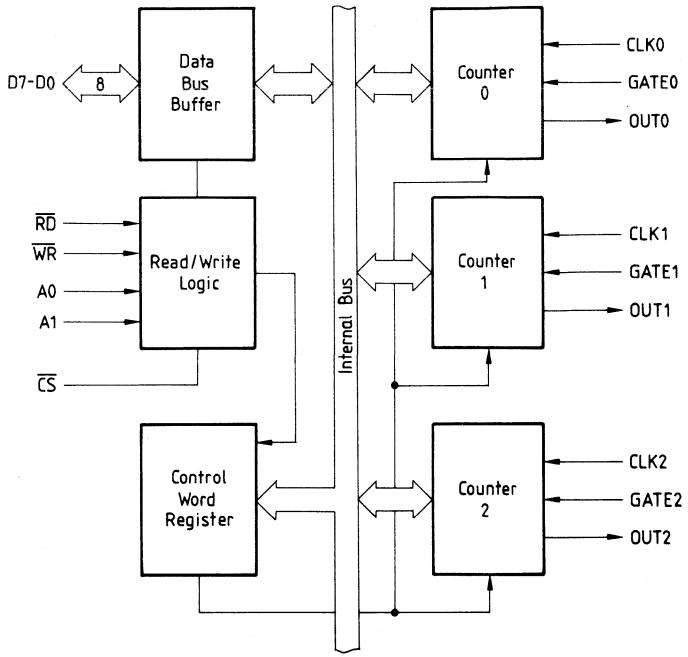
The SAB 82C53 is fabricated in Siemens advanced CMOS technology which provides low power consumption and is packaged in a 24-pin plastic dual-in-line package, P-DIP-24.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
D7-D0	1-8	I/O	DATA 7-0 Bidirectional tristate data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0 Clock input of counter 0.
OUT 0	10	O	OUTPUT 0 Output of counter 0.
GATE 0	11	I	GATE 0 Gate input of counter 0.
OUT 1	13	O	OUTPUT 1 Output of counter 1.
GATE 1	14	I	GATE 1 Gate input of counter 1.
CLK 1	15	I	CLOCK 1 Clock input of counter 1.
GATE 2	16	I	GATE 2 Gate input of counter 2.
OUT 2	17	O	OUTPUT 2 Output of counter 2.
CLK 2	18	I	CLOCK 2 Clock input of counter 2.
A1, A0	20-19	I	ADDRESS 1, 0 Used to select one of the three counters or the control word register for read or write operations. Normally connected to the system address bus.
$\overline{CS}$	21	I	$\overline{CHIP\ SELECT}$ A low on this input enables the SAB 82C53 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	$\overline{READ\ CONTROL}$ This input is low during CPU read operations.
$\overline{WR}$	23	I	$\overline{WRITE\ CONTROL}$ This input is low during CPU write operations.
V_{CC}	24	–	POWER SUPPLY (+5V)
GND	12	–	GROUND (0 V)

A1	A0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

Block Diagram



Functional Description

General

The SAB 82C53 is a programmable interval timer/counter designed for use with Siemens and other microcomputer systems. It is a general-purpose, multitiming element that can be treated as an array of I/O ports in the system software.

The SAB 82C53 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the SAB 82C53 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the SAB 82C53 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other timer/counter functions common to microcomputers which can be implemented with the SAB 82C53 are:

- Real time clock
- Event counter
- Digital monoflop
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Slave Interface

The bidirectional tristate data bus buffer is used to interface the SAB 82C53 to the system bus.

The read/write logic accepts inputs from the system bus and generates control signals for the other functional blocks of the SAB 82C53. A1 and A0 select one of the three counters or the control word register for read or write accesses. An active (low) $\overline{RD}$ input allows the CPU to read one of the counters. An active (low) $\overline{WR}$ input allows the CPU to write into one of the control word registers. $\overline{RD}$ and $\overline{WR}$ are ignored unless the SAB 82C53 is selected by an active (low) $\overline{CS}$ input.

Control Word Register

The control word register is selected by the read/write logic with A1, A0 = 11. A CPU write operation stores a control word into the control word register. These control words specify the operating mode of the counters.

The control word register can only be written to; no read operation of its contents is available.

Counters

These three functional blocks are identical in operation, so only a single counter will be described.

The counters are fully independent. Each counter may operate in a different mode. The internal block diagram of a single counter is shown in the following figure. The control word register shown in the figure is not part of the counter itself, but determines the operating mode of the counter.

The actual counter is labelled CE (for "counting element"). It is a 16-bit presettable synchronous down counter.

Output latch M and output latch L are two 8-bit latches. The designations M and L stand for "most significant byte" and "least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable counter latch command is sent to the SAB 82C53, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's control logic to drive the internal bus. This is how the 16-bit counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called count register M and count register L. Both are normally referred to as one unit and called just CR. When a new count is written to the counter, the count is stored in the CR and later transferred to the CE. The control logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR M and CR L are cleared when the counter is programmed. In this way, if the counter has been programmed for one byte counts (either most significant byte only or least significant byte only), the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

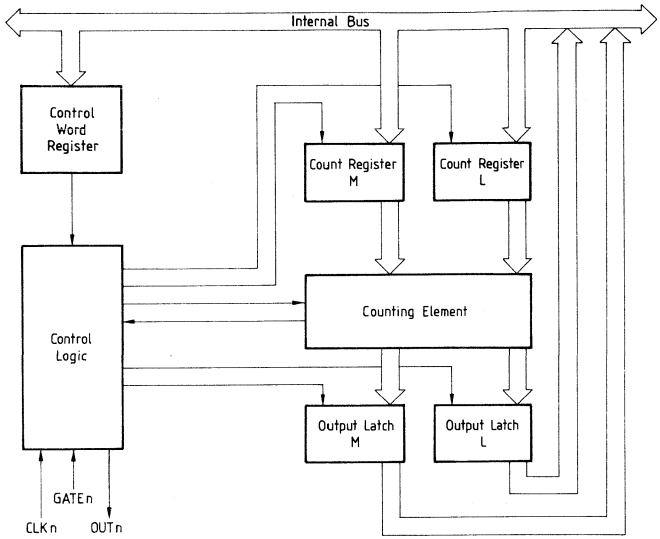
The control logic is also shown in the diagram. CLKn, GATEn, and OUTn are all connected to the outside world through the control logic.

System Interface

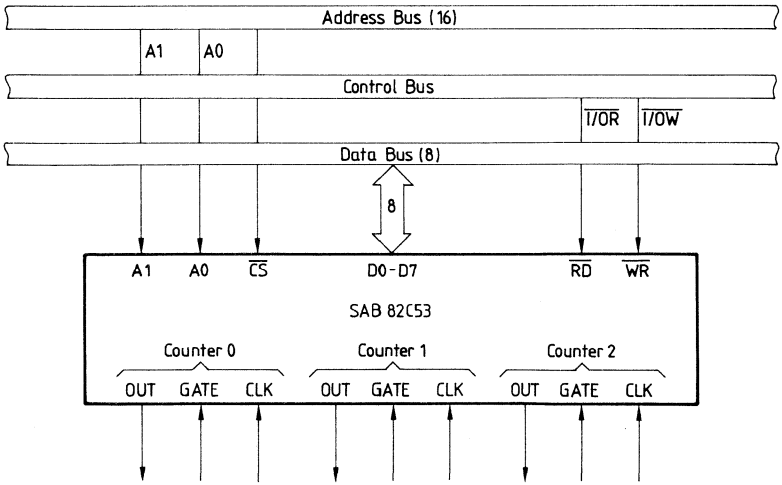
The SAB 82C53 is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for mode programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder for larger systems.

Internal Block Diagram of a Counter



SAB 82C53 System Interface



Operational Description

General

After power-up, the state of the SAB 82C53 is undefined. The mode, count value, and output of all counters are undefined.

The operating mode of each counter is determined when it is programmed. Each counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the SAB 82C53

Counters are programmed by writing a control word and then an initial count. The control word format is shown in the following figure.

All control words are written into the control word register, which is selected with A1, A0 = 11. The control word itself specifies which counter is being programmed.

By contrast, initial counts are written into the counters, not the control word register. The A1, A0 inputs are used to select the counter to be written into. The format of the initial count is determined by the control word used.

Control Word Format

A1, A0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC – Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RW – Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see read operations)
0	1	Read/Write Least Significant Byte Only.
1	0	Read/Write Most Significant Byte Only.
1	1	Read/Write Least Significant Byte First, Then Most Significant Byte.

M – Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter, 16-Bit
1	Binary-Coded Decimal (BCD) Counter (4 decades)

NOTE: Don't care bits (X) should be 0 to insure compatibility with future products.

Write Operations

The programming procedure for the SAB 82C53 is very flexible. Only two conventions need to be remembered:

1) For each counter the control word must be written before the initial count is written.
2) The initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the control word register and the three counters have separate addresses (selected by the A1, A0 inputs), and each control word specifies the counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a counter at any time without affecting the counter's programmed mode in any way. Counting will be affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

A Few Possible Programming Sequences

	A1	A0
Control Word – Counter 0	1	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0
Control Word – Counter 1	1	1
LSB of Count – Counter 1	0	1
MSB of Count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 2	1	0

	A1	A0
Control Word – Counter 2	1	1
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 2	1	0
LSB of Count – Counter 1	0	1
MSB of Count – Counter 1	0	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0

	A1	A0
Control Word – Counter 0	1	1
Counter Word – Counter 1	1	1
Control Word – Counter 2	1	1
LSB of Count – Counter 2	1	0
LSB of Count – Counter 1	0	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0
MSB of Count – Counter 1	0	1
MSB of Count – Counter 2	1	0

	A1	A0
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of Count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 1	0	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 0	0	0
MSB of Count – Counter 2	1	0

Note:
In all four examples, all counters are programmed to read/write two-byte counts.
These are only four of many possible programming sequences.

Read Operations

It is often desirable to read the value of a counter without disturbing the count in progress. This is easily done in the SAB 82C53.

There are two possible methods for reading the counters: a simple read operation and the counter latch command.

Each is explained below. The first method is to perform a simple read operation. To read the counter which is selected with the A1, A0 inputs, the CLK input of the selected counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.
Note that reading the control word register is illegal and will return unreliable data.

Counter Latch Command

The second method uses the "counter latch command". Like a control word, this command is written to the control word register, which is selected with A1, A0 = 11. Also like a control word, the SC0, SC1 bits select one of the three counters, but two other bits, D5 and D4, distinguish this command from a control word.

The selected counter's output latch (OL) latches the count at the time the counter latch command is received. This count is held in the latch until it is read by the CPU (or until the counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the counters "on the fly" without affecting counting in progress. Multiple counter latch commands may be used to latch more than one counter. Each latched counter's OL holds its count until it is read. Counter latch commands do not affect the programmed mode of the counter in any way.

If a counter is latched and then, some time later, latched again before the count is read, the second counter latch command is ignored. The count read will be the count at the time the first counter latch command was issued.

With either method, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other counters may be inserted between them.

Another feature of the SAB 82C53 is that reads and writes of the same counter may be interleaved; for example, if the counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte
2. Write new least significant byte
3. Read most significant byte
4. Write new most significant byte

If a counter is programmed to read/write two-byte counts, the following precaution applies; a program must not transfer control between reading the first and second byte to another routine which also reads from that same counter. Otherwise, an incorrect count will be read.

Counter Latch Command Format

A1, A0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 = specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Illegal

D5, D4 = 00 designates counter latch command

X = don't care

Note:
Don't care bits (X) should be 0 to insure compatibility with future products.

Read/Write Operations Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Description
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No Operation (tristate)
1	X	X	X	X	No Operation (tristate)
0	1	1	X	X	No Operation (tristate)

Mode Definitions

The following are defined for use in describing the operation of the SAB 82C53.

CLK pulse: a rising edge, then a falling edge, in that order, of a counter's CLK input.

Trigger: a rising edge of a counter's GATE input.

Counter loading: the transfer of a count from the CR to the CE (refer to the "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the control word is written, OUT is initially low, and will remain low until the counter reaches zero. OUT then goes high and remains high until a new count or a new mode 0 control word is written into the counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the control word and initial count are written to a counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

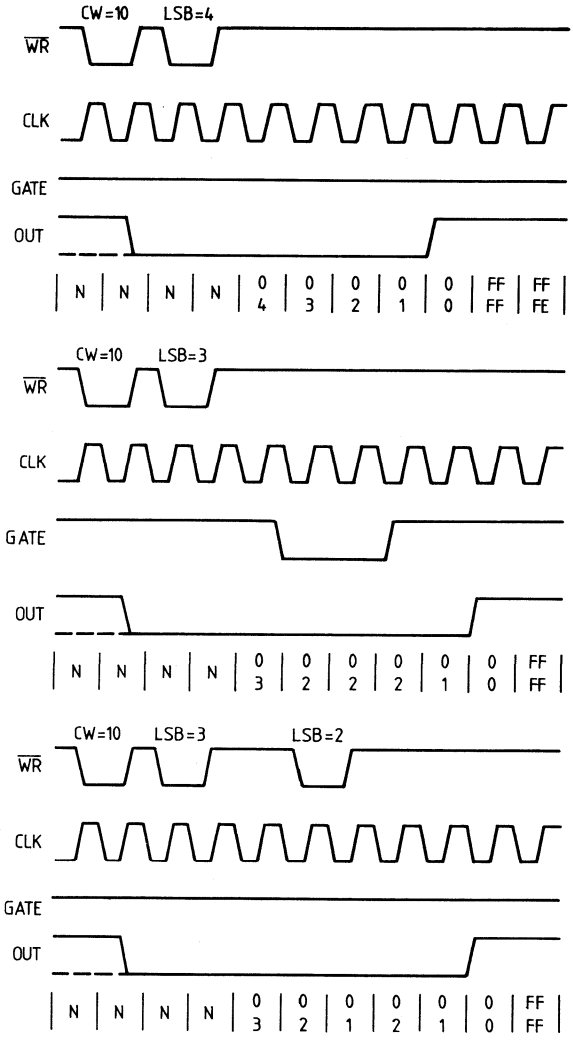
1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

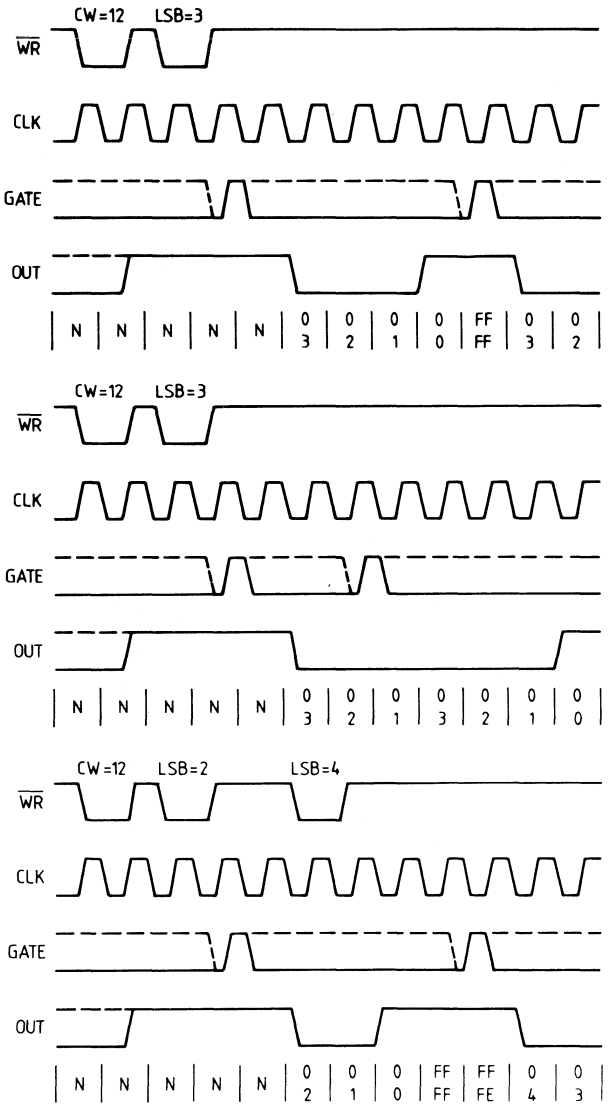
If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter as this has already been done.

Note:
The following conventions apply to all mode timing diagrams:
1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant bytes (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "control word"; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB stands for "Least Significant Byte" of count.
5. Numbers below diagrams are count values.
The lower number is the least significant byte.
The upper number is the most significant byte.
Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
N stands for an undefined count.
Vertical lines show transitions between count values.

Mode 0 Timing Diagram



Mode 1 Timing Diagram



Mode 1: Hardware-Retriggerable Single-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the single-shot pulse, and will remain low until the counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the control word and initial count, the counter is armed. A trigger results in loading the counter and setting OUT low on the next CLK pulse, thus starting the single-shot pulse. An initial count of N will result in a single-shot pulse N CLK cycles in duration. The single-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The single-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the counter during a single-shot pulse, the current single-shot is not affected unless the counter is retriggered. In that case, the counter is loaded with the new count and the pulse continues until the new count expires.

Mode 2: Rate Generator

This mode functions like a divide-by-N counter. It is typically used to generate a real-time clock interrupt. OUT will initially be high. When the initial count has decrement to 1, OUT goes low for one CLK pulse. OUT then goes high again, the counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated infinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the counter.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

Mode 3: Square Wave Mode

Mode 3 is typically used for baud rate generation. Mode 3 is similar to mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated infinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the counter.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. This allows the counter to be synchronized by software also.

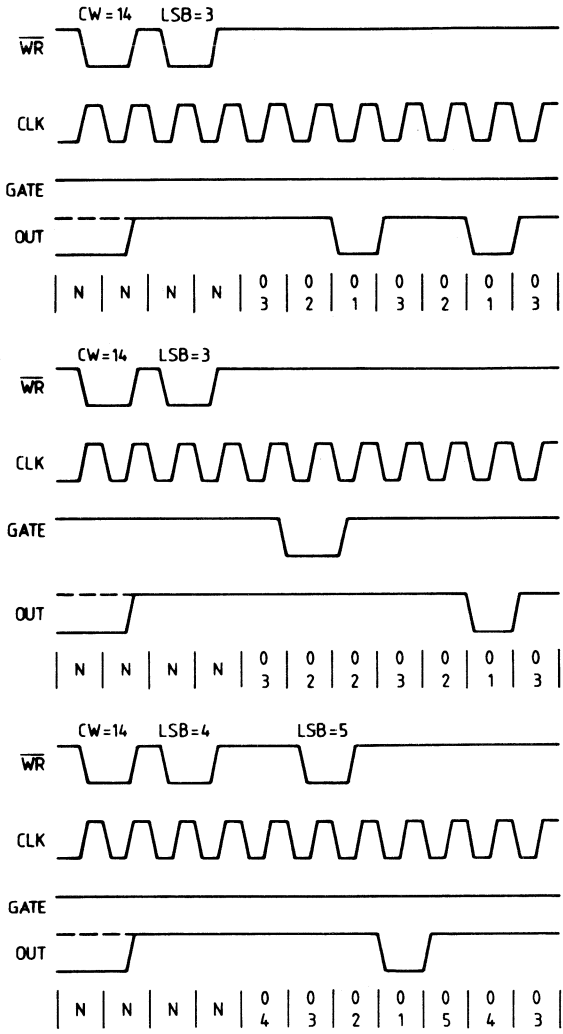
Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the counter is reloaded with the initial count. The above process is repeated infinitely.

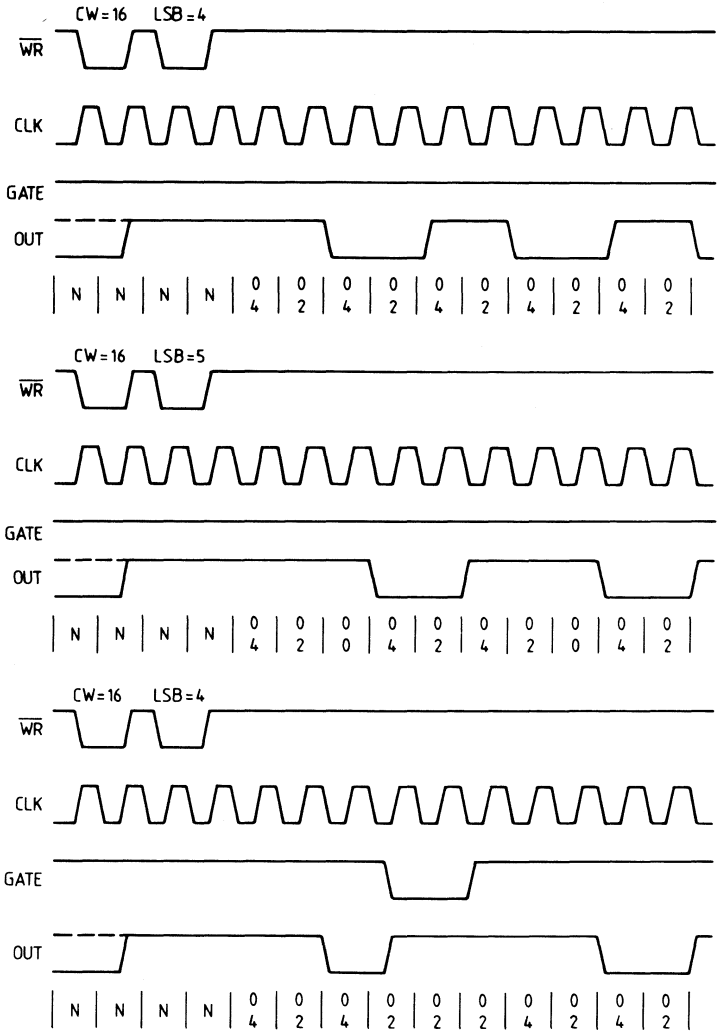
Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the counter is reloaded with the initial count minus one. The above process is repeated infinitely. So for odd counts, OUT will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.

Mode 2 Timing Diagram



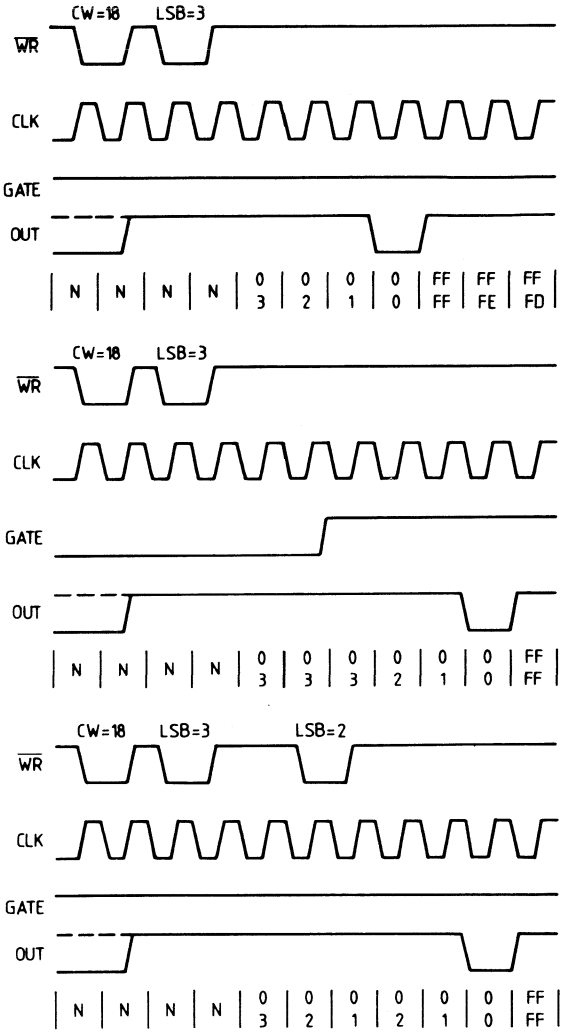
Note:
A GATE transition should not occur one clock prior to terminal count.

Mode 3 Timing Diagram



Note:
A GATE transition should not occur one clock prior to terminal count.

Mode 4 Timing Diagram



Mode 4: Software-Triggered Strobe

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5: Hardware-Triggered Strobe (retriggerable)

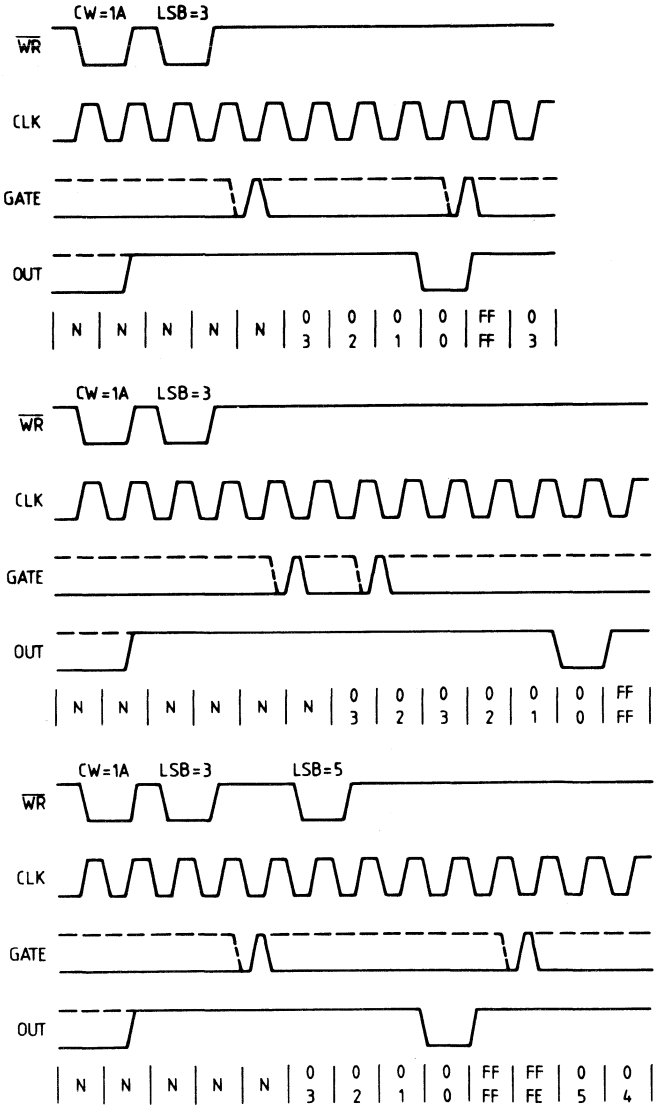
OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the control word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger results in the counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Mode 5 Timing Diagram



Operation Common to All Modes

Programming

When a control word is written to a counter, all control logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

GATE

The GATE input is always sampled on the rising edge of CLK. In modes 0, 2, 3, and 4 the GATE input is level-sensitive, and the logic level is sampled on the rising edge of CLK. In modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these modes a rising edge of GATE (trigger) sets an edge-sensitive flipflop in the counter. This flipflop is then sampled on the next rising edge of CLK; the flipflop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs – a high logic level does not have to be maintained until the next rising edge of CLK. Note that in modes 2 and 3, the GATE input is both edge- and level-sensitive. In modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following $\overline{WR}$ of a new count value.

GATE Pin Operations Summary

Signal Status Modes	Low or Going Low	Rising	High
0	Disables Counting	–	Enables Counting
1	–	1) Initiates Counting 2) Resets Output after Next Clock	–
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	–	Enables Counting
5	–	Initiates Counting	–

Counter

New counts are loaded and counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop when it reaches zero. In modes 0, 1, 4, and 5 the counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the counter reloads itself with the initial count and continues counting from there.

Minimum and Maximum Initial Counts

Mode	Min. Count	Max. Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0

Note:
0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to + 150°C
Supply voltage	−0.5 to + 8.0V
Voltage on any input	−2.0V to V_{CC} + 0.5V
Voltage on any output	−0.5V to V_{CC} + 0.5V
Power dissipation	1W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5V ±10%

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage	V_{IL}	−0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC} + 0.5	V	–
Output low voltage	V_{OL}	–	0.4	V	I_{OL} = 2.5 mA
Output high voltage	V_{OH}	3.0 V_{CC} − 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
Input load current	I_{IL}	–	±1	µA	$0 \leq V_{IN} \leq V_{CC}$
Output float leakage current	I_{OFL}	–	±10	µA	$0.45V \leq V_{OUT} \leq V_{CC}$
V_{CC} supply current	I_{CC}	–	10	mA	f = max. CLK frequency $V_{IN} = V_{CC}$ or GND All outputs open
V_{CC} supply current-standby	I_{CCSB}	–	10	µA	f_C = 0 (DC) $\overline{CS}$ = 1 All inputs/data bus high All outputs floating

Capacitance[1)]

T_A = 25°C, V_{CC} = GND = 0 V, f_C = 1 MHz

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input capacitance	C_{IN}	–	5	pF	Unmeasured pins returned to GND
I/O capacitance	C_{IO}	–	20	pF	
Output capacitance	C_{OUT}	–	15	pF	

[1)] These parameters are periodically sampled, not 100% tested.

AC Characteristics SAB 82C53

T_A = 0 to 70°C, V_{CC} = 5 V ±10%
AC timings are referred to 0.8 and 2.0 V points of signals unless otherwise noted.

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Address stable before $\overline{RD}$ ↓	t_{AR}	50	–	ns	–
Address hold time after $\overline{RD}$ ↓	t_{RA}	5	–	ns	–
$\overline{RD}$ pulse width	t_{RR}	400	–	ns	–
Data delay from $\overline{RD}$ ↓	t_{RD}	–	300	ns	–
$\overline{RD}$ ↑ to data floating	t_{DF}	25	125	ns	–
Command recovery time	t_{RV}	1	–	µs	–
Address stable before $\overline{WR}$ ↓	t_{AW}	50	–	ns	–
Address hold time after $\overline{WR}$ ↑	t_{WA}	30	–	ns	–
$\overline{WR}$ pulse width	t_{WW}	400	–	ns	–
Data setup time before $\overline{WR}$ ↑	t_{DW}	300	–	ns	–
Data hold time after $\overline{WR}$ ↑	t_{WD}	40	–	ns	–
Command recovery time	t_{RV}	1	–	µs	–
Clock period	t_{CLK}	380	DC	ns	–
High pulse width	t_{PWH}	230	–	ns	[1]
Low pulse width	t_{PWL}	150	–	ns	[1]
Gate width high	t_{GW}	150	–	ns	–
Gate width low	t_{GL}	100	–	ns	–
Gate setup time to CLK ↑	t_{GS}	100	–	ns	–
Gate hold time after CLK ↑	t_{GH}	50	–	ns	[2]
Output delay from CLK ↓	t_{OD}	–	400	ns	–
Output delay from GATE ↓	t_{ODG}	–	300	ns	–

[1] Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
[2] In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns of the rising clock edge may not be detected.

AC Characteristics SAB 82C53-5

T_A = 0 to 70°C, V_{CC} = 5 V ±10%
AC timings are referred to 0.8 and 2.0 V points of signals unless otherwise noted.

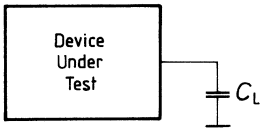
Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Address stable before $\overline{RD}\downarrow$	t_{AR}	30	–	ns	–
Address hold time after $\overline{RD}\downarrow$	t_{RA}	5	–	ns	–
$\overline{RD}$ pulse width	t_{RR}	300	–	ns	–
Data delay from $\overline{RD}\downarrow$	t_{RD}	–	200	ns	–
$\overline{RD}\uparrow$ to data floating	t_{DF}	25	100	ns	–
Command recovery time	t_{RV}	1	–	µs	–
Address stable before $\overline{WR}\downarrow$	t_{AW}	30	–	ns	–
Address hold time after $\overline{WR}\uparrow$	t_{WA}	30	–	ns	–
$\overline{WR}$ pulse width	t_{WW}	300	–	ns	–
Data setup time before $\overline{WR}\uparrow$	t_{DW}	250	–	ns	–
Data hold time after $\overline{WR}\uparrow$	t_{WD}	30	–	ns	–
Command recovery time	t_{RV}	1	–	µs	–
Clock period	t_{CLK}	380	DC	ns	–
High pulse width	t_{PWH}	230	–	ns	[1]
Low pulse width	t_{PWL}	150	–	ns	[1]
Gate width high	t_{GW}	150	–	ns	–
Gate width low	t_{GL}	100	–	ns	–
Gate setup time to CLK ↑	t_{GS}	100	–	ns	–
Gate hold time after CLK ↑	t_{GH}	50	–	ns	[2]
Output delay from CLK ↓	t_{OD}	–	400	ns	–
Output delay from GATE ↓	t_{ODG}	–	300	ns	–

[1] Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.

[2] In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 70 ns of the rising clock edge may not be detected.

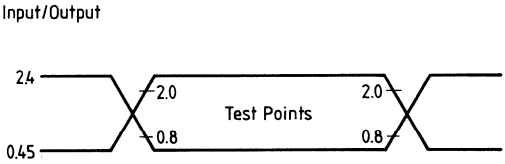
AC Testing Waveforms

Test Loadings



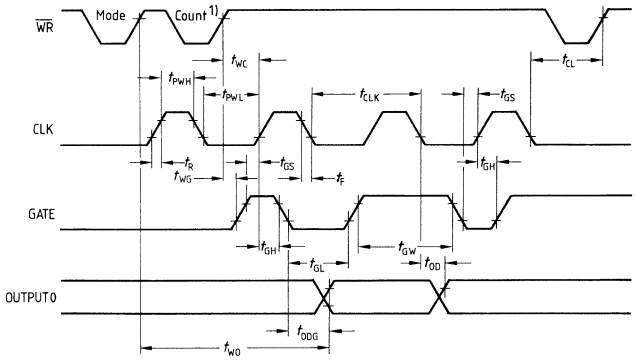
C_L = 150 pF
C_L Includes Jig Capacitance

Measurement Reference Levels



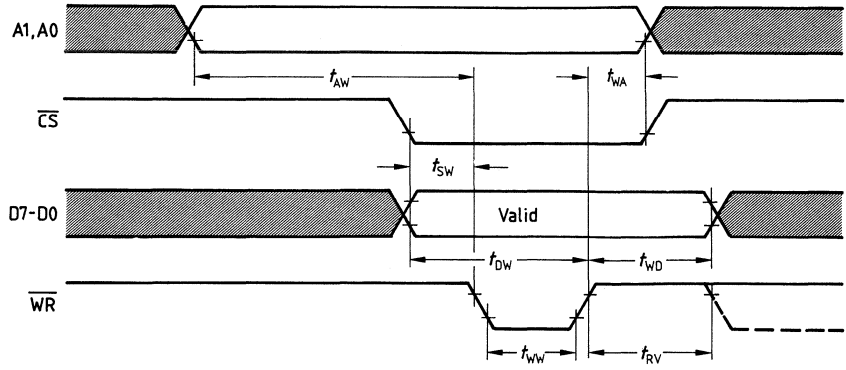
AC Testing: Inputs are driven at 2.4V for a logic "1" and at 0.45V for a logic "0".

Counter Control Timing

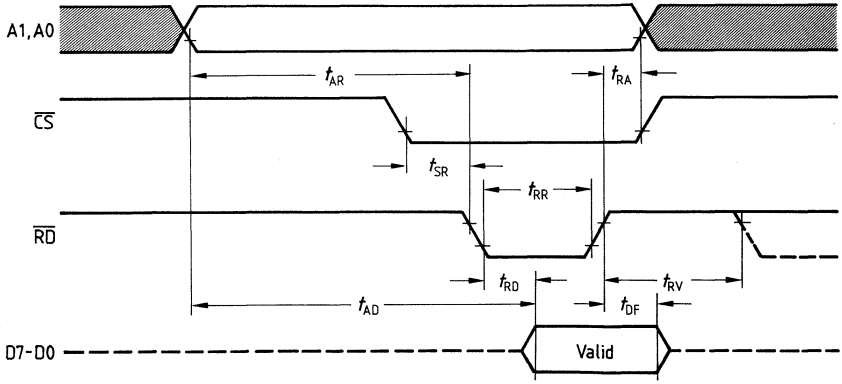


1) Last byte of count being written

Write Cycle Timing



Read Cycle Timing



Ordering Information

Type	Ordering code	Description
SAB 82C53-P	Q67120-P217	Programmable CMOS interval timer
SAB 82C53-5-P	Q67120-P264	Programmable CMOS interval timer

Preliminary

SAB 82C54 Programmable CMOS Interval Timer

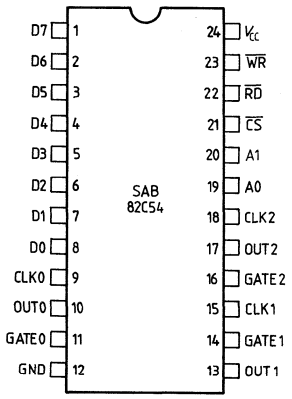
SAB 82C54 up to 8 MHz

- Compatible with all Siemens and most other microprocessors
- Three independent 16-bit counters
- Handles inputs from DC to 8 MHz (10 MHz for SAB 82C54-2)
- Low power CMOS (I_{CC} = 10 mA at max. count frequency)
- Completely TTL compatible

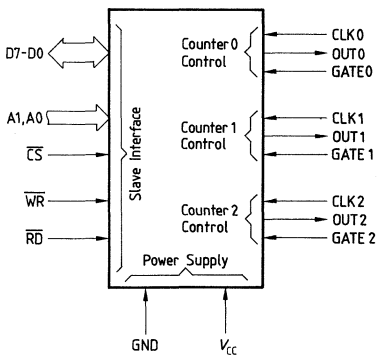
SAB 82C54-2 up to 10 MHz

- Six programmable counter modes
- Binary or BCD counting
- Status read back command
- Available in 24-pin dual-in-line package (P-DIP-24)

Pin Configuration



Logic Symbol



The SAB 82C54 is a high-performance, CMOS version of the industry standard 8254 timer/counter which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software-programmable. The SAB 82C54 is pin-compatible with the NMOS 8254, and is a superset of the SAB 82C53.

Six programmable timer modes allow the SAB 82C54 to be used as an event counter, elapsed time indicator, programmable monoflop, and in many other applications.

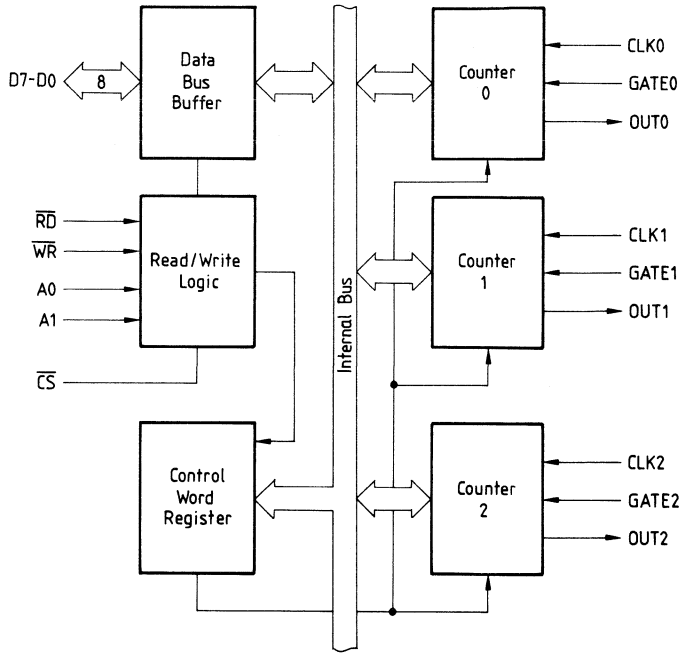
The SAB 82C54 is fabricated in Siemens advanced CMOS technology which provides low power consumption and is packaged in a 24-pin dual-in-line plastic package (P-DIP-24).

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
D7-D0	1-8	I/O	**DATA 7-0** Bidirectional tristate data bus lines, connected to system data bus.
CLK 0	9	I	**CLOCK 0** Clock input of counter 0.
OUT 0	10	O	**OUTPUT 0** Output of counter 0.
GATE 0	11	I	**GATE 0** Gate input of counter 0.
OUT 1	13	O	**OUTPUT 1** Output of counter 1.
GATE 1	14	I	**GATE 1** Gate input of counter 1.
CLK 1	15	I	**CLOCK 1** Clock input of counter 1.
GATE 2	16	I	**GATE 2** Gate input of counter 2.
OUT 2	17	O	**OUTPUT 2** Output of counter 2.
CLK 2	18	I	**CLOCK 2** Clock input of counter 2.
A1, A0	20-19	I	**ADDRESS 1, 0** Used to select one of the three counters or the control word register for read or write operations. Normally connected to the system address bus.
$\overline{CS}$	21	I	**$\overline{CHIP\ SELECT}$** A low on this input enables the SAB 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	**$\overline{READ\ CONTROL}$** This input is low during CPU read operations.
$\overline{WR}$	23	I	**$\overline{WRITE\ CONTROL}$** This input is low during CPU write operations.
V_{CC}	24	–	**POWER SUPPLY** (+5 V)
GND	12	–	**GROUND** (0 V)

A1	A0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

Block Diagram



Functional Description

General

The SAB 82C54 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general-purpose, multitiming element that can be treated as an array of I/O ports in the system software.

The SAB 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the SAB 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the SAB 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other timer/counter functions common to microcomputers which can be implemented with the SAB 82C54 are:

- Real time clock
- Event counter
- Digital monoflop
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Slave Interface

The bidirectional tristate data bus buffer is used to interface the SAB 82C54 to the system bus.

The read/write logic accepts inputs from the system bus and generates control signals for the other functional blocks of the SAB 82C54. A1 and A0 select one of the three counters or the control word register for read or write accesses. An active (low) $\overline{RD}$ input allows the CPU to read one of the counters. An active (low) $\overline{WR}$ input allows the CPU to write into one of the control word registers. $\overline{RD}$ and $\overline{WR}$ are ignored unless the SAB 82C54 is selected by an active (low) $\overline{CS}$ input.

Control Word Register

The control word register is selected by the read/write logic with A1, A0 = 11. A CPU write operation stores a control word into the control word register. These control words specify the operating mode of the counters.

The control word register can only be written to; status information is available with the read-back command.

Counters

These three functional blocks are identical in operation, so only a single counter will be described.

The counters are fully independent. Each counter may operate in a different mode. The internal block diagram of a single counter is shown in the following figure. The control word register shown in the figure is not part of the counter itself, but determines the operating mode of the counter.

The status register, shown in the figure, when latched, contains the current contents of the control word register and status of the output and null count flag. (See detailed explanation of the read-back command.)

The actual counter is labelled CE (for "counting element"). It is a 16-bit presettable synchronous down counter.

Output latch M and output latch L are two 8-bit latches. The designations M and L stand for "most significant byte" and "least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable counter latch command is sent to the SAB 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's control logic to drive the internal bus. This is how the 16-bit counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called count register M and count register L. Both are normally referred to as one unit and called just CR. When a new count is written to the counter, the count is stored in the CR and later transferred to the CE. The control logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR M and CR I are cleared when the counter is programmed. In this way, if the counter has been programmed for one byte counts (either most significant byte only or least significant byte only), the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

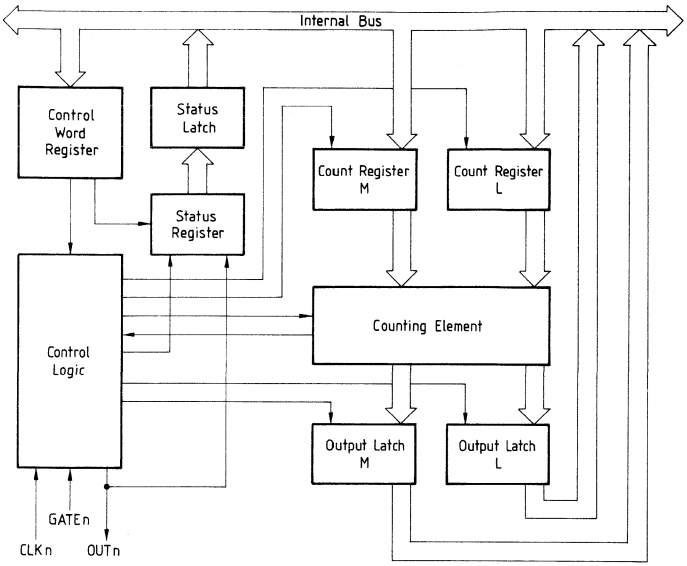
The control logic is also shown in the diagram. CLKn, GATEn, and OUTn are all connected to the outside world through the control logic.

System Interface

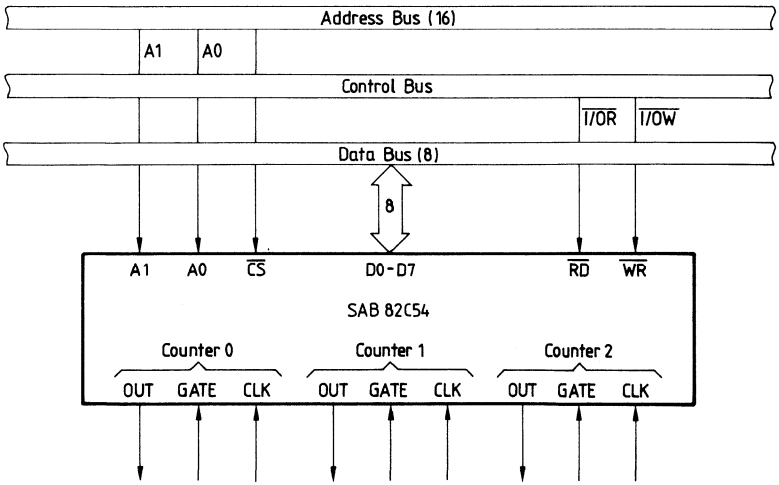
The SAB 82C54 is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for mode programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder for larger systems.

Internal Block Diagram of a Counter



SAB 82C54 System Interface



Operational Description

General

After power-up, the state of the SAB 82C54 is undefined. The mode, count value, and output of all counters are undefined.

The operating mode of each counter is determined when it is programmed. Each counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the SAB 82C54

Counters are programmed by writing a control word and then an initial count. The control word format is shown in the following figure.

All control words are written into the control word register, which is selected with A1, A0 = 11. The control word itself specifies which counter is being programmed.

By contrast, initial counts are written into the counters, not the control word register. The A1, A0 inputs are used to select the counter to be written into. The format of the initial count is determined by the control word used.

Control Word Format

A1, A0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC – Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see read operations)

RW – Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see read operations)
0	1	Read/Write Least Significant Byte Only.
1	0	Read/Write Most Significant Byte Only.
1	1	Read/Write Least Significant Byte First, Then Most Significant Byte.

M – Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter, 16-Bit
1	Binary-Coded Decimal (BCD) Counter (4 decades)

NOTE: Don't care bits (X) should be 0 to insure compatibility with future products.

Write Operations

The programming procedure for the SAB 82C54 is very flexible. Only two conventions need to be remembered:

1) For each counter the control word must be written before the initial count is written.
2) The initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the control word register and the three counters have separate addresses (selected by the A1, A0 inputs), and each control word specifies the counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a counter at any time without affecting the counter's programmed mode in any way. Counting will be affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

A Few Possible Programming Sequences

	A1	A0
Control Word – Counter 0	1	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0
Control Word – Counter 1	1	1
LSB of Count – Counter 1	0	1
MSB of Count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 2	1	0

	A1	A0
Control Word – Counter 2	1	1
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 2	1	0
LSB of Count – Counter 1	0	1
MSB of Count – Counter 1	0	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0

	A1	A0
Control Word – Counter 0	1	1
Counter Word – Counter 1	1	1
Control Word – Counter 2	1	1
LSB of Count – Counter 2	1	0
LSB of Count – Counter 1	0	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 0	0	0
MSB of Count – Counter 1	0	1
MSB of Count – Counter 2	1	0

	A1	A0
Control Word – Counter 1	1	1
Control Word – Counter 0	1	1
LSB of Count – Counter 1	0	1
Control Word – Counter 2	1	1
LSB of Count – Counter 0	0	0
MSB of Count – Counter 1	0	1
LSB of Count – Counter 2	1	0
MSB of Count – Counter 0	0	0
MSB of Count – Counter 2	1	0

Note:
In all four examples, all counters are programmed to read/write two-byte counts.
These are only four of many possible programming sequences.

Read Operations

It is often desirable to read the value of a counter without disturbing the count in progress. This is easily done in the SAB 82C54.

There are three possible methods for reading the counters: a simple read operation, the counter latch command, and the read-back command. Each is explained below. The first method is to perform a simple read operation. To read the counter which is selected with the A1, A0 inputs, the CLK input of the selected counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

Counter Latch Command

The second method uses the "counter latch command". Like a control word, this command is written to the control word register, which is selected with A1, A0 = 11. Also like a control word, the SC0, SC1 bits select one of the three counters, but two other bits, D5 and D4, distinguish this command from a control word.

The selected counter's output latch (OL) latches the count at the time the counter latch command is received. This count is held in the latch until it is read by the CPU (or until the counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the counters "on the fly" without affecting counting in progress. Multiple counter latch commands may be used to latch more than one counter. Each latched counter's OL holds its count until it is read. Counter latch commands do not affect the programmed mode of the counter in any way.

If a counter is latched and then, some time later, latched again before the count is read, the second counter latch command is ignored. The count read will be the count at the time the first counter latch command was issued.

With either method, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other counters may be inserted between them.

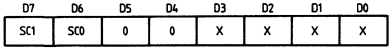
Another feature of the SAB 82C54 is that reads and writes of the same counter may be interleaved; for example, if the counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte
2. Write new least significant byte
3. Read most significant byte
4. Write new most significant byte

If a counter is programmed to read/write two-byte counts, the following precaution applies; a program must not transfer control between reading the first and second byte to another routine which also reads from that same counter. Otherwise, an incorrect count will be read.

Counter Latch Command Format

A1, A0 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0



SC1, SC0 = specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-back command

D5, D4 = 00 designates counter latch command

X = don't care

Note:
Don't care bits (X) should be 0 to insure compatibility with future products.

Read-Back Command

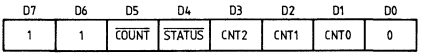
The third method uses the read-back command. This command allows the user to check the count value, programmed mode, current state of the OUT pin, and "null count" flag of the selected counter(s).

The command is written into the control word register and has the format shown in the figure below. The command applies to the counters selected by setting their corresponding bits D3, D2, D1 to 1.

The read-back command may be used to latch multiple counter output latches (OL) by setting the $\overline{COUNT}$ bit D5 to 0 and selecting the desired counter(s). The single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the

Read-Back Command Format

A0, A1 = 11, $\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0



D5: 0 = Latch Count of Selected Counter(s)
D4: 0 = Latch Status of Selected Counter(s)
D3: 1 = Select Counter 2
D2: 1 = Select Counter 1
D1: 1 = Select Counter 0
D0: Reserved for Future Expansion; Must Be 0

Status Byte

D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7: 1 = OUT Pin is 1
0 = OUT Pin is 0
D6: 1 = Null count
0 = Count available for reading
D5-D0: Counter programmed mode

count, all but the first are ignored, i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting $\overline{\text{STATUS}}$ bit D4 to 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in the next figure. Bits D5 through D0 contain the counter's programmed mode exactly as written in the last mode control word. Output bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

Null count bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time when this happens depends on the mode of the counter and is described in the mode definitions, but until the count is loaded into the counting element (CE), it cannot be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of null count is shown in the following figure.

Null Count Operation

THIS ACTION:	CAUSES:
A. Write to the control word register: [1]	Null count = 1
B. Write to the count register (CR); [2]	Null count = 1
C. New count is loaded into CE (CR → CE);	Null count = 0

[1] Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

[2] If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both $\overline{\text{COUNT}}$ and $\overline{\text{STATUS}}$ bits D5, D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in the figure below.

If both count and status of a counter are latched, the first read operation of that counter will return the latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two byte counts) return latched count. Subsequent reads return unlatched count.

Read-Back Command Example

Command								Description	Results
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read Back Count and Status of Counter 0	Count and Status Latched for Counter 0
1	1	1	0	0	1	0	0	Read Back Status of Counter 1	Status Latched for Counter 1
1	1	1	0	1	1	0	0	Read Back Status of Counter 2, 1	Status Latched for Counter 2, but Not Counter 1
1	1	0	1	1	0	0	0	Read Back Count of Counter 2	Count Latched for Counter 2
1	1	0	0	0	1	0	0	Read Back Count and Status of Counter 1	Count Latched for Counter 1, but Not Status
1	1	1	0	0	0	1	0	Read Back Status of Counter 1	Command Ignored, Status Already Latched for Counter 1

Read/Write Operations Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Description
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No Operation (tristate)
1	X	X	X	X	No Operation (tristate)
0	1	1	X	X	No Operation (tristate)

Mode Definitions

The following are defined for use in describing the operation of the SAB 82C54.

CLK pulse: a rising edge, then a falling edge, in that order, of a counter's CLK input.

Trigger: a rising edge of a counter's GATE input.

Counter loading: the transfer of a count from the CR to the CE (refer to the "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the control word is written, OUT is initially low, and will remain low until the counter reaches zero. OUT then goes high and remains high until a new count or a new mode 0 control word is written into the counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the control word and initial count are written to a counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

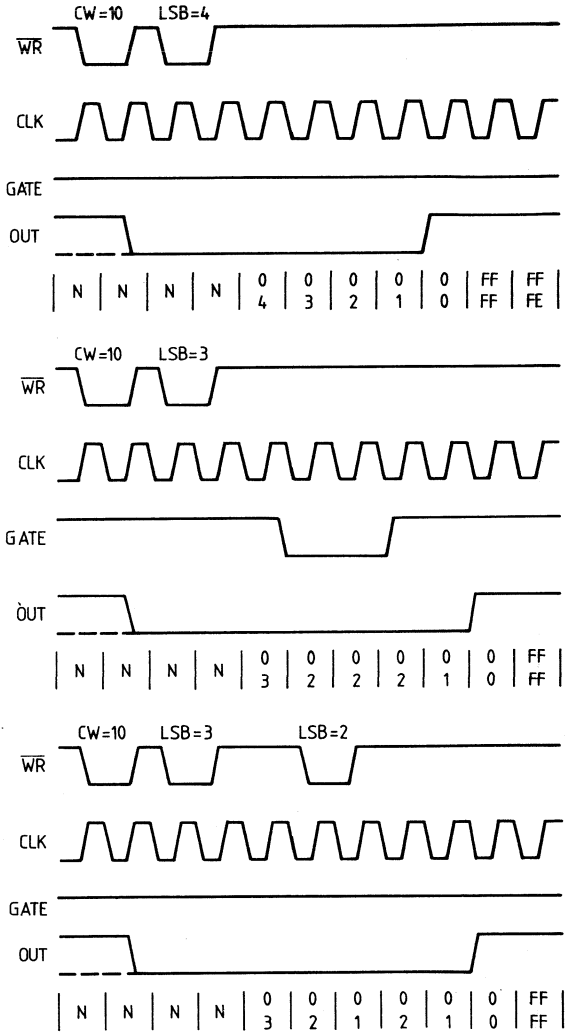
1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

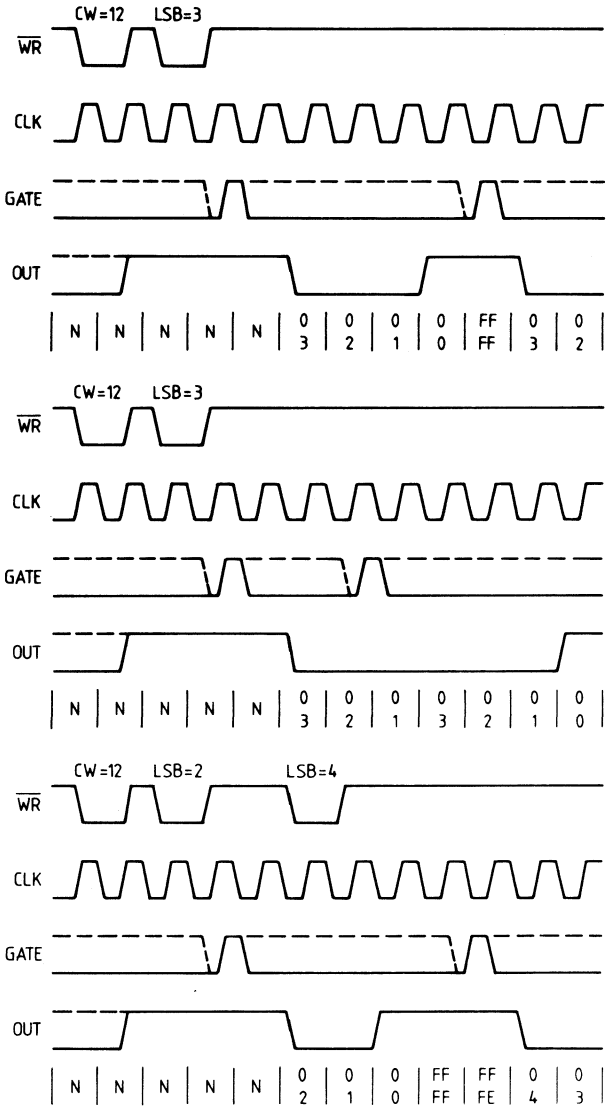
If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter as this has already been done.

Note:
The following conventions apply to all Mode Timing Diagrams:
1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant bytes (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "control word"; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB stands for "Least Significant Byte" of count.
5. Numbers below diagrams are count values.
The lower number is the least significant byte.
The upper number is the most significant byte.
Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
N stands for an undefined count.
Vertical lines show transitions between count values.

Mode 0 Timing Diagram



Mode 1 Timing Diagram



Mode 1: Hardware-Retriggerable Single-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the single-shot pulse, and will remain low until the counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the control word and initial count, the counter is armed. A trigger results in loading the counter and setting OUT low on the next CLK pulse, thus starting the single-shot pulse. An initial count of N will result in a single-shot pulse N CLK cycles in duration. The single-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The single-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the counter during a single-shot pulse, the current single-shot is not affected unless the counter is retriggered. In that case, the counter is loaded with the new count and the pulse continues until the new count expires.

Mode 2: Rate Generator

This mode functions like a divide-by-N counter. It is typically used to generate a real-time clock interrupt. OUT will initially be high. When the initial count has decrement to 1, OUT goes low for one CLK pulse. OUT then goes high again, the counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated infinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the counter.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

Mode 3: Square Wave Mode

Mode 3 is typically used for baud rate generation. Mode 3 is similar to mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated infinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the counter.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. This allows the counter to be synchronized by software also.

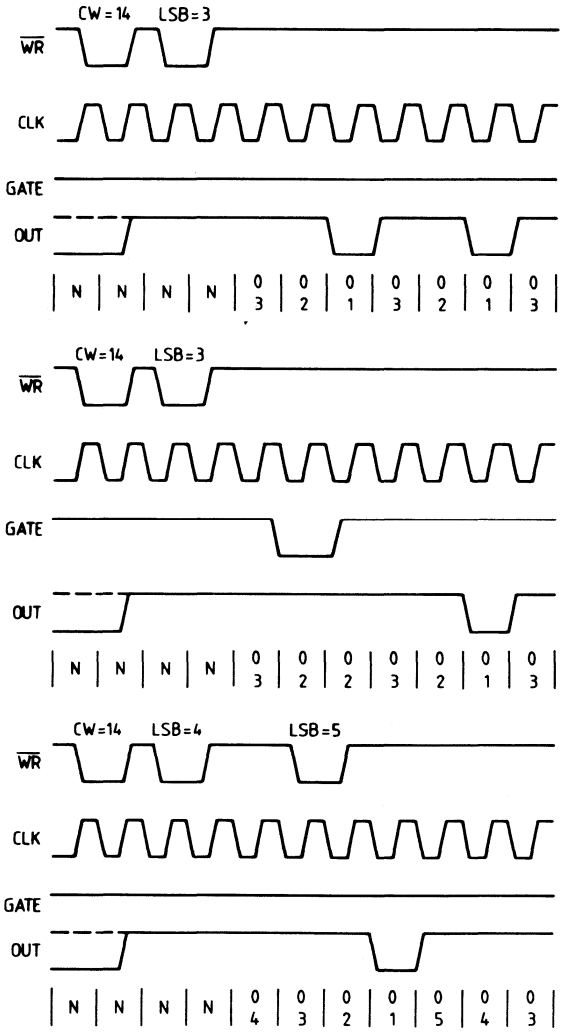
Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the counter is reloaded with the initial count. The above process is repeated infinitely.

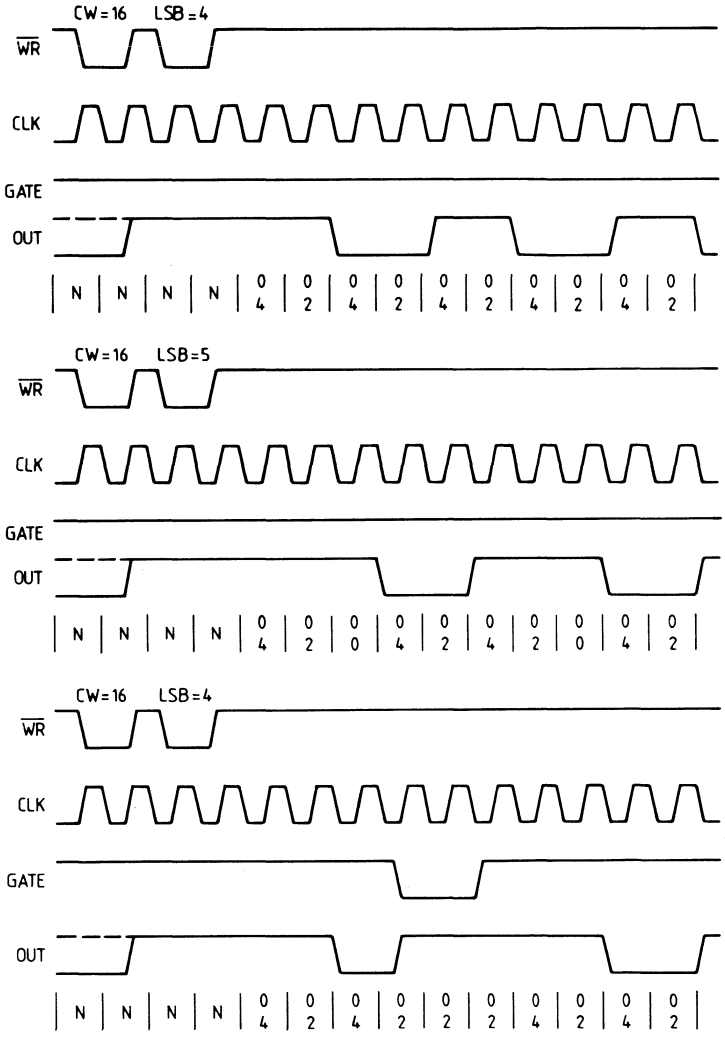
Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the counter is reloaded with the initial count minus one. The above process is repeated infinitely. So for odd counts, OUT will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.

Mode 2 Timing Diagram



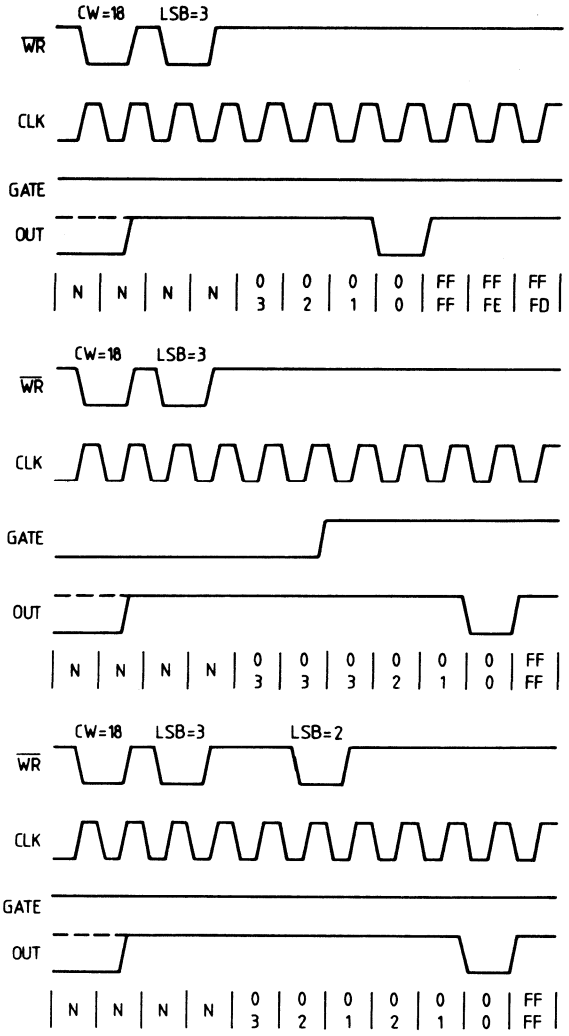
Note:
A GATE transition should not occur one clock prior to terminal count.

Mode 3 Timing Diagram



Note:
A GATE transition should not occur one clock prior to terminal count.

Mode 4 Timing Diagram



Mode 4: Software-Triggered Strobe

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5: Hardware-Triggered Strobe (retriggerable)

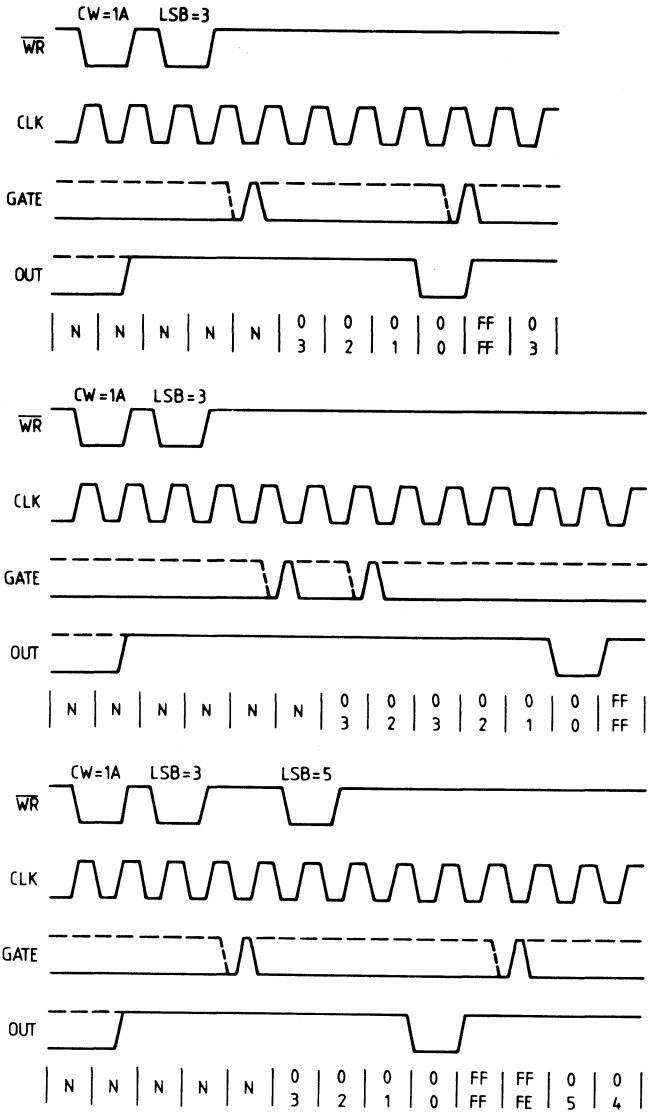
OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the control word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger results in the counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Mode 5 Timing Diagram



Operation Common to All Modes

Programming

When a control word is written to a counter, all control logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

GATE

The GATE input is always sampled on the rising edge of CLK. In modes 0, 2, 3, and 4 the GATE input is level-sensitive, and the logic level is sampled on the rising edge of CLK. In modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these modes a rising edge of GATE (trigger) sets an edge-sensitive flipflop in the counter. This flipflop is then sampled on the next rising edge of CLK; the flipflop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs – a high logic level does not have to be maintained until the next rising edge of CLK. Note that in modes 2 and 3, the GATE input is both edge- and level-sensitive. In modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following $\overline{WR}$ of a new count value.

GATE Pin Operations Summary

Signal Status Modes	Low or Going Low	Rising	High
0	Disables Counting	–	Enables Counting
1	–	1) Initiates Counting 2) Resets Output after Next Clock	–
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	–	Enables Counting
5	–	Initiates Counting	–

Counter

New counts are loaded and counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop when it reaches zero. In modes 0, 1, 4, and 5 the counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the counter reloads itself with the initial count and continues counting from there.

Minimum and Maximum Initial Counts

Mode	Min. Count	Max. Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0

Note:
0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to + 150°C
Supply voltage	−0.5 to + 8.0V
Voltage on any input	−2.0V to V_{CC} + 0.5V
Voltage on any output	−0.5V to V_{CC} + 0.5V
Power dissipation	1W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} − 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input load current	–	±1	µA	0 ≤ V_{IN} ≤ V_{CC}
I_{OFL}	Output float leakage current	–	±10	µA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} supply current	–	10	mA	f = max. CLK frequency V_{IN} = V_{CC} or GND All outputs open
I_{CCSB}	V_{CC} supply current-standby	–	10	µA	f_C = 0 (DC) $\overline{CS}$ = 1 All inputs/data bus high All outputs floating

Capacitance[1)]

T_A = 25°C, V_{CC} = GND = 0V, f_C = 1 MHz

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	Unmeasured pins returned to GND
C_{IO}	I/O capacitance	–	20	pF	
C_{OUT}	Output capacitance	–	15	pF	

[1)] These parameters are periodically sampled, not 100% tested.

AC Characteristics SAB 82C54

T_A = 0 to 70°C, V_{CC} = 5 V ±10%
AC timings are referred to 0.8 and 2.0 V points of signals unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
t_{AR}	Address stable before $\overline{RD}$ ↓	45	–	ns	–
t_{SR}	$\overline{CS}$ stable before $\overline{RD}$ ↓	0	–	ns	–
t_{RA}	Address hold time after $\overline{RD}$ ↓	0	–	ns	–
t_{RR}	$\overline{RD}$ pulse width	150	–	ns	–
t_{RD}	Data delay from $\overline{RD}$ ↓	–	120	ns	–
t_{AD}	Data delay from address	–	220	ns	–
t_{DF}	$\overline{RD}$ ↑ to data floating	5	90	ns	–
t_{RV}	Command recovery time	200	–	ns	–
t_{AW}	Address stable before $\overline{WR}$ ↓	0	–	ns	–
t_{SW}	$\overline{CS}$ stable before $\overline{WR}$ ↓	0	–	ns	–
t_{WA}	Address hold time after $\overline{WR}$ ↑	0	–	ns	–
t_{WW}	$\overline{WR}$ pulse width	150	–	ns	–
t_{DW}	Data setup time before $\overline{WR}$ ↑	100	–	ns	–
t_{WD}	Data hold time after $\overline{WR}$ ↑	0	–	ns	–
t_{RV}	Command recovery time	200	–	ns	–
t_{CLK}	Clock period	125	DC	ns	–
t_{PWH}	High pulse width	60	–	ns	[1]
t_{PWL}	Low pulse width	60	–	ns	[1]
t_R	Clock rise time	–	100	ns	–
t_F	Clock fall time	–	100	ns	–
t_{GW}	Gate width high	50	–	ns	–
t_{GL}	Gate width low	50	–	ns	–
t_{GS}	Gate setup time to CLK ↑	50	–	ns	–
t_{GH}	Gate hold time after CLK ↑	50	–	ns	[2]
t_{OD}	Output delay from CLK ↓	–	150	ns	–
t_{ODG}	Output delay from GATE ↓	–	120	ns	–
t_{WC}	CLK delay for loading	0	55	ns	–
t_{WG}	Gate delay for sampling	−5	50	ns	–
t_{WO}	OUT delay from mode write	–	260	ns	–
t_{CL}	CLK setup for count latch	−4	45	ns	–

[1] Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
[2] In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns of the rising clock edge may not be detected.

AC Characteristics SAB 82C54-2

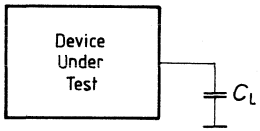
T_A = 0 to 70°C, V_{CC} = 5 V ±10%
AC timings are referred to 0.8 and 2.0 V points of signals unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
t_{AR}	Address stable before $\overline{RD}$ ↓	30	–	ns	–
t_{SR}	$\overline{CS}$ stable before $\overline{RD}$ ↓	0	–	ns	–
t_{RA}	Address hold time after $\overline{RD}$ ↓	0	–	ns	–
t_{RR}	$\overline{RD}$ pulse width	95	–	ns	–
t_{RD}	Data delay from $\overline{RD}$ ↓	–	85	ns	–
t_{AD}	Data delay from address	–	185	ns	–
t_{DF}	$\overline{RD}$ ↑ to data floating	5	65	ns	–
t_{RV}	Command recovery time	165	–	ns	–
t_{AW}	Address stable before $\overline{WR}$ ↓	0	–	ns	–
t_{SW}	$\overline{CS}$ stable before $\overline{WR}$ ↓	0	–	ns	–
t_{WA}	Address hold time after $\overline{WR}$ ↑	0	–	ns	–
t_{WW}	$\overline{WR}$ pulse width	95	–	ns	–
t_{DW}	Data setup time before $\overline{WR}$ ↑	85	–	ns	–
t_{WD}	Data hold time after $\overline{WR}$ ↑	0	–	ns	–
t_{RV}	Command recovery time	165	–	ns	–
t_{CLK}	Clock period	100	DC	ns	–
t_{PWH}	High pulse width	30	–	ns	[1]
t_{PWL}	Low pulse width	50	–	ns	[1]
t_R	Clock rise time	–	100	ns	–
t_F	Clock fall time	–	100	ns	–
t_{GW}	Gate width high	50	–	ns	–
t_{GL}	Gate width low	50	–	ns	–
t_{GS}	Gate setup time to CLK ↑	40	–	ns	–
t_{GH}	Gate hold time after CLK ↑	50	–	ns	[2]
t_{OD}	Output delay from CLK ↓	–	100	ns	–
t_{ODG}	Output delay from GATE ↓	–	100	ns	–
t_{WC}	CLK delay for loading	0	55	ns	–
t_{WG}	Gate delay for sampling	−5	40	ns	–
t_{WO}	OUT delay from mode write	–	240	ns	–
t_{CL}	CLK setup for count latch	−4	40	ns	–

[1] Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
[2] In modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 70 ns of the rising clock edge may not be detected.

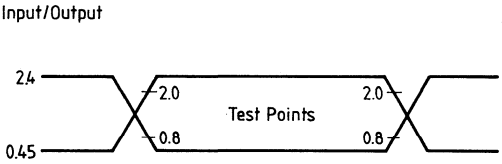
AC Testing Waveforms

Test Loadings



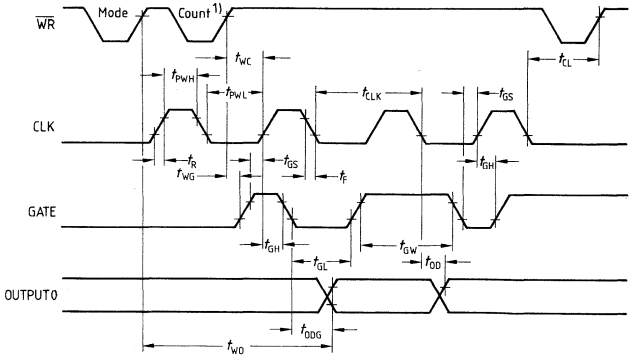
C_L = 150 pF
C_L Includes Jig Capacitance

Measurement Reference Levels



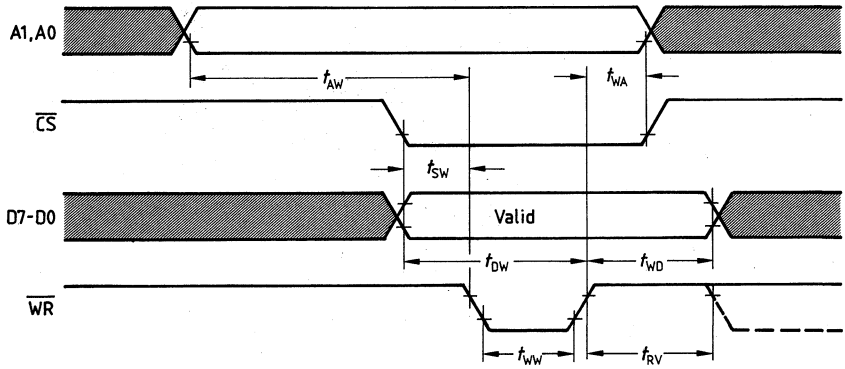
AC Testing: Inputs are driven at 2.4V for a logic "1" and at 0.45V for a logic "0".

Counter Control Timing

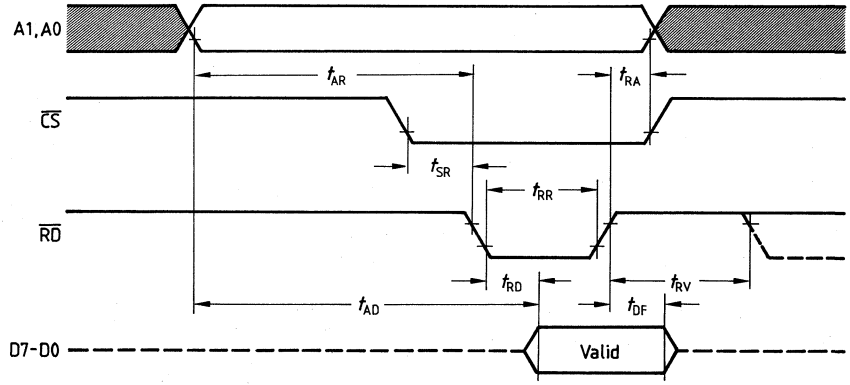


1) Last byte of count being written

Write Cycle Timing



Read Cycle Timing



Ordering Information

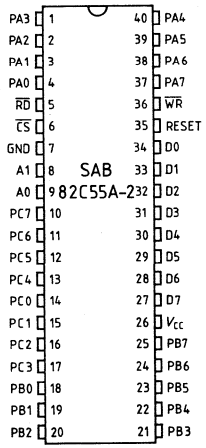
Type	Ordering code	Description
SAB 82C54-P	Q67120-P212	Programmable CMOS interval timer (8 MHz)
SAB 82C54-2-P	Q67120-P253	Programmable CMOS interval timer (10 MHz)

Preliminary

SAB 82C55A-2 CMOS Programmable Peripheral Interface

- Compatible with all Siemens and most other microprocessors
- High-speed "zero wait state" operation with 8 MHz SAB 8086/8088 and SAB 80186/80188
- 24 programmable I/O pins
- Low-power CMOS
- Completely TTL-compatible
- Control word read-back capability
- Direct bit-set/reset capability
- 2.5 mA DC drive capability on all I/O port outputs
- Available in 40-pin dual-in-line plastic package (P-DIP-40)

Figure 1
Pin Configuration



Pin Names

PA 3-0	Port A, Pins 0 to 3
$\overline{RD}$	Read Input
$\overline{CS}$	Chip Select
A 1-0	Address Inputs
PC 7-4	Port C, Pins 4 to 7
PC 0-3	Port C, Pins 0 to 3
PB 0-7	Port B, Pins 0 to 7
D 7-0	Data Bus (bidirectional)
RESET	Reset Input
$\overline{WR}$	Write Input
PA 7-4	Port A, Pins 4 to 7

The SAB 82C55A-2 is a high-performance, CMOS version of the industry standard 8255A general-purpose, programmable I/O device which is designed for use with all Siemens and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12, and used in 3 major modes of operation. The SAB 82C55A-2 is pin-compatible with the NMOS 8255A and 8255A-5.

In mode 0 , each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs.

In mode 1, each group may be programmed to have 8 lines of input or output. Three of the remaining 4 pins are used for handshaking and interrupt control signals. Mode 2 is a strobed bidirectional bus configuration.

The SAB 82C55A-2 is fabricated in Siemens CMOS technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The SAB 82C55A-2 is available in a 40-pin dual-in-line plastic package.

Pin Definitions and Functions

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>PA3-PA0</td><td>1-4</td><td>I/O</td><td>PORT A, PINS 0–3
Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.</td></tr>
<tr><td>$\overline{RD}$</td><td>5</td><td>I</td><td>$\overline{READ}$ CONTROL
This input is low during CPU read operations.</td></tr>
<tr><td>$\overline{CS}$</td><td>6</td><td>I</td><td>$\overline{CHIP\ SELECT}$
A low on this input enables the SAB 82C55A-2 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.</td></tr>
<tr><td>A1-A0</td><td>8-9</td><td>I</td><td>ADDRESS INPUTS 1 AND 0
These input signals, in conjunction $\overline{RD}$ and $\overline{WR}$, control the selection of one the three ports or of the control word registers.
<table>
<tr><th>A1</th><th>A0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Input Operation (read)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port A - Data Bus</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Port B - Data Bus</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port C - Data Bus</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Control Word - Data Bus</td></tr>
<tr><td colspan="5"></td><td>Output Operation (write)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port A</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port B</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port C</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Control</td></tr>
<tr><td colspan="5"></td><td>Disable Function</td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>Data Bus - Tristate</td></tr>
<tr><td>X</td><td>X</td><td>1</td><td>1</td><td>0</td><td>Data Bus - Tristate</td></tr>
</table></td></tr>
<tr><td>PC7-PC4</td><td>10-13</td><td>I/O</td><td>PORT C, PINS 4-7
Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch, and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.</td></tr>
<tr><td>PC0-PC3</td><td>14-17</td><td>I/O</td><td>PORT C, PINS 0-3
Lower nibble of port C.</td></tr>
<tr><td>PB0-PB7</td><td>18-25</td><td>I/O</td><td>PORT B, PINS 0-7
An 8-bit data output latch/buffer and an 8-bit data input buffer.</td></tr>
</table>

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
D7-D0	27-34	I/O	**DATA BUS** Bidirectional, tristate data bus lines, connected to system data bus.
RESET	35	I	**RESET** A high on this input clears the control register and all ports are set to the input mode.
$\overline{WR}$	36	I	**$\overline{WRITE\ CONTROL}$** This input is low during CPU write operations.
PA7-PA4	37-40	I/O	**PORT A, PINS 4-7** Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.
V_{CC}	26	–	**POWER SUPPLY** (+5 V)
GND	7	–	**SYSTEM GROUND** (0 V)

Functional Description

General

The SAB 82C55A-2 is a programmable peripheral interface device designed for use in Siemens microcomputer systems. Its function is that of a general-purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the SAB 82C55A-2 is programmed by system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This tristate bidirectional 8-bit buffer is used to interface the SAB 82C55A-2 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both data and control or status words. It accepts inputs from the CPU address and control buses and, in turn, issues commands to both of the control groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the SAB 82C55A-2. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the SAB 82C55A-2.

Each of the control blocks (group A and group B) accepts "commands" from the read/write control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control group A - port A and upper port C (C7-C4)
Control group B - port B and lower port C (C3-C0)

The control word register can be both written and read as shown in the address decode table in the pin description. Figure 5 shows the control word format for both read and write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

The SAB 82C55A-2 contains three 8-bit ports (A, B, and C). All of them can be configured in a wide variety of functional characteristics by the system software, but each has its own special features or "personality" to further enhance the power and flexibility of the SAB 82C55A-2.

Port A One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both "pullup" and "pulldown" bus-hold devices are present on port A.

Port B One 8-bit data input/output latch/buffer. Only "pullup" bus-hold devices are present on port B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pullup" bus-hold devices are present on port C.

See figure 3 for the bus-hold circuit configuration for ports A, B, and C.

Figure 2
Block Diagram

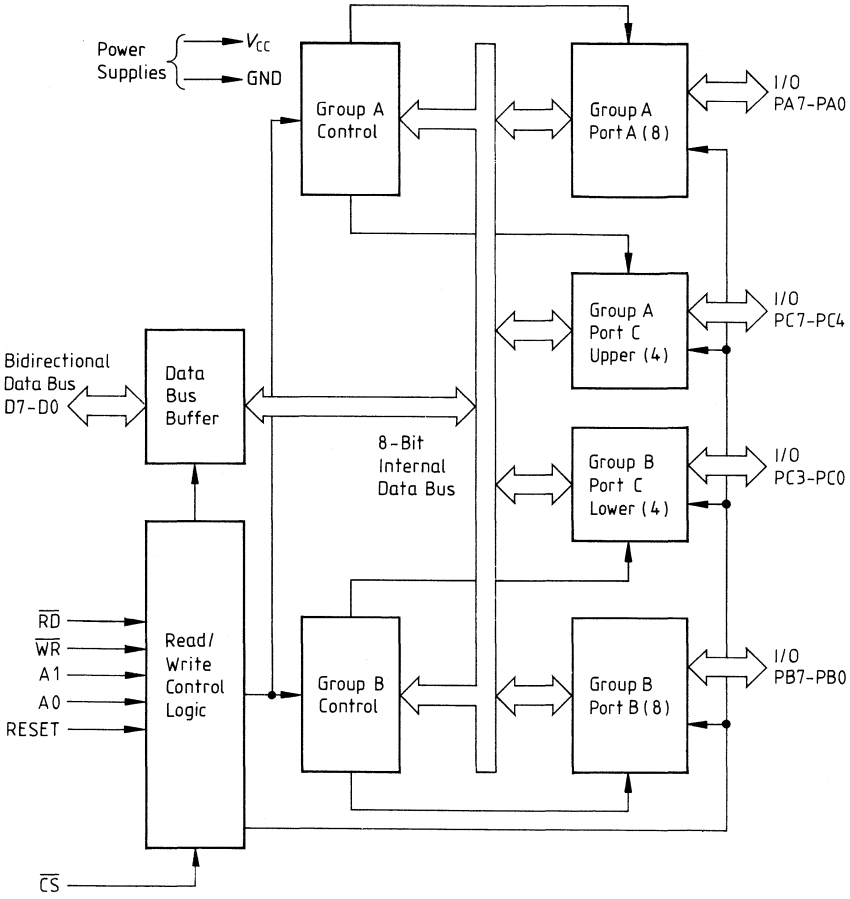
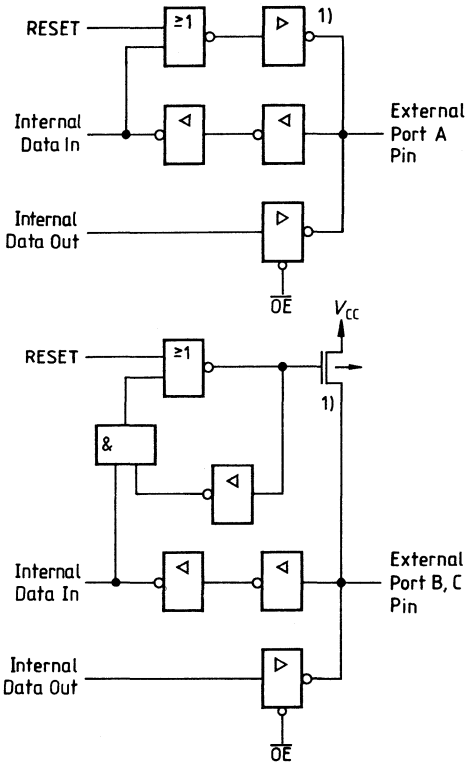


Figure 3
Port A, B, C, Bus-Hold Configuration



[1]) Port pins loaded with more than 20 pF capacitance may not have their logic level guaranteed following a hardware reset.

Operational Description

Mode Selection

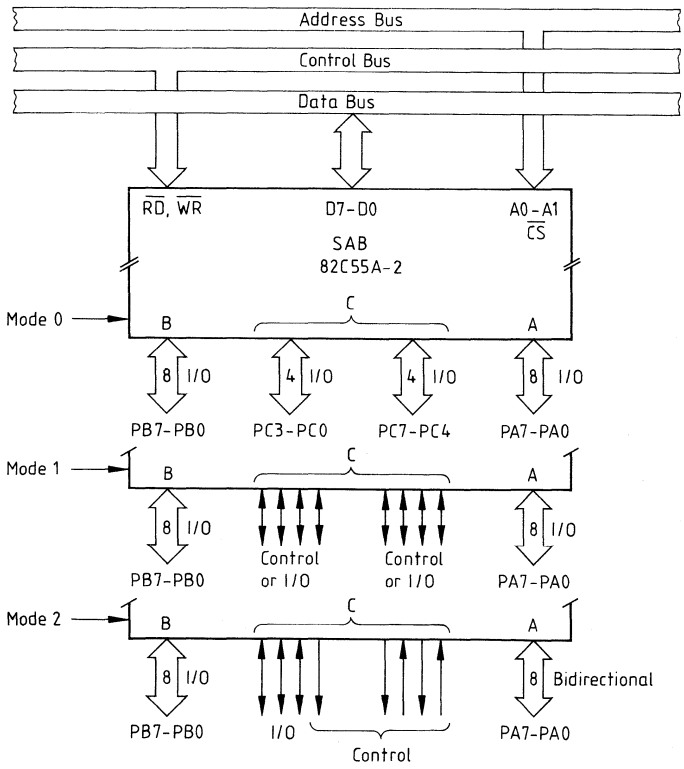
There are three basic modes of operation that can be selected by the system software:

Mode 0 – basic input/output
Mode 1 – strobed input/output
Mode 2 – bidirectional bus

When the reset input goes high all ports will be set to the input mode with all 24 port lines held at a logic "one" level by the internal bus-hold devices (see footnote in figure 3). After the reset is removed the SAB 82C55A-2 can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in "all CMOS" designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single SAB 82C55A-2 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for port A and port B can be separately defined, while port C is divided into two portions as required by the port A and port B definitions. All of the output registers, including the status flipflops, will be reset whenever the mode is changed.

Figure 4
Basic Mode Definitions and Bus Interface

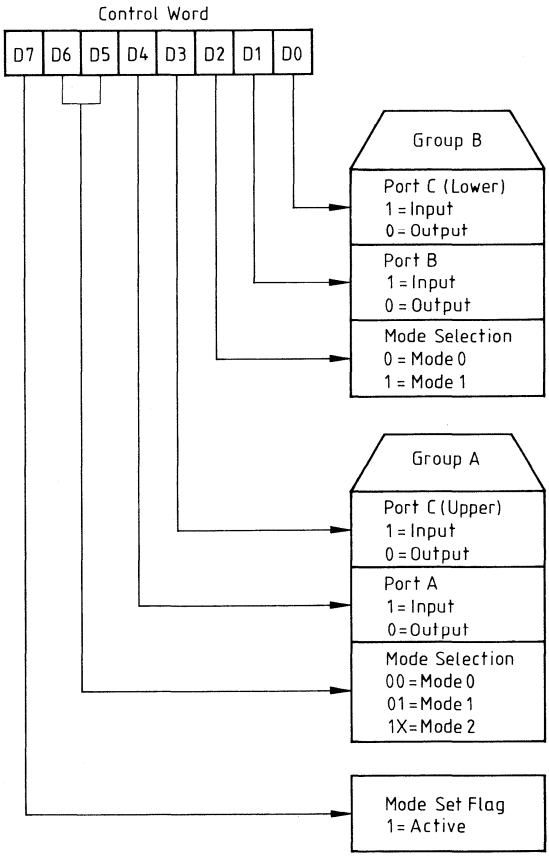


Modes may be combined so that their functional definition can be tailored to almost any I/O structure.

For instance: group B can be programmed in mode 0 to monitor simple switch closings or display computational results, group A could be programmed in mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the SAB 82C55A-2 has taken into account things such as efficient pc board layout, control signal definition versus pc layout, and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Figure 5
Mode Definition Format



Single Bit Set/Reset Feature

Any of the eight bits of port C can be set or reset using a single output instruction. This feature reduces software requirements in control-based applications.

When port C is being used as status/control for port A or B, these bits can be set or reset by using the bit set/reset operation just as if they were data output ports.

Interrupt Control Functions

When the SAB 82C55A-2 is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flipflop, using the bit set/reset function of port C.

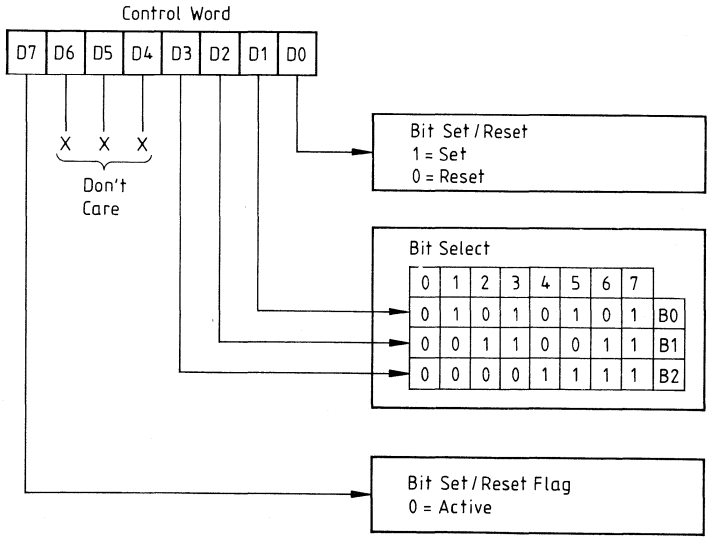
This function permits the programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flipflop definition:

(bit set) – INTE is set – interrupt enable
(bit reset) – INTE is reset – interrupt disable

Note:
All mask flipflops are automatically reset during mode selection and device reset.

Figure 6
Bit Set/Reset Format



Operating Modes

Mode 0 (basic input/output)
This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 basic functional definitions:
- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different I/O configurations are possible in this mode

Figure 7
Mode 0 (basic input)

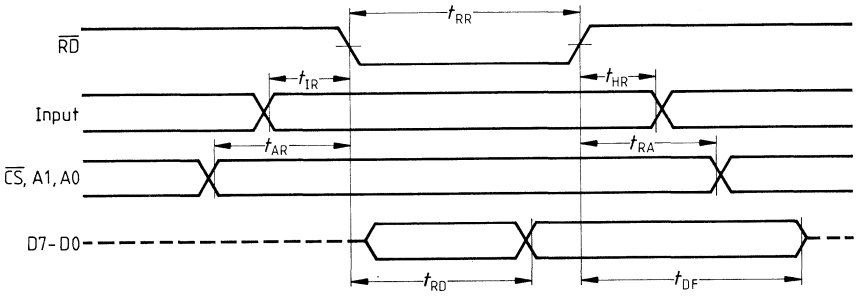
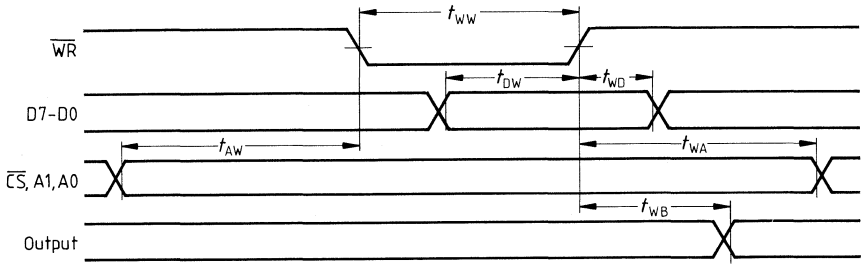


Figure 8
Mode 0 (basic output)



Mode 0 Port Definition

A		B		Group A		No.	Group B	
D4	D3	D1	D0	Port A	Port C (Upper)		Port B	Port C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 1 (strobed input/output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 basic functional definitions:

- Two groups (group A and group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{\text{STB}}$ (strobe input) – A low on this input loads data into the input latch.

IBF (input buffer full flipflop) – A high on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. The IBF is set by the $\overline{\text{STB}}$ input being low and is reset by the rising edge of the $\overline{\text{RD}}$ input.

INTR (interrupt request) – A high on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{\text{STB}}$ = 1, IBF = 1, and INTE = 1. It is reset by the falling edge of $\overline{\text{RD}}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A – Controlled by bit set/reset of PC4

INTE B – Controlled by bit set/reset of PC2

Figure 9
Mode 1 Input

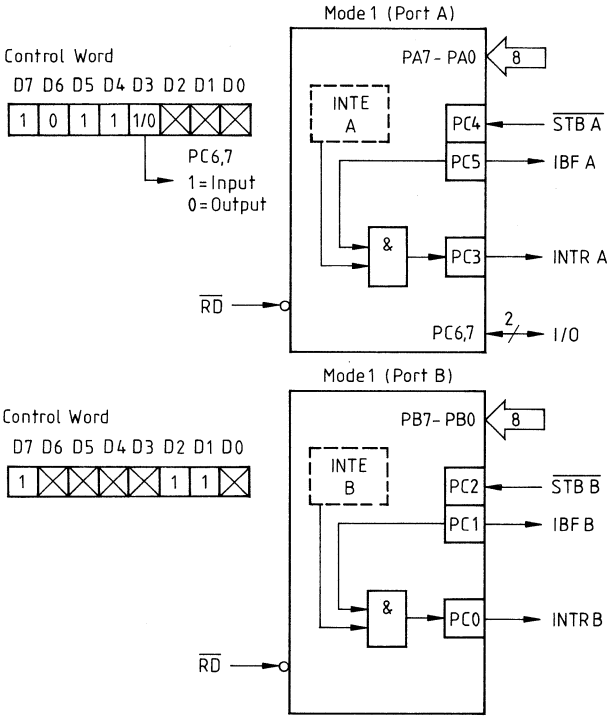
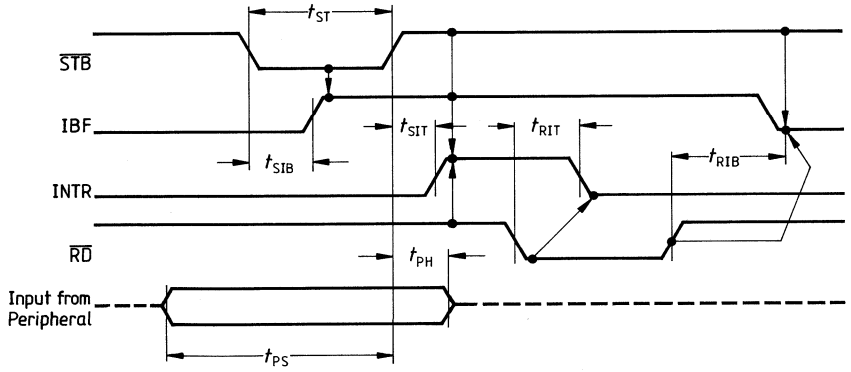


Figure 10
Mode 1 (strobed input)



Output Control Signal Definition

$\overline{OBF}$ ($\overline{OBF}$ output buffer full flipflop) – The $\overline{OBF}$ output will go low to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ flipflop will be set by the rising edge of the $\overline{WR}$ input and reset by the $\overline{ACK}$ input being low.

$\overline{ACK}$ ($\overline{ACK}$ acknowledge input) – A low on this input informs the SAB 82C55A-2 that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (interrupt request) – A high on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ = 1, $\overline{OBF}$ = 1 and INTE = 1. It is reset by the falling edge of $\overline{WR}$.

INTE A – Controlled by bit set/reset of PC6.

INTE B – Controlled by bit set/reset of PC2.

Figure 11
Mode 1 Output

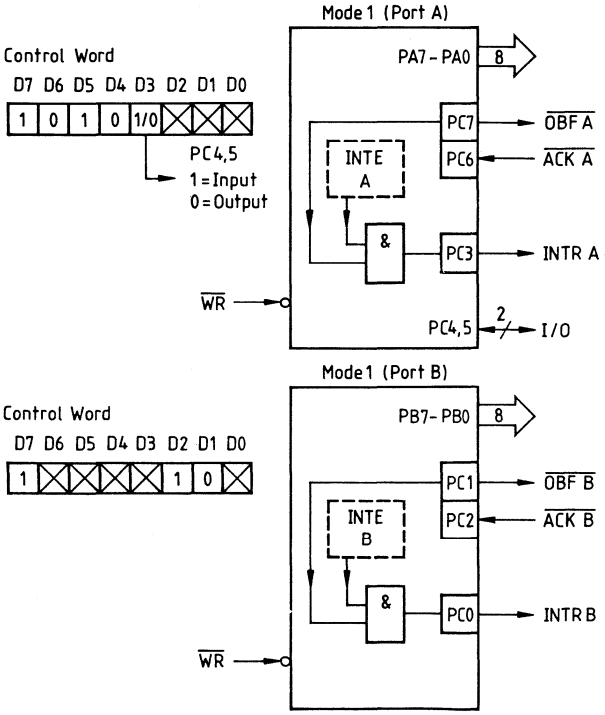
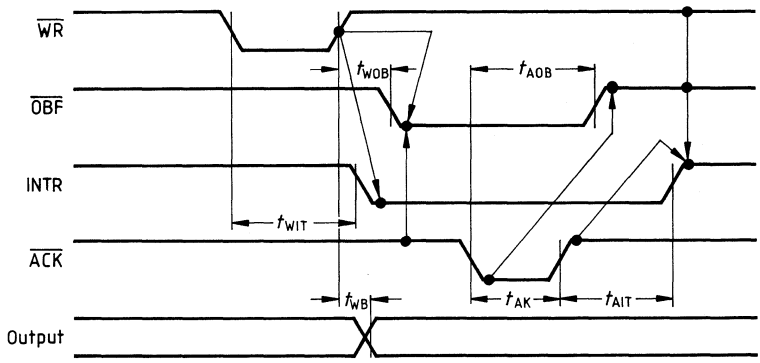


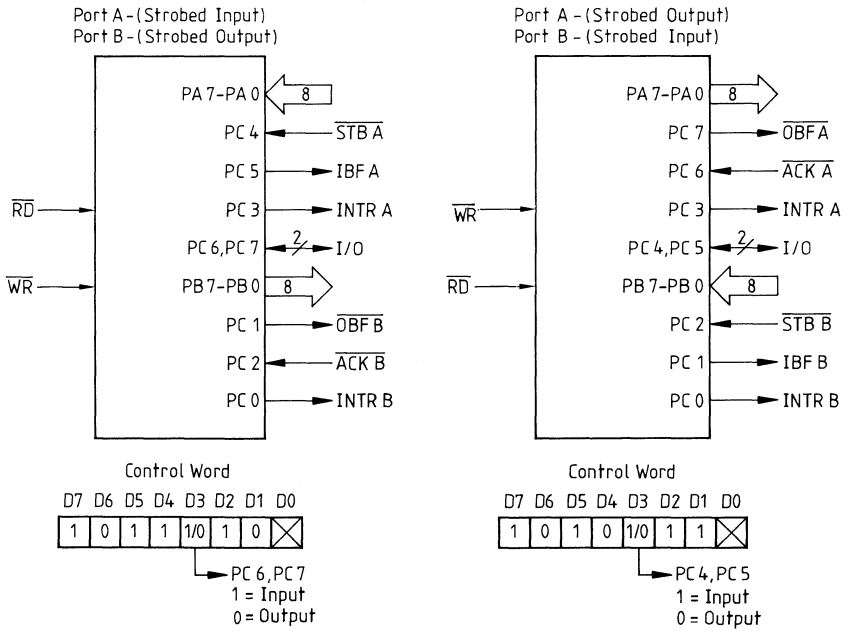
Figure 12
Mode 1 (strobed output)



Combinations of mode 1

Port A and port B can be individually defined as input or output in mode 1 to support a wide variety of strobed I/O applications.

Figure 13
Combinations of Mode 1



Mode 2 (strobed bidirectional bus I/O)
This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a manner similar to mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 basic functional definitions:

- Used in group A only.
- One 8-bit, bidirectional bus port (port A) and a 5-bit control port (port C).
- Both inputs and outputs are latched.
- The 5-bit control port (port C) is used for control and status for the 8-bit, bidirectional bus port (port A).

Bidirectional Bus I/O Control Signal Definition

INTR (interrupt request) – A high on this output can be used to interrupt the CPU for input or output operation.

Output Operations

$\overline{\text{OBF}}$ (output buffer full) – The $\overline{\text{OBF}}$ output will go low to indicate that the CPU has written data out to port A.

$\overline{\text{ACK}}$ (acknowledge) – A low on this input enables the tristate output buffer of port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTE 1 (the INTE flipflop associated with $\overline{\text{OBF}}$) – Controlled by bit set/reset of PC6.

Input Operations

$\overline{\text{STB}}$ (strobe input) – A low on this input loads data into the input latch.

IBF (input buffer full flipflop) – A high on this output indicates that data has been loaded into the input latch.

INTE 2 (the INTE flipflop associated with IBF) – Controlled by set/reset of PC4.

Figure 14
Mode Control Word

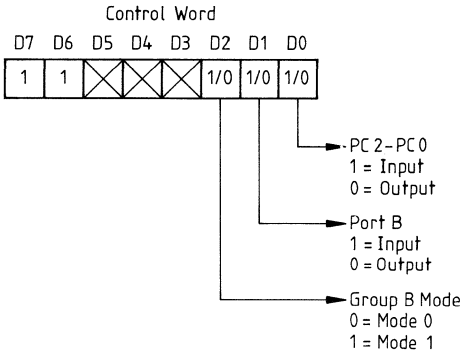


Figure 15
Mode 2

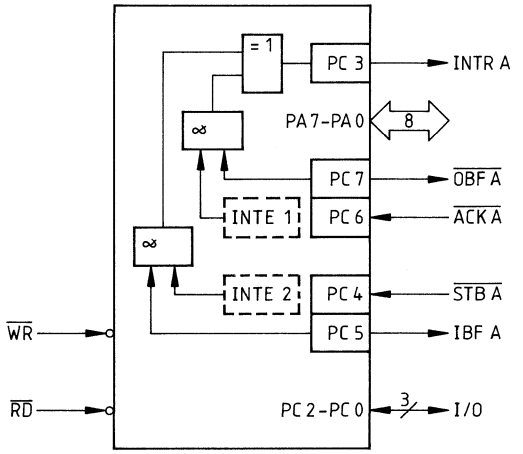
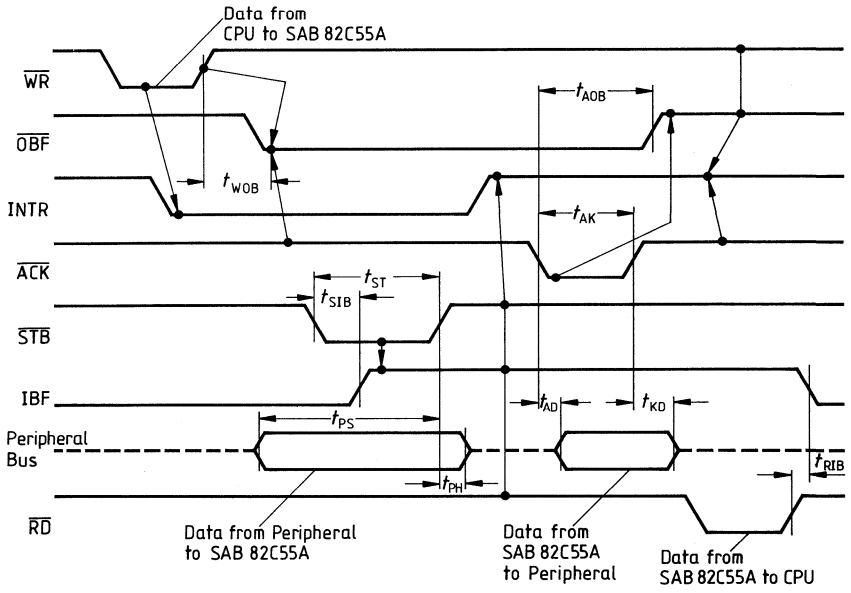
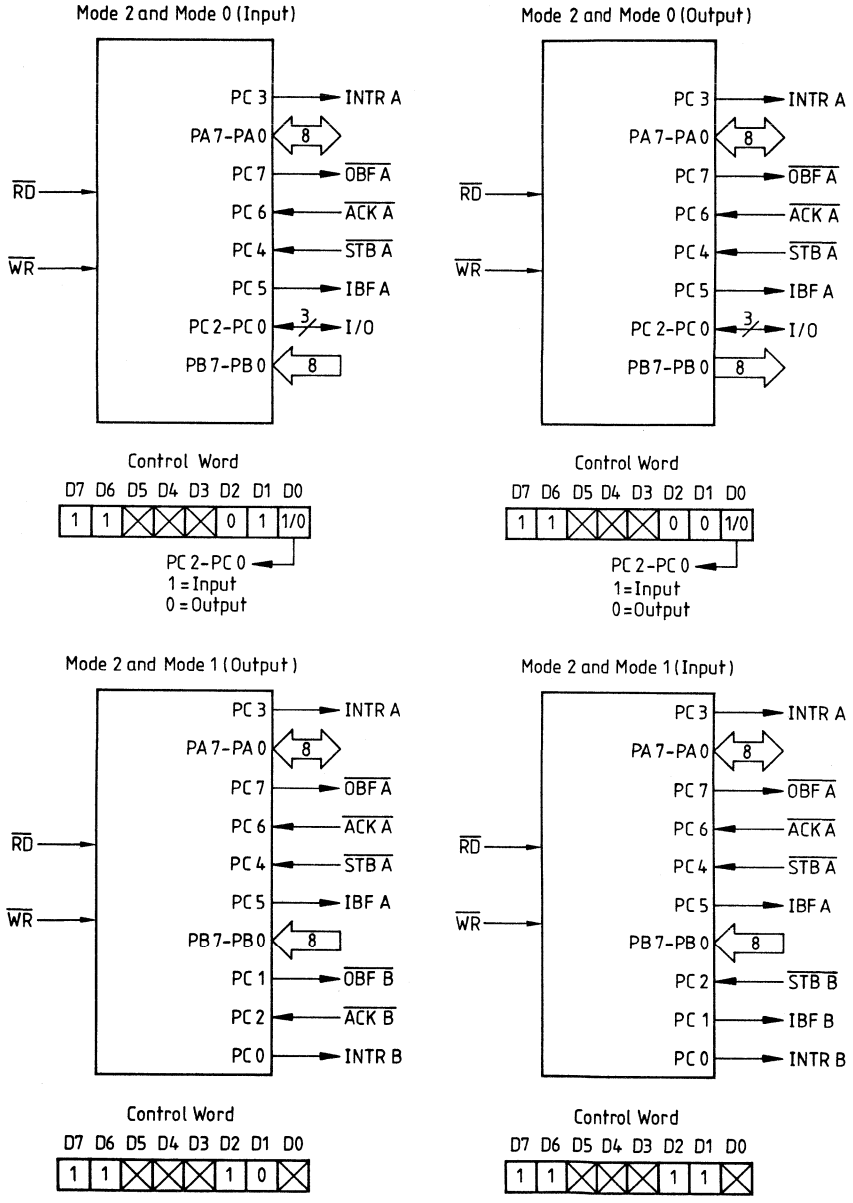


Figure 16
Mode 2 (bidirectional)



Note:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

Figure 17
Mode 1/4 Combinations



Mode Definition Summary

	Mode 0		Mode 1		Mode 2	
	In	Out	In	Out	Group A Only	
PA0	In	Out	In	Out	⟷	
PA1	In	Out	In	Out	⟷	
PA2	In	Out	In	Out	⟷	
PA3	In	Out	In	Out	⟷	
PA4	In	Out	In	Out	⟷	
PA5	In	Out	In	Out	⟷	
PA6	In	Out	In	Out	⟷	
PA7	In	Out	In	Out	⟷	
PB0	In	Out	In	Out	–	Mode 0 or Mode 1 Only
PB1	In	Out	In	Out	–	
PB2	In	Out	In	Out	–	
PB3	In	Out	In	Out	–	
PB4	In	Out	In	Out	–	
PB5	In	Out	In	Out	–	
PB6	In	Out	In	Out	–	
PB7	In	Out	In	Out	–	
PC0	In	Out	INTR B	$\overline{\text{INTR B}}$	I/O	
PC1	In	Out	IBF B	$\overline{\text{OBF B}}$	I/O	
PC2	In	Out	$\overline{\text{STB B}}$	$\overline{\text{ACK B}}$	I/O	
PC3	In	Out	INTR A	INTR A	INTR A	
PC4	In	Out	$\overline{\text{STB A}}$	I/O	$\overline{\text{STB A}}$	
PC5	In	Out	IBF A	I/O	IBF A	
PC 6	In	Out	I/O	$\overline{\text{ACK A}}$	$\overline{\text{ACK A}}$	
PC7	In	Out	I/O	$\overline{\text{OBF A}}$	$\overline{\text{OBF A}}$	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of the port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "set mode" command.

While port C is read, the state of all the port C lines, except the $\overline{\text{ACK}}$ and $\overline{\text{STB}}$ lines, will be placed on the data bus. In place of the $\overline{\text{ACK}}$ and $\overline{\text{STB}}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated in figure 20.

Through a "write port C" command, only the port C pins programmed as outputs in a mode 0 group can be written to. No other pins can be affected by a "write port C" command, nor can the interrupt enable flags be accessed. To write to any port C output programmed as an output in a mode 1 group or to change an interrupt enable flag, the "set/reset port C bit" command must be used.

With a "set/reset port C bit" command, any port C line programmed as an output (including INTR, IBF and $\overline{\text{OBF}}$) can be written to, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{\text{ACK}}$ and $\overline{\text{STB}}$ lines, associated with port C are not affected by a "set/reset port C bit" command. Writing to the corresponding port C bit positions of the $\overline{\text{ACK}}$ and $\overline{\text{STB}}$ lines with the "set/reset port C bit" command will affect the group A and group B interrupt anable flags, as illustrated in figure 20.

Current Drive Capability

Any output on port A, B or C can sink or source 2.5 mA. This feature allows the SAB 82C55A-2 to directly drive darlington-type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In mode 0, Port C transfers data to or from the peripheral device. When the SAB 82C55A-2 is programmed to function in modes 1 or 2, port C generates or accepts "handshaking" signals with the peripheral device. Reading the contents of port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from port C. A normal read operation of port C is executed to perform this function.

Figure 18
Mode 1 Status Word Format

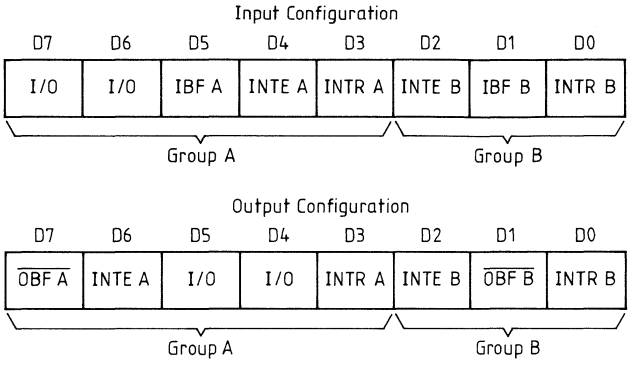


Figure 19
Mode 2 Status Word Format

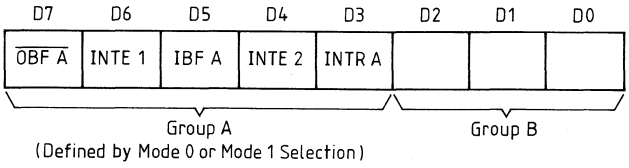


Figure 20
Interrupt Enable Flags in Modes 1 and 2

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (mode)
INTE B	PC2	$\overline{\text{ACK B}}$ (output mode 1) or $\overline{\text{STB B}}$ (input mode 1)
INTE A2	PC4	$\overline{\text{STB A}}$ (input mode 1 or mode 2)
INTE A1	PC6	$\overline{\text{ACK A}}$ (output mode 1 or mode 2)

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Supply voltage	−0.5 to +8.0 V
Operating voltage	4 to 7 V
Voltage on any input	GND −2 V to $+V_{CC}$ +0.5 V
Voltage on any output	GND −0.5 V to V_{CC} +0.5 V
Power dissipation	1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ±10%, GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage	2.0	V_{CC}+0.5	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} −0.4	–	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input leakage current	–	±1	µA	V_{IN} = V_{CC} to 0 V [1]
I_{OFL}	Output float leakage current	–	±10	µA	V_{IN} = V_{CC} to 0 V [2]
I_{DAR}	Darlington drive current	−2.5	–	mA	Ports A, B, C Test condition 3
I_{PHL}	Port hold low leakage current	+50	+300	µA	V_{OUT} = 1.0 V Port A only
I_{PHH}	Port hold high leakage current	−50	−300	µA	V_{OUT} = 3.0 V Ports A, B, C
I_{PHLO}	Port hold low overdrive current	−350	–	µA	V_{OUT} = 0.8 V
I_{PHHO}	Port hold high overdrive current	+350	–	µA	V_{OUT} = 3.0 V
I_{CC}	V_{CC} supply current, average	–	5	mA	[3]
I_{CCSB}	V_{CC} supply current, standby	–	10	µA	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open

Capacitance

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	Unmeasured pins returned to GND
C_{IO}	I/O capacitance	–	20	pF	

[1]) Pins A1, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, RESET
[2]) Data bus; ports B, C
[3]) I/O write cycle time: 1 µs

AC Characteristics

$T_A = 0$ to 70°C; $V_{CC} = +5\,V \pm 10\%$; GND = 0 V

Bus Parameters

Read Cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AR}	Address stable before $\overline{RD}\downarrow$	0	–	ns	–
t_{RA}	Address hold time after $\overline{RD}\uparrow$	0	–	ns	–
t_{RR}	$\overline{RD}$ pulse width	150	–	ns	–
t_{RD}	Data delay from $\overline{RD}\downarrow$	–	100	ns	[1]
t_{DF}	$\overline{RD}\uparrow$ to data floating	10	40	ns	[2]
t_{RV}	Recovery time between $\overline{RD}/\overline{WR}$	150	–	ns	–

Write Cycle

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AW}	Address stable before $\overline{WR}\downarrow$	0	–	ns	–
t_{WA}	Address hold time after $\overline{WR}\uparrow$	20	–	ns	Ports A and B
		20	–	ns	Port C
t_{WW}	$\overline{WR}$ pulse width	100	–	ns	–
t_{DW}	Data setup time before $\overline{WR}\uparrow$	100	–	ns	–
t_{WD}	Data hold time after $\overline{WR}\uparrow$	30	–	ns	Ports A and B
		30	–	ns	Port C

[1] INTR ↑ may occur as early as $\overline{WR}\downarrow$.

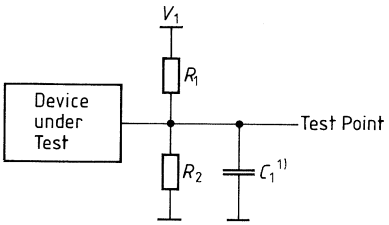
[2] Pulse width of initial reset pulse after power-on must be at least 50 µs. Subsequent reset pulses may be 500 ns minimum.

Other Timings

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{WB}	$\overline{WR}$ = 1 to output	–	350	ns	[1]
t_{IR}	Peripheral data before $\overline{RD}$	0	–	ns	–
t_{HR}	Peripheral data after $\overline{RD}$	0	–	ns	–
t_{AK}	$\overline{ACK}$ pulse width	200	–	ns	–
t_{ST}	$\overline{STB}$ pulse width	100	–	ns	–
t_{PS}	Peripheral data before $\overline{STB}$ high	20	–	ns	–
t_{PH}	Peripheral data after $\overline{STB}$ high	50	–	ns	–
t_{AD}	$\overline{ACK}$ = 0 to output	–	175	ns	[1]
t_{KD}	$\overline{ACK}$ = 1 to output float	20	250	ns	[2]
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0	–	150	ns	[1]
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1	–	150	ns	[1]
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1	–	150	ns	[1]
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0	–	150	ns	[1]
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0	–	200	ns	[1]
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1	–	150	ns	[1]
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1	–	150	ns	[1]
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0	–	200	ns	[1]
t_{RES}	Reset pulse width	500	–	ns	[2]

[1]) INTR ↑ may occur as early as $\overline{WR}$ ↓.
[2]) Pulse width of initial reset pulse after power-on must be at least 50 µs. Subsequent reset pulses may be 500 ns minimum.

AC Test Circuit



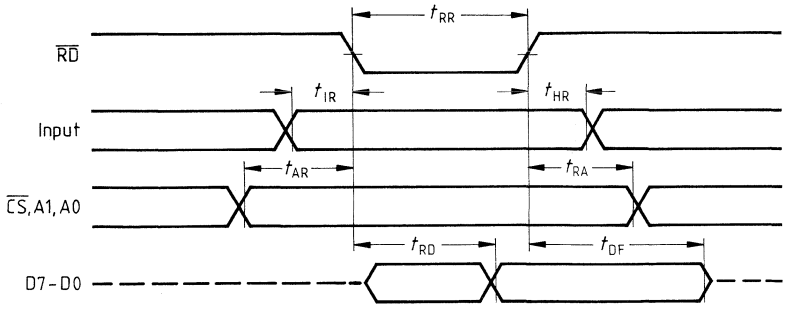
[1]) Includes Stray and Jig Capacitance

Test Condition Definition

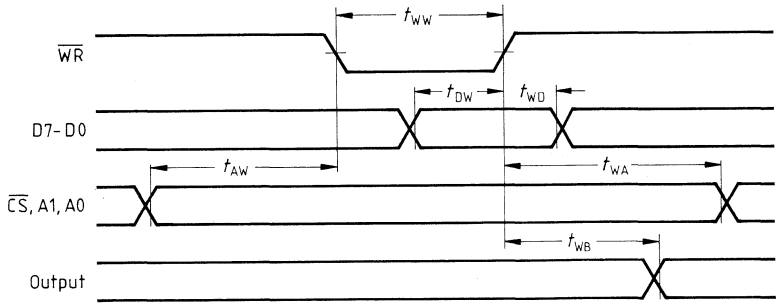
Test Condition	V_1	R_1	R_2	C_1
1	1.7 V	523 Ω	Open	150 pF
2	5.0 V	2 kΩ	1.7 kΩ	50 pF
3	1.5 V	750 Ω	Open	Open

Waveforms

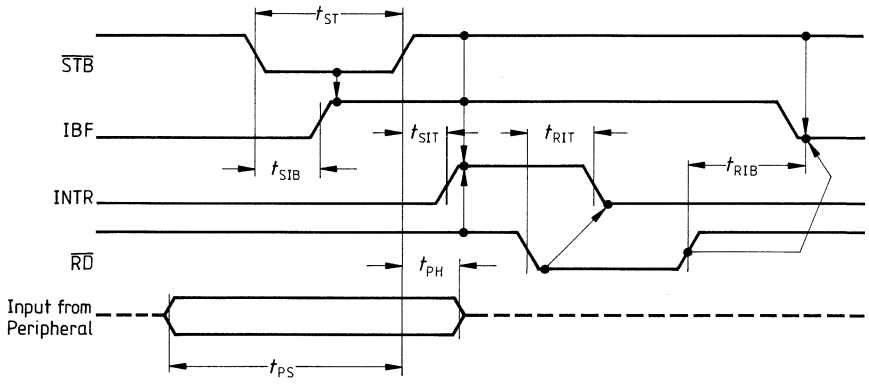
Mode 0 (basic input)



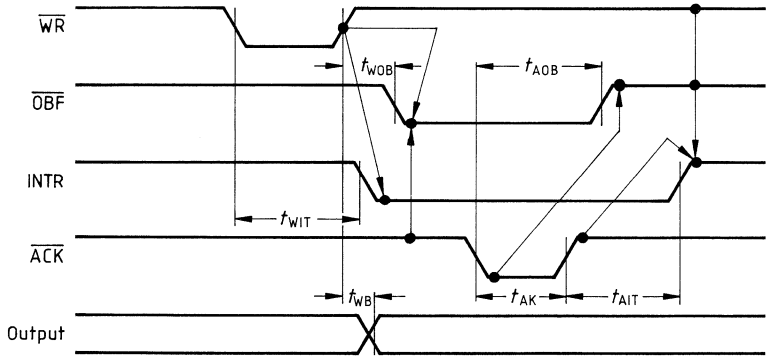
Mode 0 (basic output)



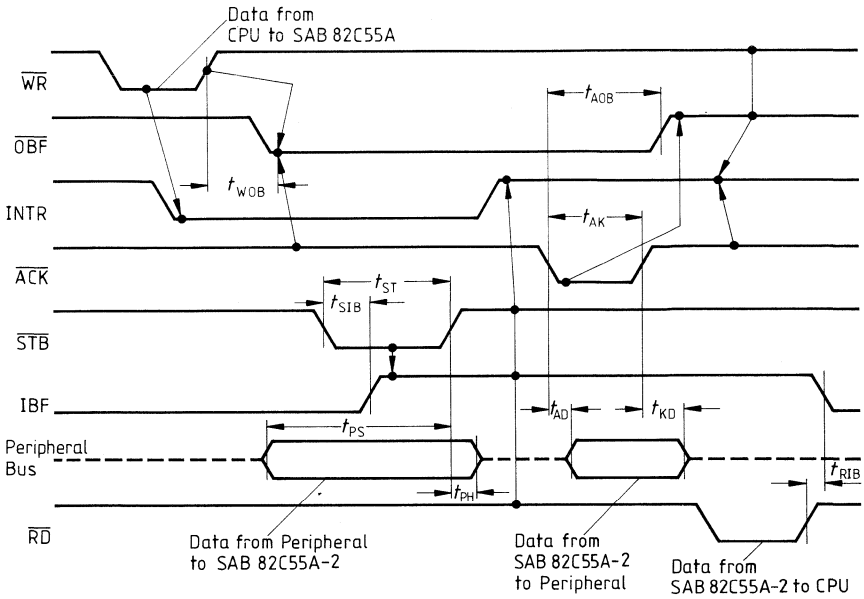
Mode 1 (strobed input)



Mode 1 (strobed output)

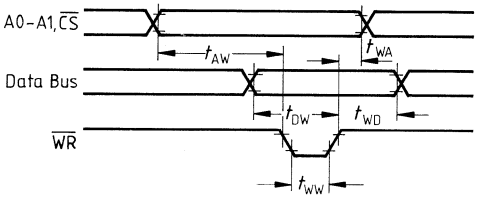


Mode 2 (bidirectional)

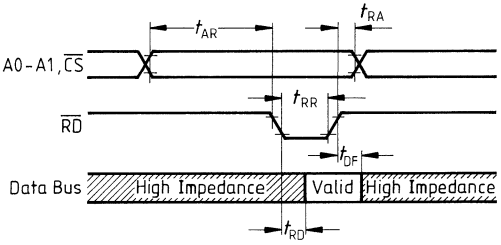


Note:
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

Write Timing



Read Timing



Ordering Information

Type	Ordering code	Description
SAB 82C55A-2-P	Q67120-P213	Programmable peripheral interface

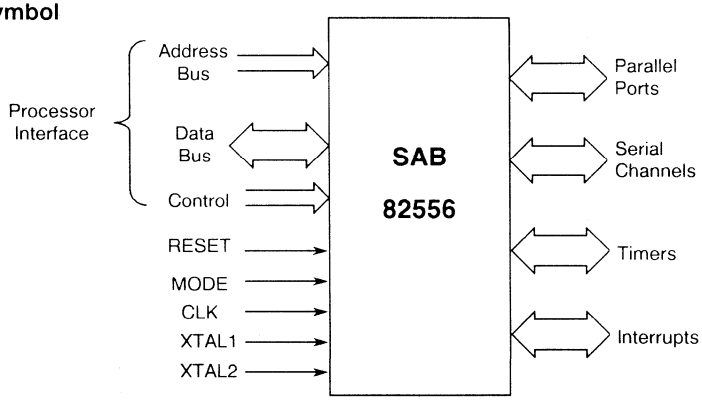
SIEMENS

SAB 82556
Universal System Interface Controller

Advance Information

- Up to three parallel 8-bit I/O ports
- 2 serial channels (one with DMA support)
- Data rate up to 4 MBaud
- Supports HDLC protocol
- On-chip clock generator
- Three 16-bit timer/counters
- Programmable interrupt controller
- 8-bit or 16-bit data bus
- Bus interface compatible with Intel-type or Motorola-type processors

Logic Symbol



The SAB 82556 Universal System Interface Controller provides 8-bit and 16-bit systems with widely used peripheral functions like interrupt controller, timers, parallel ports and serial channels. The SAB 82556's bus interface uses an 8-bit or 16-bit data bus and can be programmed to be compatible with Intel-type or Motorola-type processors. By integration and connection of the individual functional units on-chip, the SAB 82556 reduces the number of elements needed to interface a microprocessor system to its environment.

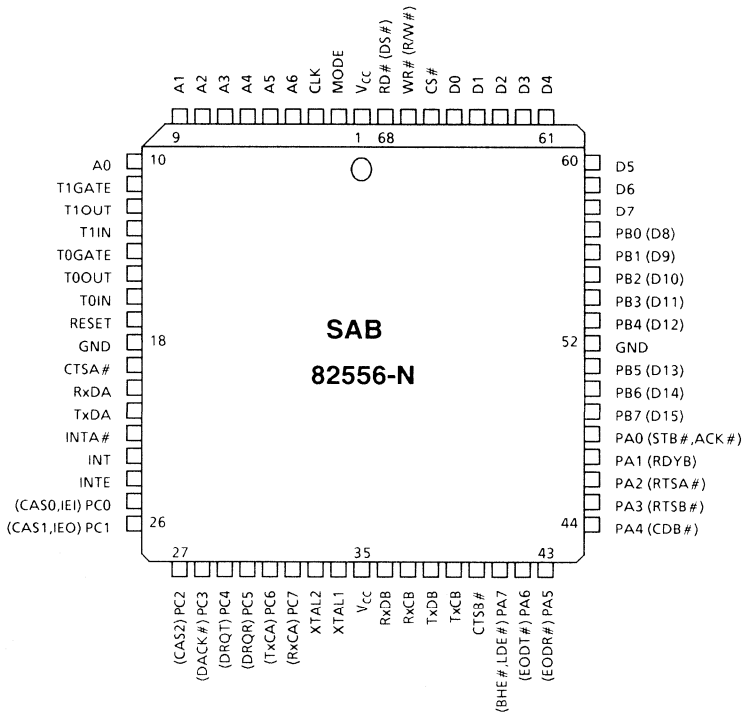
The SAB 82556 is fabricated in Siemens ACMOS technology and comes in a 68-pin plastic leaded chip carrier package.

Ordering Information

Type	Ordering Code	Description
SAB 82556-N	Q67120-P287	Universal System Interface Controller (PL-CC-68)

Pin Configuration

Top View of PL-CC-68



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
MODE	2	I	**Bus Mode Control** Selects the bus operating mode. High level selects Motorola bus mode. Low level selects Intel bus mode.
CLK	3	I	**System Cock Input** This input receives a clock signal from the system and can be used as timer clock.
A6-A0	4-10	I	**Address** These input signals select one of the registers in conjunction with the following access control signals: – DS# and R/W# in Motorola bus mode – RD# and WR# in Intel bus mode
T1GATE	11	I	**Timer 1 Gate** Control input of timer 1
T1OUT	12	O	**Timer 1 Output** Output of timer 1
T1IN	13	I	**Timer 1 Input** External clock input of timer 1
T0GATE	14	I	**Timer 0 Gate** Control input of timer 0
T0OUT	15	O	**Timer 0 Output** Output of timer 0
T0IN	16	I	**Timer 0 Input** External clock input of timer 0
RESET	17	I	**Reset** This active high input resets the USIC into the initial inactive default state.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CTSA#, CTSB#	19, 40	I	**Clear to Send#** These active low inputs serve several purposes. In auto-mode 0 they accept strobe signals which define time slots for transmission. In auto-modes 1 and 2 they accept transmission control signals. The TxD outputs can be fed back to these inputs for collision detection. They also may be used for general purpose input.
RxDA, RxDB	20, 36	I	**Receive Data** Active high inputs for receive data.
TxDA, TxDB	21, 38	O	**Transmit Data** Active high outputs for transmit data.
INTA#	22	I	**Interrupt Acknowledge#** This active low input releases the USIC's interrupt vector onto the data bus. In Intel bus mode two INTA# pulses are requested. In Motorola bus mode one INTA# pulse is requested together with a DS# pulse.
INT	23	O	**Interrupt** This active high output sends an interrupt request to the host CPU or the master interrupt controller.
INTE	24	I	**Interrupt Extension** This active high input receives level triggered interrupt requests from an external source or from the slave interrupt controller.
PC0-PC7	25-32	I/O	**Parallel Port C** Each pin of port C serves for general purpose input or output or can be used as special purpose control pin (see "Alternate Pin Definitions").
XTAL2, XTAL1	33, 34	I	**Crystal Input** A fundamental mode crystal is connected to these pins. An external CMOS level clock signal can be fed to XTAL2.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
RxCB	37	I/O	**Receive Clock (Channel B)** This pin accepts the receiver clock signal. Alternatively it may output the baudrate generator clock, the DPLL clock or the receive bit clock (ASYNC mode). If none of these functions is selected, it can be used for general purpose input.
TxCB	39	I/O	**Transmit Clock (Channel B)** This pin accepts the receiver or transmitter clock signal. Alternatively it may output the internal oscillator clock. If none of these functions is selected, it can be used for general purpose input.
PA7-PA0	41-48	I/O	**Parallel Port A** Each pin of port A serves for general purpose input or output or can be used as special purpose control pin (see "Alternate Pin Definitions"). Also each pin may generate a level or edge triggered interrupt request.
PB7-PB5 PB4-PB0	49-51 53-57	I/O	**Parallel Port B** Each pin of port B serves for general purpose input or output. Port B also realizes the the upper 8 data bus lines for 16-bit bus mode (see "Alternate Pin Definitions").
D7-D0	58-65	I/O	**Data Bus** Bi-directional, tri-state data bus lines, connected to the system data bus. Lower data bus lines for 16-bit bus mode.
CS#	66	I	**Chip Select#** This active low input enables slave accesses to the USIC's registers. During DACK# controlled DMA transfers CS# may be active but is not required.
R/W#	67	I	**Read/Write# (Motorola Bus Mode)** This input distinguishes read accesses (high level) from write accesses (low level).
WR#	67	I	**Write Control (Intel Bus Mode)** This input is low during CPU write operations.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
DS#	68	I	**Data Strobe# (Motorola Bus Mode):** This input is low during CPU slave accesses (direction controlled by R/W#).
RD#	68	I	**Read Control (Intel Bus Mode)** This input is low during CPU read operations.
V_{CC}	1,35	–	**Power Supply** +5V Supply voltage.
GND	18,52	–	**Ground** 0V Reference.

Alternate Pin Definitions

Symbol	Default Symbol	Pin	Input Output	Description
IEI	PC0	25	I	**Interrupt Enable Input (Motorola Bus Mode)** A high level on this input enables the USIC's ICU to request interrupt service (daisy chain cascading in Motorola bus mode). A low level indicates a higher priority request and thus disables the ICU.
IEO	PC1	26	I	**Interrupt Enable Output (Motorola Bus Mode)** This output is connected to the next lower priority device's IEI. A low level indicates that the USIC's ICU (or a higher priority interrupt) is active and disables lower priority devices. A high level enables lower priority devices.
CAS0-CAS2	PC0-PC2	25-27	I/O	**Cascade Lines (Intel Bus Mode)** The CAS lines form a private bus to control a multiple interrupt controller structure in Intel bus mode. These pins are outputs for a master USIC and inputs for a slave USIC.
DACK#	PC3	28	I	**DMA Acknowledge#** This active low input acknowledges a DMA request from the USIC's receiver (DRQR) or transmitter (DRQT). The serviced unit (receiver or transmitter) is identified by RD# or WR# (Intel bus mode) or by R/W# (Motorola bus mode). During DACK# controlled DMA transfers CS# may be active but is not required.
DRQT	PC4	29	O	**DMA Request, Transmitter** This active high output requests DMA service for the USIC's transmitter of channel B (load data to the transmit FIFO).
DRQR	PC5	30	O	**DMA Request, Receiver** This active high output requests DMA service for the USIC's receiver of channel B (fetch data from the receive FIFO).

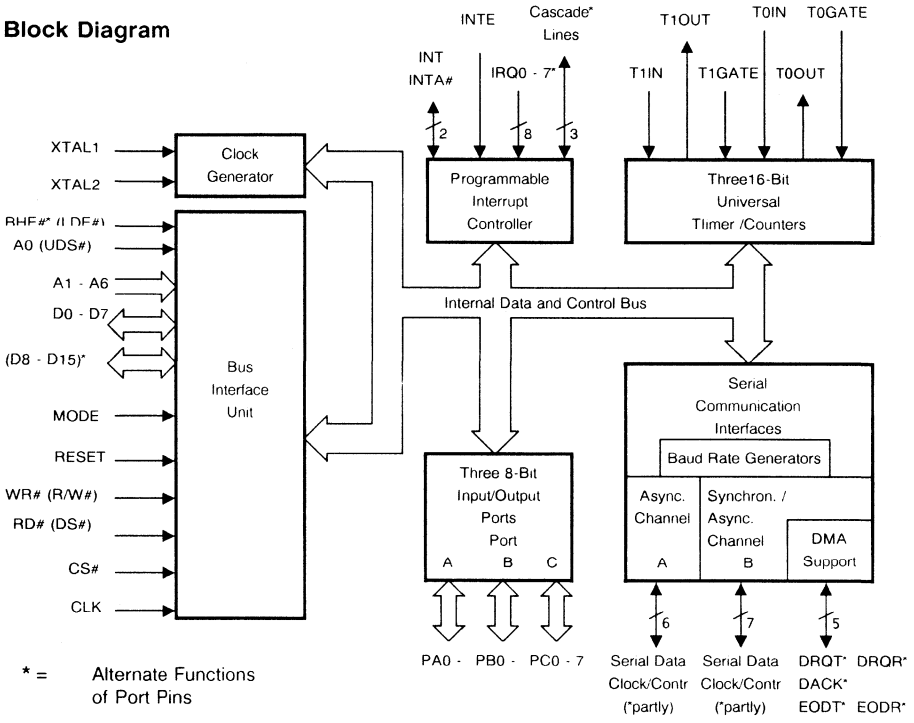
Alternate Pin Definitions (cont'd)

Symbol	Default Symbol	Pin	Type	Description
TxCA	PC6	31	I/O	**Transmit Clock, Channel A** This pin accepts the receiver or transmitter clock signal. Alternatively it may output the internal oscillator clock.
RxCA	PC7	32	I/O	**Receive Clock, Channel A** This pin accepts the receiver clock signal. Alternatively it may output the baudrate generator clock.
LDE#	PA7	41	I	**Lower Data Bus Enable# (Motorola Bus Mode)** This active low input enables data transfers on data lines D7-D0 in 16-bit Motorola bus mode.
BHE#	PA7	41	I	**Bus High Enable# (Intel Bus Mode)** This active low input enables data transfers on data lines D15-D8 in 16-bit Intel bus mode.
EODT#	PA6	42	I	**End of Data, Transmitter#** This active low input is controlled by an intelligent DMA controller (e.g. SAB 82258A). A low level indicates that a complete frame has been loaded to the transmit FIFO (HDLC mode on channel B).
EODR#	PA5	43	O	**End of Data, Receiver#** This active low output controls an intelligent DMA controller. A low level indicates that a complete frame has been fetched from the receive FIFO (HDLC mode on channel B).
CDB#	PA4	44	I	**Carrier Detect, Channel B#** This active low input serves for several purposes. In Auto Mode 0 it accepts a strobe signal which defines timeslots for reception. In Auto Modes 1 and 2 it accepts a transmission control signal. It also may be used for general purpose input.

Alternate Pin Definitions (cont'd)

Symbol	Default Symbol	Pin	Type	Description
RTSB#, RTSA#	PA3, PA2	45, 46	O	**Request to Send#** These active low inputs serve for several purposes. The transmitter can control external line drivers (enable/disable). In ASYNC mode the receiver can control a remote transmitter depending on the filling level of the receive FIFO. They also may be used for general purpose output (e.g. modem control).
RDYB	PA1	47	O	**Ready on Port B** This output is used for handshake controlled transfers on port B. During handshake controlled input a high level indicates that the input data has been latched. During handshake controlled output a low level indicates that output data is available.
STB#	PA0	48	I	**Strobe#** This active low input latches new data into port B during handshake controlled input.
ACK#	PA0	48	I	**Acknowledge#** A low level on this line indicates that the remote device has fetched the output data from port B during handshake controlled output.
D15-D13 D12-D8	PB7-PB5 PB4-PB0	49-51 53-57	I/O	**High Data Bus** Bi-directional, tri-state upper data bus lines for 16-bit bus mode, connected to the system data bus.

Block Diagram



Functional Description

General

The SAB 82556 Universal System Interface Controller (USIC) is a multifunction combo device. It combines system and interface functions necessary for most microprocessor systems like:

- serial interfaces
- parallel interfaces
- timers / counters
- interrupt controller

with a flexible adaptable bus interface. This bus interface can operate in the so called "Intel bus mode" (used e.g. by Siemens, Intel, NS, NEC microprocessors) or in the so called "Motorola bus mode" (used e.g. by Motorola, Zilog microprocessors) in order to minimize the required interface logic.

It is fast enough to allow operation without waitstates in many systems (e.g. 10 MHz SAB 80286 system) or operation with only one waitstate.

The USIC also features a clock generator, baud rate generators, a digital phase locked loop and DMA support.

The USIC's functional blocks are compatible with the corresponding standard devices (SAB82C59A, SAB82C54, etc.) as far as possible. Upgrades and minor changes have been made to integrate the various blocks into one controller.

To reduce the pin count some of the USIC's 68 pins serve for different purposes according to the programmed operating mode (see "Alternate Pin Definitions").

Notation:

The USIC's 16-bit data bus (D15 ... D0) consists of a primary part (used for the low byte of a word) and a secondary part (used for the high byte of a word).This description is used within the following chapters and has different meanings for "Intel bus mode" and "Motorola bus mode", since the USIC supports both byte ordering schemes:

D15 . . . D8	D7 . . . D0	Supported Byte Ordering
Secondary Part	Primary Part	Intel Bus Mode
Primary Part	Secondary Part	Motorola Bus Mode

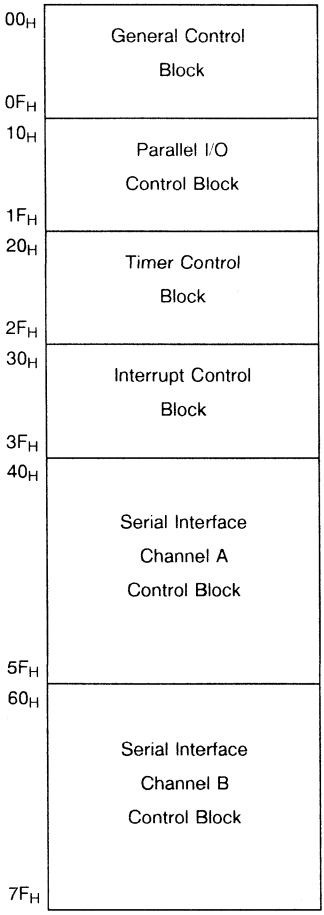
Register Architecture

Nearly all modes and functions of the USIC are controlled via a series of control and status registers. The USIC's address space is divided into several register blocks, where each block controls a specific peripheral function (see figure below).

The register arrangement within a given block conforms with the register arrangement of the corresponding standard device. This simplifies portating existing software to a USIC-based system.

Each register block will be described along with the peripheral function it controls.

Basic USIC Register Architecture



Register Access

The bus interface allows 8-bit access as well as 16-bit access to the USIC registers. However, only a few registers really support 16-bit data transfer (data register, receive interrupt status register 0, receive status register, transmit command register 0 for serial channel B).

Word accesses to the other (8-bit) registers only use the primary part of the data bus and will ignore the secondary part (i.e. discard written data, invalid data during read). Note that these word accesses can only reach even addressed registers!

If bytes are read via the 16-bit data bus, the 8-bit data is provided on both parts of the data bus!

Byte accesses ensure compatibility with standard devices.

Note:
Register locations within the USIC's register area which are marked "reserved" should not be accessed. Read operations will result in invalid data, write operations may cause malfunctions of the USIC.

"Reserved" bits within defined registers should be "0" during write operations and be discarded after read operations. This will provide compatibility with future versions.

The Bus Interface

The USIC provides a flexible bus interface that can be adapted to support various microprocessor buses . It can be programmed to support either the transfer control scheme with RD# and WR# strobe lines (Intel Bus Mode) or the scheme using Data Strobe DS# and a Read/Write control Line R/W# (Motorola Bus Mode). The USIC's bus interface is fast enough to allow operation without waitstates (or 1 waitstate) in most systems. In addition an optional 16-bit transfer capability is provided for accesses to the FIFOs and some registers of the Serial Unit.

16-bit accesses to the FIFOs will read or write two consecutive entries of the FIFOs. If only one FIFO entry is available (read) or empty (write), the transfer is done on the primary part of the (16-bit) data bus and the secondary part is invalid (read) or discarded (write).

The Serial Interface Unit

The USIC's Serial Interface Unit provides two powerful, differently equipped serial channels (A and B). The performance of the two channels is listed in the table below:FIFOs are available on both receivers and transmitters to allow fast and efficient

Feature	Channel A	Channel B
Transmitter FIFO	4 bytes	16 bytes
Receiver FIFO	16 bytes	16 bytes
Data Transfer Modes	Polling, Interrupt	Polling, Interrupt, DMA
Data Transfer Width	8/16 bit	8/16 bit
Coding	NRZ	NRZ, NRZI, FM0, FM1, Manch.
Clock Options	Baudrate Gen., 2 CLK pins	Baudrate Gen., 2 CLK pins, DPLL
Compare Options	Receive Data	Receive Data, 8/16 bit Address (HDLC)
SYN Character (COP)	------	6,8,12,16 bit
Supported Protocols	Asynchronous	Asynchronous, Byte-synchronous, Bit-synchronous (HDLC)

block transfers of data. These FIFOs buffer data to/from the transmit/receive machine. In addition to data also some control information is passed through the FIFOs.

The transmit machine fetches data from the associated FIFO and serializes it to the transmitter output. Additional information can be appended.

The receive machine samples data from the receiver input and stores it to the associated FIFO. The receive machine also performs error checking, character/address matching, collision detection, loopback diagnostics, etc.

The Parallel Interface Unit

The Parallel Interface Unit consists of three 8-bit Input/Output ports. In addition several control inputs (T0IN, T0GATE, T1IN, T1GATE, INTE, TxCB, RxCB, CTSA#, CTSB#) can be used as general purpose inputs, if not needed for their original functions.

Each pin of the different ports can be programmed to be an input or an output or to provide additional control and bus support functions.

The logical state of each pin can be read regardless of the actual function of the pin (input, output or control). The content of the output latch can be read via a separate register. The optional control functions of the port pins are implicitly selected, if the related optional function is enabled. The I/O definition in the port control register is ignored in this case.

If no control functions are needed, the USIC will provide 24 programmable I/O pins and 9 inputs. Of course every mix between I/O and control functions is possible.

The following alternate functions can be realized with the parallel port pins:

Pins	Alternate functions
Port A	16-bit bus control, DMA support, modem control, Port B handshake, interrupt inputs
Port B	Higher data bus D15 . . . D8
Port C	Interrupt control, DMA control, clock signals

The Timer/Counter Unit

The USIC holds three 16-bit timers/counters which are similar to those of the SAB 82C54. Controlled by 5 registers the timers can produce single or repeated output pulses, square waves or strobes from a selection of input clock signals. The following clock inputs can be selected:

Clock Source Signal	Timer 0	Timer 1	Timer 2
System clock CLK	YES	YES	YES
Receiver A character strobe	YES	YES	YES
Receiver B character strobe	YES	YES	YES
Transmitter B character strobe	YES	YES	YES
Timer clock input pin	YES	YES	NO
Baud rate generator 0	YES	YES	NO
Baud rate generator 1	YES	YES	NO
Transmitter A character strobe	YES	YES	NO

Note:
All timer outputs can generate interrupts, timer 0 and 1 outputs are also externally available on pins.

The Interrupt Control Unit

The USIC's interrupt control unit is able to connect up to 11 internal and 9 external interrupt sources to the host processor. Its operation is similar to the operation of the SAB82C59A interrupt controller. For cascaded applications the USIC's interrupt control unit can operate as master or slave together with other SAB82C59As (in Intel bus mode) or it can operate in a Daisy chain together with other interrupt sources (Motorola bus mode).

Each of the interrupt inputs can be assigned to one of eight interrupt levels. Operation in two nested modes is possible as well as software polling.

Operating the SAB 82556

Reset Operation and Mode Selection

To put the various units into a well defined initial state the USIC provides two reset mechanisms:

- **Hardware Reset,**
  performed through activation of the RESET input. Hardware Reset is normally used during power up or system re-initialization.
- **Master Reset Command,**
  performed by setting and then clearing the MRES bit in the general control register (GCR). The Master Reset Command can be used for system warm-boot or to immediately stop operation in case of an emergency (e.g. power fail).

The actions taken upon Hardware Reset and Master Reset Command are identical. Generally speaking, the USIC is put into an inactive state.

The following actions are taken upon Reset:

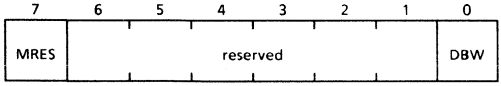
- receivers and transmitters are stopped
- receive and transmit FIFOs are flushed
- interrupt level 7 is assigned lowest priority
- ICU is in master mode and slave mode address is set to 7
- all interrupt source assignments are cleared
- control outputs are forced to inactive state
- control register bits are cleared (except mask bits and MRES)
- source interrupt mask bits are set
- level interrupt mask bits are cleared
- parallel ports are set to input mode

After Reset the USIC can operate in two different bus modes, which are selected via the MODE pin:

- Intel Bus Mode MODE = "0"
- Motorola Bus Mode MODE = "1"

For both modes the data bus width can be 8-bit or 16-bit, selected by bit 0 (DBW) of the GCR.

General Control Register (GCR), offset 00_H:



Data Bus Width 1)
0: 8-bit
1: 16-bit

Master Reset
0: Complete Master Reset Command (if previously begun), otherwise: NOP
1: Begin Master Reset Command

Note 1):
Setting this bit together with "MRES" will have no effect!

Bus Interface Operation

In Intel Bus Mode the USIC provides two strobe signals for read (RD#) and write (WR#) accesses and transfers the low byte of a word on the lower part of the data bus (D7 ... D0).

In Motorola Bus Mode the USIC provides a strobe signal for data access (DS#) and a control signal (R/W#) to distinguish read from write accesses. The low byte of a word is transferred on the upper part of the data bus (D15 ... D8).

16-bit accesses are supported for the FIFO registers, receive interrupt status register 0, receive status register and transmit command register 0 of serial channel B.

FIFO Handling in 16-bit Mode

Reading a word from a FIFO register provides the top of FIFO on the primary part of the data bus and the next entry on the secondary part. If there is only one byte stored in the FIFO, the secondary part will hold an arbitrary value, which is notified by the appropriate status bit and an optional interrupt. Writing a word to a FIFO register will copy the primary part of the data bus to the FIFO's first empty entry and the secondary part to the next entry. If there is only one empty entry, the secondary part is discarded, which is notified by the TxOverrun flag and an optional interrupt.

Register Accesses in 16-bit Mode:

Access Type	Data Transfer Operation (Register ⟷ Data Bus)
Word - Read	Standard byte register to primary part, extension to secondary part 1)
Byte - Read	Byte register to primary and secondary part
Word - Write	Primary part to standard byte register, secondary part to extension 2)
Byte - Write	Active part (A0, BHE#/LDE#) to byte register

Notes:

1) Registers without extension will return invalid data on the secondary part!

2) Secondary part will be discarded, if there is no extension. In this case the following byte register is not affected by the write operation!

DMA Transfers

The USIC's serial channel B is equipped to support communication with a DMA controller.

A request signal can be generated

- for blocks, i.e. requests stay active as long as the receive FIFO holds characters or the transmit FIFO is not full.
- for characters, i.e. requests are deactivated after each transfer.

A request can be serviced by two different accesses:

- regular transfers using CS# and read/write control
  (allows access to all registers like with processor cycles)
- DMA transfers using DACK# and read/write control
  (allows access to channel B's receive/transmit FIFO)

It thus can be used together with a variety of DMA controllers. Additionally the USIC supports single cycle DMA transfers where data is moved from source to destination with one single bus cycle. For this feature the meaning of the read/write control lines can be changed while DACK# is active (i.e. RD# and WR# are exchanged, or R/W# is inverted). This eliminates several gates of the external control logic.

Fast DMA controllers (e.g. SAB 82258A) are supported by a "look-ahead" control which deactivates the DMA request at the end of the last but one transfer. This prevents a FIFO over/underrun during pipelined transfers with continuous DACK#.

Serial Interface Operation

The USIC supports 3 major groups of serial protocols (asynchronous, character-oriented, bit-oriented) with a number of variations within each group. The following sections describe several features common to all protocols and the supported protocols themselves.

Status Information to the Host

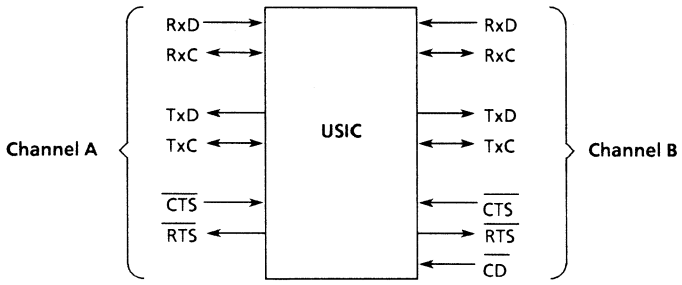
The USIC provides extensive status information for the host CPU. This information can be read from various status registers either by means of polling or initiated through interrupts. A new status is always indicated by setting/clearing the respective status bits. If the corresponding interrupt is enabled, also an interrupt signal is sent to the host CPU.

In the following chapter the action upon a new status (i.e. modifying status bits and sending interrupts, if enabled) is called a **"condition"**. Please note that a "condition" does not necessarily send an interrupt.

Serial Interface Signals

In addition to the data and clock lines the USIC provides 2 or 3 interface lines to control the serial channels (see figure).

Serial Interface Lines



The control lines can be programmed to serve various purposes:

- Clear To Send input (CTS#), selected via "Automatic Transmit Control" bits and "Collision Detect" bit
  - CPU controlled input
    The signal level and transitions (indicated by a condition) can be evaluated by the host CPU.
  - Strobe signal to define time slots in Auto Mode 0
    Transmission is executed only during time slots which are identified by CTS# being active. The CTS# pulse must be synchronized to the transmit clock (external clocking required). A character, block or frame can be distributed over multiple time slots. Correct operation is provided with NRZ/NRZI coding.
  - Transmission Enable signal in Auto Mode 1
    If CTS# is active, data or timefill bit pattern is transmitted. If CTS# gets inactive, transmission stops after the current character, block or frame is completely sent. The TxD output is forced high. A single CTS# pulse can trigger transmission of one data unit (character, block, frame).
  - Transmission enable signal in Auto Mode 2
    If CTS# is active, data or timefill bit pattern is transmitted. If CTS# gets inactive, transmission aborts immediately. The TxD output is forced high. The transmit machine is cleared and the "TxEnable" bit is reset. The TxFIFO should be flushed to prevent transmission of the residues of the aborted data unit.
  - Collision Detection Input
    To allow collision detection the TxD output is fed back to the CTS# input. If the two signals are different (sampled with the falling edge of the transmit clock), this is indicated by the "Collision" condition. Proper operation is provided with NRZ and NRZI coding. Collision detection can be combined with Auto Modes 1 and 2, where the collision detect output replaces the original CTS# input.

  Note:
  CTS# does not affect the Auto Modes, when the XOn/XOff protocol is active.

- Request To Send output (RTS#), selected via "RTS# Select" bits
  - Software controlled RTS#
    The RTS# output level is controlled via the "RTS# Control" bit by the host software.
  - Transmitter controlled RTS#
    The RTS# output is active, while data is transmitted (including start/stop bits, SYN characters and opening/closing Flags). It is inactive during idle times. This output signal can be used to enable external line drivers.
  - Receiver controlled RTS#
    The RTS# output is active, while the receiver is enabled and the RxFIFO holds 12 or less characters. It is inactive, while the receiver is disabled or when the RxFIFO holds more than 12 characters. This output signal can be used to control the remote transmitter.

    Note: This feature applies to ASYNC mode.

- Carrier Detect input (CD#), selected via "CD# Select" bit, and "Automatic Receive Control" bits
  - CPU controlled input
    The signal level and transitions (indicated by a condition) can be evaluated by the host CPU.
  - Strobe signal to define time slots in Auto Mode 0
    Reception is enabled only during time slots which are identified by CD# being active. A character, block or frame can be distributed over multiple time slots. Correct operation is provided with NRZ/NRZI coding.
  - Reception Enable signal in Auto Mode 1.
    If CD# is active, the receiver is sampling. If CD# gets inactive, reception stops after the current character, block or frame is completely received. A single CD# pulse can trigger reception of one data unit (character, block, frame).
    Note:
    In COP mode the receiver cannot determine the end of a block. Reception therefore must be stopped by an "Enter Hunt Phase" command.
  - Reception Enable signal in Auto Mode 2

    If CD# is active, the receiver is sampling. If CD# gets inactive, reception stops immediately and the currently received character is lost.

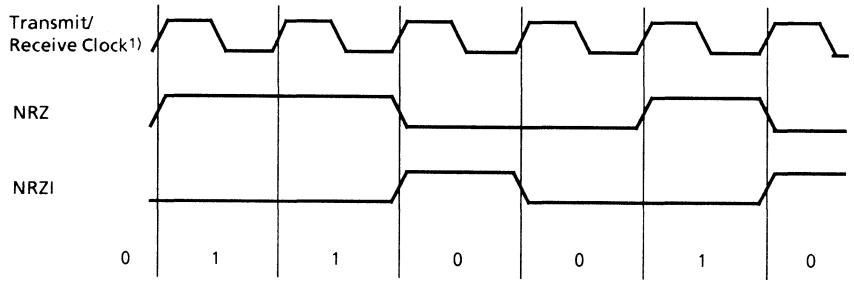
Data Encoding

Serial channel B supports five different data encoding modes (see below). On channel A data is always encoded with NRZ.

The following data encoding modes are provided:

- NRZ (Non-Return-to-Zero)
  The signal level during each bit cell represents the corresponding data bit.
- NRZI (Non-Return-to-Zero-Inverted)
  For a "0" bit the signal level changes at the beginning of the corresponding bit cell. For a "1" bit the signal level remains the same.

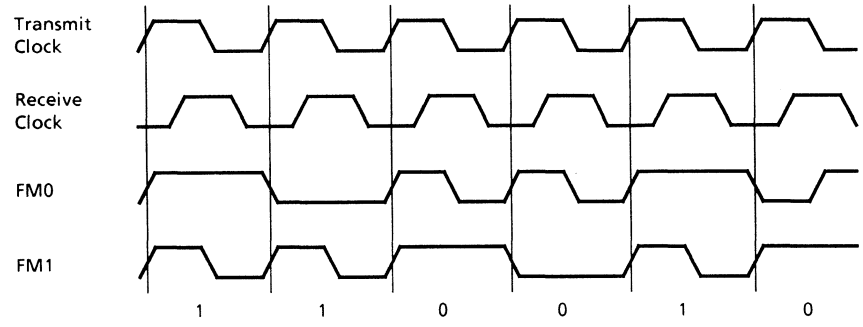
NRZ and NRZI Data Encoding



1) Transmitter uses rising edge, receiver uses falling edge

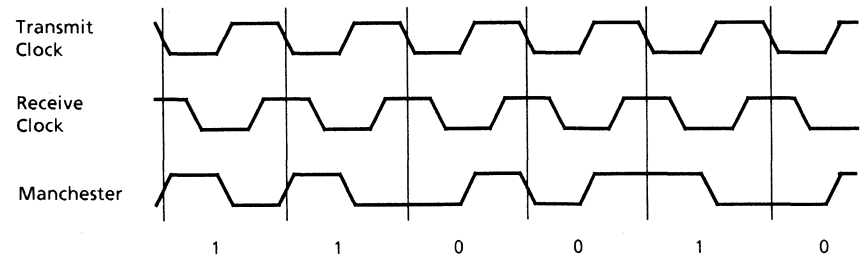
- FM0 (Also known as Bi-Phase-Space)
  The signal level changes at the beginning of each bit cell. For a "0" bit it also changes in the middle of the corresponding bit cell.
- FM1 (Also known as Bi-Phase-Mark)
  The signal level changes at the beginning of each bit cell. For a "1" bit it also changes in the middle of the corresponding bit cell.

FM0 and FM1 Coding



- Manchester (Also known as Bi-Phase)
  The signal level changes at the beginning and in the middle of each bit cell. The level during the first half of the bit cell represents the corresponding data bit, the level during the second half represents the inverted data bit. The receiver evaluates the signal level during the first half of the bit cell with the falling edge of the receive clock.

Manchester Coding



Clocking Options

The serial interface unit of the USIC uses and provides a number of clock signals. The Clocking Register (CR) and the Baudrate Count Registers (BCR) control these functions.

Note:
The shaded options and modes are not available on serial channel A. Also the respective register sections are reserved.

Possible clock sources:

Source	Ch. A Rec.	Ch. A Transm.	Ch. B Rec.	Ch. B Transm.
Baud rate Generator [1]	✓	✓	✓	✓
External clock TxC [1]	✓	✓	✓	✓
External clock RxC [1]	✓	—	✓	—
DPLL [2]	—	—	✓	✓
Oscillator	—	—	—	✓

[1] Separate for both channels
[2] Can be fed from oscillator or from baud rate generator

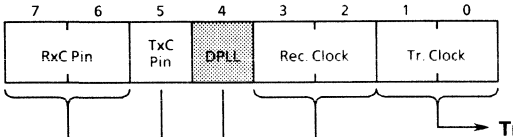
Possible clock outputs:

Clock Signal	RxC (A)	TxC (A)	RxC (B)	TxC (B)
Baudrate Generator [1]	✓	—	✓	—
DPLL	—	—	✓	—
Oscillator	—	✓	—	✓

[1] Separate for both channels

Note:
The receive and transmit clock pins can be used as general purpose input/output (channel A) or input (channel B), if their specific function is not selected.

Clocking Register (CR), offset $44/64_H$ (channel A/B):



Transmit Clock
(Selects the clock source for the transmitter)
00 Baudrate Generator
01 TxC Pin
10 DPLL
11 Oscillator for COP/HDLC only
reserved for ASYNC

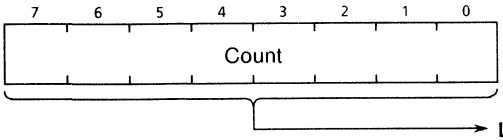
Receive Clock
(Selects the clock source for the receiver)
00 Baudrate Generator
01 RxC Pin
10 TxC Pin
11 DPLL

DPLL
(Selects the ref. clock for the DPLL circuit)
0 Baudrate Generator
1 Oscillator

TxC Pin (Defines the output on this pin)
0 no Output
1 Output Oscillator Clock

RxC Pin (Defines the output on this pin)
00 no Output
01 Output Baudrate Generator Clock
10 reserved
11 Output DPLL Clock

Baudrate Count Register Low, High (BCRL,H), offsets $42/62_H$, $43/63_H$ (channel A/B):



Low Byte / High Byte
of the 16-bit baudrate count for dividing the oscillator frequency

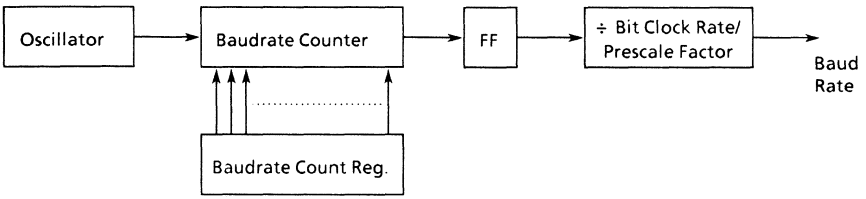
The resulting data rate is:

$$\text{Data Rate} = \frac{\text{Oscillator Frequency}}{\text{Baudrate Count} * 2^{*}}$$

where XX = Bit Clock Rate for ASYNC mode.
XX = Prescale Factor for COP/HDLC

Both baudrate generators are fed from the on-chip oscillator. A flipflop produces a symmetrical square wave signal.

Baudrate Generation:



Notes:

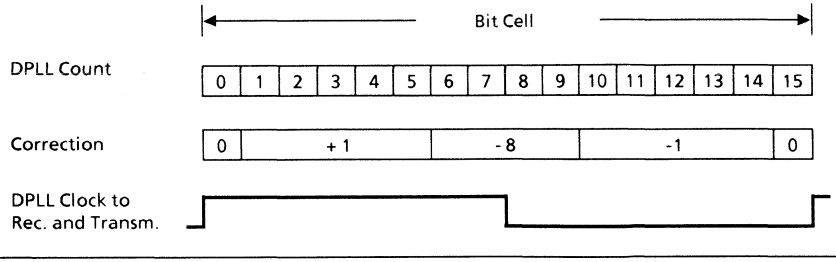
- The BCRL must be loaded first, baudrate generation is disabled between loading BCRL and loading BCRH.
- Baudrate generation can be disabled by only loading the BCRL (not BCRH).

The Digital Phase Locked Loop

The Digital Phase Locked Loop can be used for clock recovery on channel B's receiver, when no external clock is available. The baudrate generator or the oscillator can be selected as reference clock input (16 times the data rate). The DPLL is implemented with a 16-bit counter, which is modified (or not) on transitions of the data signal. For correction the DPLL count 0 is doubled (+ 1), or count 4 is skipped (-1), or counts 4 to 11 are skipped (-8; see figures). The exact operation of the DPLL differs with the selected data encoding mode (see figures).

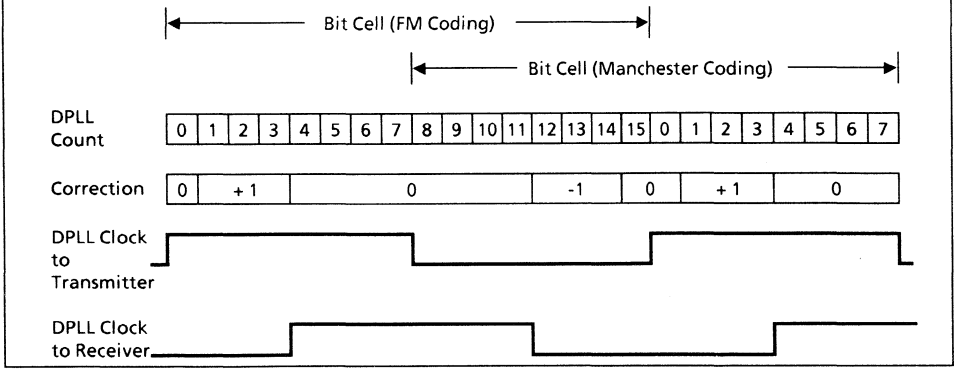
For NRZ/NRZI coding the DPLL only corrects, if only one transition occurs during the count interval. This filters out spikes and glitches.

DPLL Algorithm for NRZ and NRZI Coding



For FM0/FM1/Manchester coding the data edges are excluded from clock recovery, since they are not regular. Finding no transition within the band from count 12 to 3 for two consecutive cycles disables reception and transmission (if clocked from the DPLL) and resets the DPLL count to 0 (FM0/FM1 coding) or 8 (Manchester coding). This is indicated by the "DPLL Unsynchronized" condition.

DPLL Algorithm for FM and Manchester Coding

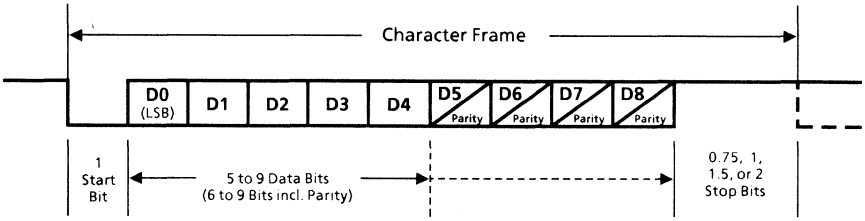


Asynchronous protocol

Asynchronous protocols transfer characters which are preceeded by a start bit and followed by a stop bit with a length of 0.75, 1, 1.5 or 2 bit cells. The characters themselves may consist of 5 to 8 bits plus a multi-purpose bit. This additional bit may serve as 9th data bit, parity bit or as address/data control (A/D) bit in the so called µLAN mode (also known as "Multi Drop Mode"). This mode enables the USIC to ignore data characters (with the A/D-bit cleared) from the incoming data stream, but recognize address characters (with the A/D-bit set).

Small networks can easily be built using this feature.

Asynchronous Character Frame



Data reception can be truly asynchronous, where the receiver scans the data line at a clock rate of 16, 32 or 64 times the data rate, or it can be "isochronous", where the scan clock rate equals the data rate. Isochronous mode requires an external clock signal, but provides higher data rates. On serial channel B this clock signal can also be generated by the internal Digital Phase Locked Loop (DPLL).

The USIC can recognize parity errors and framing errors (i.e. stop bit = "0") and generate appropriate interrupts. A Break Condition (character and stop bit are "0") can also cause an interrupt, as can a receive FIFO overflow. A received character in this case will be lost.

Received characters can be compared with a given pattern through a mask. Match or mismatch can be used to lock or unlock the receive FIFO, i.e. prevent parts of the data stream from being received.

The USIC's transmitter can be controlled by a remote station with the XOn/XOff protocol. Reception of an XOn control character (specified in Compare Register 0) starts the transmitter, reception of an XOff control character (specified in CR1) stops it. Selecting the XOn/XOff protocol switches the transmitter to Auto Mode 1, disregarding the programming in the "Automatic Transmit Control" field. The XOn/XOff protocol machine's status can be read from the "XOn/XOff Status" bit.

Character Oriented Protocol

Character oriented protocols (COP) transfer blocks of characters (5 to 8 bits), which are preceeded by SYN characters. The data blocks are often enclosed within a header and a frame check sequence (FCS). The USIC allows user definable SYN characters (6,8,12,16 bits) and provides a Cyclic Redundancy Check (CRC) generator/checker that features two selectable generation polynomials and two selectable preset values. Additionally parity generation/checking is available.

Characters can be included in or excluded from CRC generation through the "CRC On/Off" bit, leading SYN characters and Interblock-Time-Fill (ITF) are never part of the CRC. Interblock-Time-Fill (ITF) is the bit pattern which is sent by an active transmitter, when no data is available. It can be programmed to be SYN characters or logical "1"s.

Transmission of the CRC pattern is triggered by setting the "CRC Append" bit. Afterwards more data is sent (TxFIFO not empty) or ITF (TxFIFO empty). Transmission of the last character (before ITF) is indicated by the "All Sent" condition. From this condition (or interrupt) the CPU learns that a block has been completely transmitted.

After enabling, the receiver searches for a SYN character to synchronize (Hunt phase). Afterwards (SYNC phase) received characters are pushed into the RxFIFO (right justified).

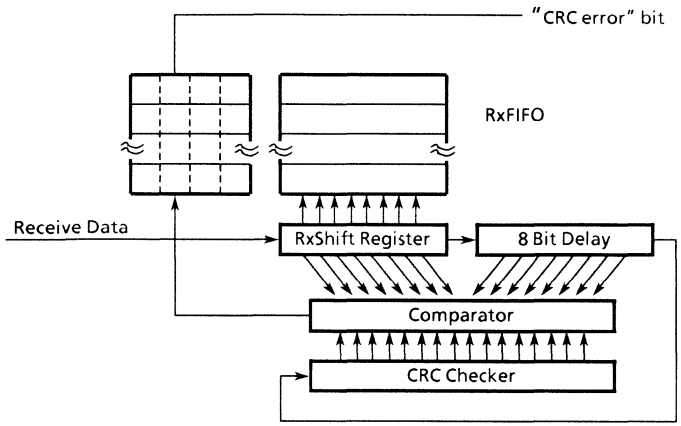
The "SYN character load inhibit" bit enables/prevents SYN characters from being pushed into the RxFIFO.

The begin of the Hunt phase or SYNC phase is indicated by the "Hunt phase" condition or "SYNC phase" condition. The reception of the first character of a block is indicated by the "Start of block" condition (this is not a data read request).

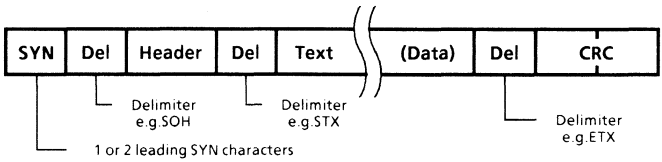
The host CPU is responsible for data interpretation as well as for CRC management. This includes selecting characters for CRC calculation ("CRC On/Off" bit), initializing the CRC checker for the next block ("Reset CRC checker" bit) and controlling the proper reception of blocks and subblocks. The latter involves recognizing (sub)block delimiters (ETB, ETX, etc.), evaluating CRC results ("CRC error" bit) and ensuring that the complete CRC sequence (16 bits) is received. This may require to temporarily switch the character length to 8 bits ("Receive CRC" bit) for the two CRC characters (is restored automatically).

After reception of a block the "Enter Hunt Phase" command makes the USIC wait for the start of a new block again, and hereby prevents the ITF patterns from being pushed into the RxFIFO.

CRC Logic



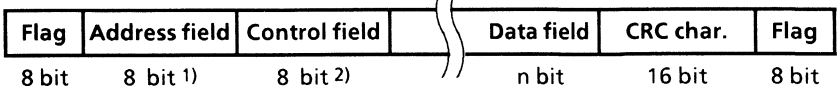
COP Block (example)



HDLC Protocol

High Level Data Link Control (HDLC) protocols transfer data frames of arbitrary size which are enclosed in flags together with additional fields (see figure). The Cyclic Redundancy Check (CRC) is performed on the complete frame except the flags.

HDLC Frame Format



1) Extendable to 2 or more Bytes
2) Extendable to 2 Bytes

Full transparency of the frame fields is guaranteed by means of the bit stuffing mechanism. The transmitter hereby inserts a "0" bit after each 5 consecutive "1" bits. The receiver eliminates these additional "0" bits to restore the original data.

This allows to transfer data without "reserved characters" and at the same time provides dedicated bit patterns to run the protocol.

Six "1" bits enclosed in two "0" bits form the Flag pattern. The Abort Sequence is made up of eight consecutive "1" bits. It allows to immediately abort the transmission of a frame, e.g. in case of an error.

15 or more consecutive "1" bits identify the Idle Sequence which is sent, when there is no data available.

The USIC can be programmed to start transmission of a frame with 1, 2, 4 or 8 Flags to accomodate the respective receiver. Between two frames continuous Flags or continuous logical "1" bits can be sent (Interframe Time Fill, ITF).In case of a frame abort (no data available or abort command) the USIC can send the specified abort sequence or immediately switch to ITF. This is indicated by the "Frame Aborted" condition.

The character length in HDLC mode is fixed to 8 bits. Nevertheless the USIC also handles HDLC protocols with data field lengths other than multiples of 8 bits. A part of the last byte can be excluded from transmission ("Residual Code" bits) which results in an arbitrary data field size. The USIC's receiver can detect and indicate residual bits during reception.

Received frames can also be classified by an 8-bit or 16-bit address field. The address field is compared with the contents of Compare Register 0 and 1. On a match the frame is accepted, on a mismatch it is discarded.

The end of the current frame is marked with the "End of Frame" condition, which can be generated with the "End of Frame" command or the EODT# input. This condition is stored in the TxFIFO along with the frame's last character. Afterwards the next frame can be loaded immediately ("Send Frame" command).

If enough data is present in time, the USIC can feature back-to-back framing, i.e. sending successive frames with only two (or more) Flags between them.

Transmission of a complete frame (including closing flag) is indicated by the "All Sent" condition.

After enabling, the receiver searches for a Flag to synchronize (Hunt phase). Afterwards (SYNC phase) received frames are pushed into the RxFIFO. The begin of the Hunt phase, of the SYNC phase and of data reception is indicated by the "Hunt phase", "SYNC phase" or "Start of Frame" condition.

The "End of Frame" indication is stored in the FIFO along with the last byte of a frame. The next frame can be pushed into the FIFO immediately afterwards. Therefore the USIC can also handle back-to-back frames which are separated by only one Flag.

The USIC supports end of frame handling (buffer management) by an intelligent DMA controller. The EODR# line is activated when the last byte of a frame is removed from the RxFIFO. This tells the DMA controller to check the status and/or switch to the next free buffer for reception of the next frame.

The USIC provides additional support for the host CPU:

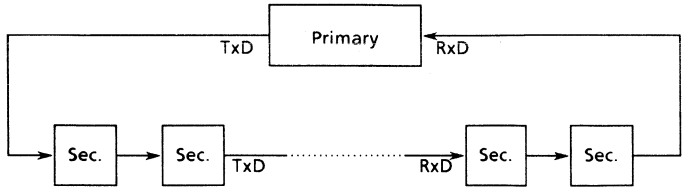
- CRC character transfer — to the RxFIFO can be enabled (transparent mode) or disabled (CRC is checked only)
- Abort condition — is indicated when the last byte of an aborted frame is removed from the RxFIFO
- CRC error condition — is indicated (along with the last byte read), when the received CRC character does not correspond with the received frame
- Residual Length indication — tells the host CPU that the last byte is not complete. The valid residual bits can be recovered by software.

SDLC Loop Support

The USIC can support a variation of the HDLC protocol: the SDLC loop.

An SDLC loop connects one primary station and several secondary stations by a physical ring (see figure). The logical connection is point (master) to multi-point (secondaries). The secondary stations are enabled for transmitting by the primary station (information request).

SDLC Loop Configuration

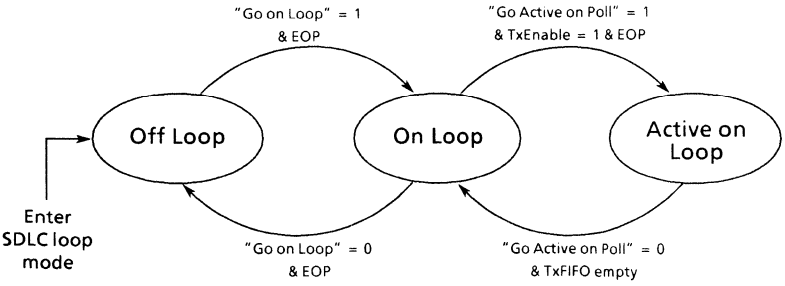


The USIC's SDLC loop mode directly supports secondary stations with the following differences compared to HDLC mode:

- Data can be encoded with NRZ and NRZI only
- Interframe-Time-Fill (ITF) only sends Flags
- EOP sequence (End of Poll) is defined as one "0" bit followed by seven "1" bits in a row
- Abort definition is changed to continuous Flags (ITF) without preceding CRC character (the original definition of eight "1" bits is used for EOP!).

Two control bits ("Go on loop" and "Go active on Poll") allow a secondary station to switch between its 3 possible operation states (see figure). Entering each state is indicated by an appropriate condition, so the host CPU knows the actual state.

SDLC Loop Secondary Station State Diagram



In the "Off Loop" state the RxD input is directly connected (gate delay) to the TxD output, data reception is disabled. In the "On Loop" state the RxD input data is output on TxD with 1 bit delay, data reception is enabled.

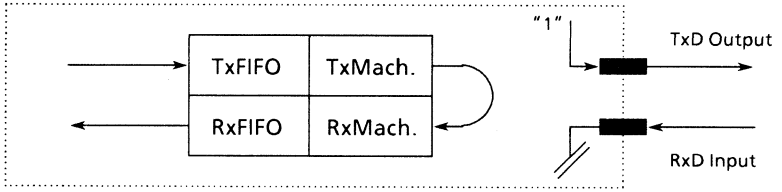
Transitions between these two states are realized by doubling or erasing the seventh "1" bit of an EOP sequence. In the "Active On Loop" state the RxD input is disconnected from the TxD output. Data reception is disabled and data transmission is enabled. The "Active On Loop" state is entered by changing the seventh "1" bit of an EOP sequence to "0", which produces a Flag instead of EOP. This state is left only, if all data are completely transmitted.

Loopback Diagnostics

To ease the evaluation and debugging of serial communication systems the USIC provides two diagnostic functions. They allow to test the USIC's operation as well as the system's operation.

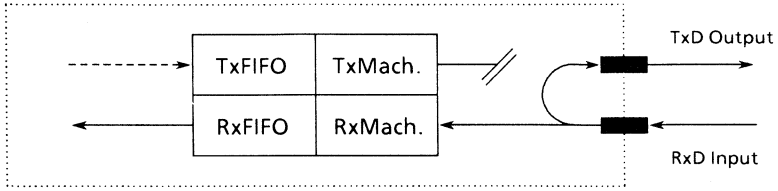
- Local Loopback Mode
  In this mode the TxD output is held high ("1"), the RxD input is disconnected. The output of the transmit machine is directly connected to the input of the receive machine. Transmitted data is directly reflected to the receiver (see figure).

Local Loopback Mode



- Remote Loopback Mode
  In this mode the RxD input is directly connected to the TxD output. Data reception is possible, the transmit machine is disconnected (see figure).

Remote Loopback Mode



Registers controlling the serial channels

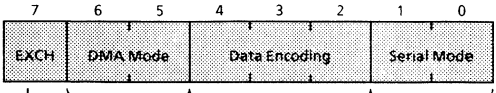
The following section specifies the control blocks for the serial interface unit. The registers are described in the order they appear within the control blocks.

Registers of the control block for serial channel A occupy the internal addresses from 40_H to $5F_H$, registers of the control block for serial channel B occupy the internal addresses from 60_H to $7F_H$.

The control blocks for channels A and B are described in parallel.

Note:
The shaded options and modes are not available on serial channel A.
Also the respective registers and register sections are reserved.
This shall help to easily determine, which features are provided on which channel.

Operation Mode Register 0 (OMR0), offset 65_H:



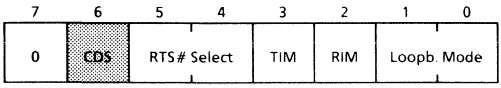
Serial Mode
0 0 Asynchronous
0 1 COP (Character Oriented Protocol)
1 0 HDLC (High Level Data Link Control)
1 1 SDLC Loop

Data Encoding
0 0 0 NRZ
0 0 1 NRZI
0 1 0 FM0
0 1 1 FM1
1 0 0 Manchester
1 0 1 reserved
1 1 X reserved

DMA Mode
0 0 No DMA (control by polling or interrupt)
0 1 Edge Triggered DMA
A single DRQ pulse is generated for each character to be transferred
1 0 Level Triggered DMA, DRQ remains active as long as data is to be transferred. This allows burst transfers.
1 1 reserved

RD#/WR# Exchange
0 RD# and WR# (or R/W#) operate as defined.
1 RD# and WR# lines are exchanged (R/W# is inverted) while DACK# is active. This allows single cycle DMA transfers without additional hardware.

Operation Mode Register 1 (OMR1) offset $46/66_H$ (channel A/B):



Loopback Mode
0 0 Normal Operation (no loopback)
0 1 Local Loopback Mode (see description)
1 0 Remote Loopback Mode (see description)
1 1 reserved

RxFIFO Interrupt Mask / EODR# 1)
0 RxFIFO interrupt is enabled
1 RxFIFO interrupt is masked

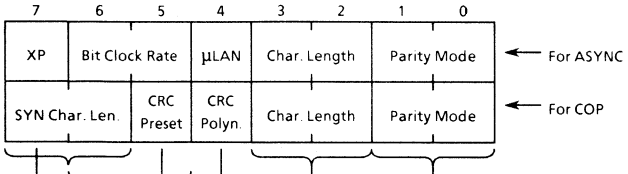
TxFIFO Interrupt Mask / EODT# 1)
0 TxFIFO interrupt is enabled
1 TxFIFO interrupt is masked

RTS#Select (see description)
0 0 No RTS# function selected
0 1 Software controlled RTS#
1 0 Transmitter controlled RTS#
1 1 Receiver controlled RTS# (ASYNC only!)

CD# Select (see description)
0 No CD# function selected
1 CD# line can be evaluated by software or be used for Automatic Receive Control

Note 1):
If any DMA mode is selected, this bit enables the EODT# or EODR# function, respectively. During any DMA mode the TxFIFO and RxFIFO interrupts are always masked.

Operation Mode Register 2 (OMR2), offset 47/67$_H$ (channel A/B):



Parity Mode
0 0 No parity
0 1 Odd parity
1 0 Even parity
1 1 Software parity (ASYNC only!)

Character Length
0 0 8 bits
0 1 7 bits
1 0 6 bits
1 1 5 bits

µLAN Mode ← ASYNC
0 Normal mode, defined parameters are used
1 µLAN mode active, selected character length and parity mode is ignored.

CRC Polynomial Select ← COP
0 CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
1 CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)

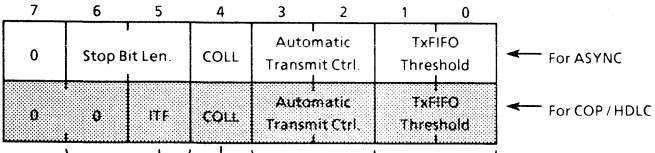
CRC Preset Value ← COP
All bits of the CRC gen., are preset with this value

Bit Clock Rate ← ASYNC
The serial clock frequency divided by the specified factor gives the data rate.
0 0 Use clock directly (factor 1)
0 1 Divide by 16
1 0 Divide by 32
1 1 Divide by 64

SYN Character Length ← COP
0 0 8 bits (CR0:D7 ... D0)
0 1 6 bits (CR0:D5 ... D0)
1 0 16 bits (CR0.D7... D0, CR1:D7...D0)
1 1 12 bits (CR0.D7... D0, CR1:D3...D0

XOn/XOff Protocol ←ASYNC
0 The XOn/XOff protocol is inactive
1 The XOn/XOff protocol is active, the transmitter can be controlled by a remote station

Transmit Mode Register 0 (TMR0), offset 48/68$_H$ (channel A/B):



TxFIFO Threshold
Data requests are generated, if the TxFIFO contents are equal or below the selected threshold.
0 0 0 Characters
0 1 4 Characters (1 on channel A)
1 0 8 Characters (2 on channel A)
1 1 15 Characters (3 on channel A)
Note: 14 characters with 16-bit data mode

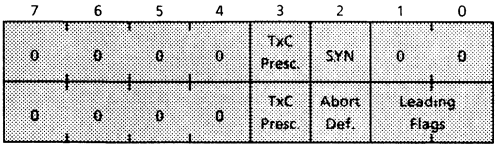
Automatic Transmit Control (see control line description)
0 0 Non-Auto Mode (CPU control)
0 1 Auto Mode 0 (Strobe mode)
1 0 Auto Mode 1
1 1 Auto Mode 2
Note:
If the XOn/XOff protocol is selected (ASYNC), the transmitter is switched to Auto Mode 1 and this field is disregarded.

Collision Detect
0 CTS# is used for transmit control or general input
1 CTS# is used for the collision detect function

Interbl./-frame Time Fill (ITF) ←COP/HLDC
0 Send SYN characters (COP) or Flags (HDLC)
1 Send logical "1" bits

Stop Bit Length ←ASYNC
0 0 1 bit cell
0 1 1.5 bit cells
1 0 2 bit cells
1 1 0.75 bit cells

Transmit Mode Register 1 (TMR1) offset 69_H:



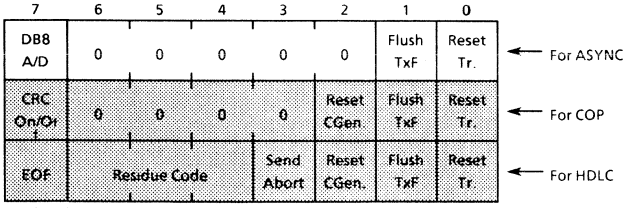
Leading Flags ←HDLC
0 0 1 Flag
0 1 2 Flags
1 0 4 Flags
1 1 8 Flags

Leading SYN Characters ←COP
0 One SYN character
1 Two SYN characters

Abort Definition ←HDLC
0 Abort Sequence is sent (eight "1" bits), after that Interframe-Time-Fill
1 Interframe-Time-Fill is sent immed.

TxClock Prescale
0 No prescaling
1 Divide transmitter clock by 16

Transmit Command Register 0 (TCR0), offset 4A/6A$_H$ (channel A/B):



Reset Transmitter
0 No operation
1 Clear TxFIFO and TxShift Register, drive TxD high, reset associated bits of TCR1 and TISR

Flush TxFIFO
0 No operation
1 Clear TxFIFO

Reset CRC Generator ←COP/HDLC
0 No operation
1 Load CRC generator bits with the selected value ("1" bits for HDLC)

Send Abort ←HDLC
0 No operation
1 Immediately send the defined abort sequence, clear TxFIFO and TxShift Register

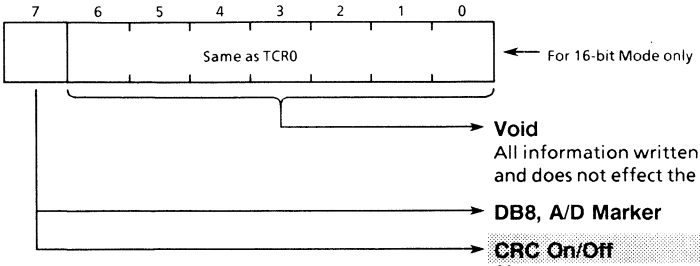
Residue Code ←HDLC
nnn There are nnn bits to send (nnn = 000 means 8 bits)

DB8, A/D Marker ←ASYNC
This bit holds the 8th data bit, the software parity bit or the A/D marker bit (uLAN mode)

CRC On/Off ←COP
0 Exclude following characters from CRC generation
1 Include following characters in CRC generation

End of Frame ←HDLC
0 No operation
1 Mark the end of the current frame

TCR0 16-bit Extension (TCR0X), offset $4B/6B_H$ (channel A/B):



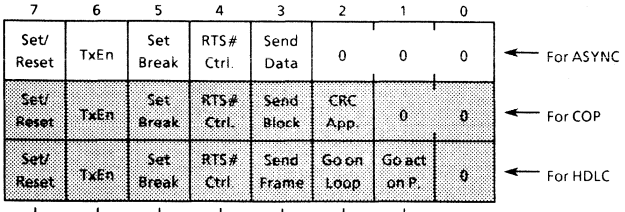
Void
All information written to this area is discarded and does not effect the USIC's operation

DB8, A/D Marker ←ASYNC

CRC On/Off ←COP

Note:
This bit of the TCR0X corresponds to the character transferred on the secondary part of the data bus.

Transmit Command Register 1 (TCR1), offset 4C/6C$_H$ (channel A/B):



Go Active on Poll ←SDLC
0 Enter the "On Loop" state after sending the current data
1 Enter the "Active on Loop" state after reception of an EOP sequence

CRC Append ←COP
0 Send ITF on Tx underrun
1 Send CRC character on Tx underrun

Go on Loop ←SDLC
0 Enter the "Off Loop" state after reception of an EOP sequence
1 Enter the "On Loop" state after reception of an EOP sequence

Send Data / Block / Frame
0 Do not generate data requests for the TxFIFO
1 Request Transmit data, if the contents of the TxFIFO is equal or below the defined threshold

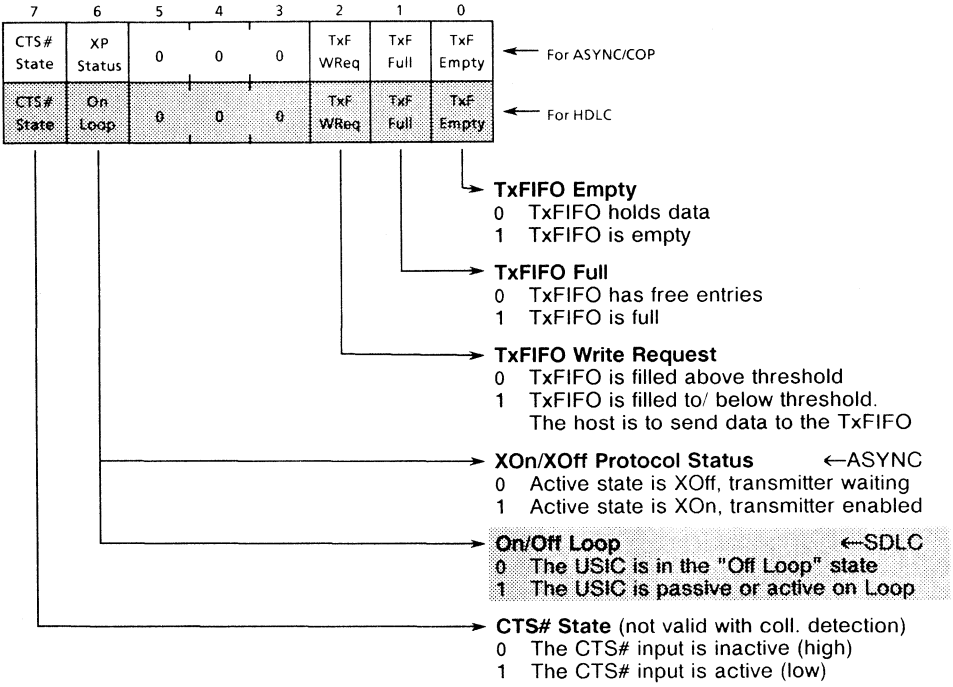
RTS# Control (Software controlled RTS#)
0 RTS# output inactive (high)
1 RTS# output active (low)

Set Break
0 Resume sending data or ITF
1 Stop sending data, clear TxShift Register, force TxD low

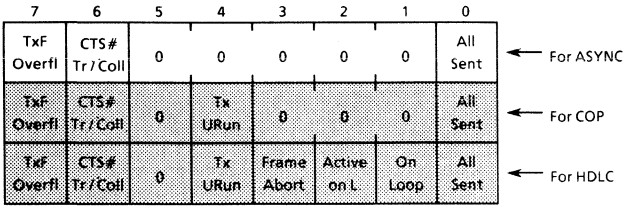
Tx Enable
0 Transmitter disabled (TxD high)
1 Transmitter enabled

Set / Reset
0 Reset the marked command bits ("1")
1 Set the marked command bits ("1")

Transmit Status Register (TSR), offset 4E/6E$_H$ (channel A/B):



Transmit Interrupt Status Register (TISR), offset 4F/6F$_H$ (channel A/B):



All Sent
0 Transmitter is busy sending
1 The last character of the current data unit is completely shifted out

On Loop ←SDLC
0 -
1 The USIC has entered the "On Loop" state

Active On Loop ←SDLC
0 -
1 The USIC has entered the "Active On Poll" state

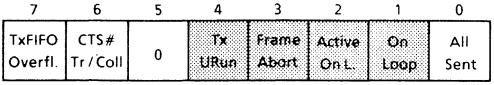
Frame Aborted ←HDLC
0 Frame is sent properly
1 Frame has been aborted

Tx Underrun ←COP/HDLC
0 The transmitter is busy sending
1 TxFIFO and TxShift Register are empty

CTS# Transition / Collision
0 No transition on CTS# input found or no collision detected
1 CTS# input has changed or collision was detected

TxFIFO Overflow
0 The last character was loaded properly
1 TxFIFO full, the last character is lost

Transmit Interrupt Mask Register (TIMR), offset 4D/6D$_H$ (channel A/B):

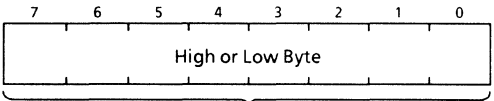


Respective Mask Bit

0 The respective condition also generates an interrupt

1 The respective condition is indicated in the TISR, but no interrupt is generated

Compare Register 0, 1 (CR0,1), offset 50,51$_H$ / 70,71$_H$ (channel A/B):



Compare Value ←ASYNC

Each register holds a compare value for character/address recognition [1].
A match with one of the values may unlock (or lock in µLAN mode) the RxFIFO.

SYN Character ←COP

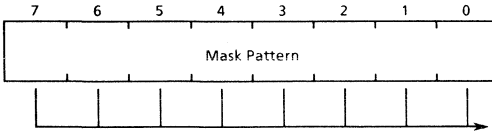
The concatenation CR1&CR0 defines the bit pattern for the SYN characters. For SYN characters shorter than 16 bits the highest bits (respectively) are ignored.

Address Value ←HDLC

An address is defined by one of the registers CR0 or CR1 (8-bit address) or by the concatenation CR1&CR0 (16-bit address) [1]

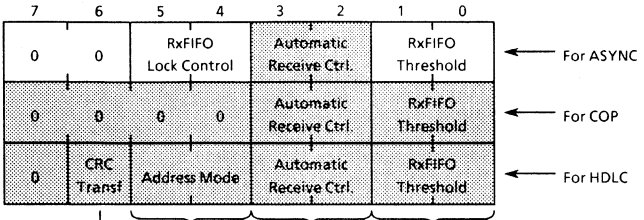
Note [1]: The bits of CR1 can be masked (CMR), which allows to define certain groups of matching characters /addresses.

Compare Mask Register (CMR), offset $52/72_H$ (channel A/B):



Mask Pattern
(Defines a compare mask for CR1)
0 The corresponding bit pos. is checked.
1 The corresponding bit pos. is ignored.

Receive Mode Register (RMR), offset 53/73$_H$ (channel A/B):



RxFIFO Threshold
0 0 1 character
0 1 4 characters
1 0 8 characters
1 1 16 characters

Automatic Receive Control
(Refer to Carrier Detect input description)
0 0 Non Auto Mode
0 1 Auto Mode 0 (Strobe Mode)
1 0 Auto Mode 1
1 1 Auto Mode 2

RxFIFO Lock Control ←ASYNC

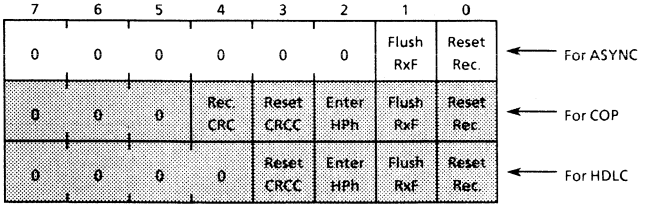
Non µLAN Mode:
0 0 No Automatic Unlock
0 1 Unlock on character match
1 X reserved

µLAN Mode:
0 0 No Automatic Unlock
0 1 Unlock on address character recognition
1 0 Unlock on address character match
1 1 Unlock on address character match and lock on address character mismatch

Address Mode ←HDLC
0 0 No address match, all frames accepted
0 1 8-bit address match
1 0 16-bit address match
1 1 reserved

CRC Transfer ←HDLC
0 Discard the CRC character of received frame
1 Transfer CRC character of received frame to RxFIFO

Receive Command Register 0 (RCR0), offset $54/74_H$ (channel A/B):



Reset Receiver
0 No operation
1 RxShift register and RxFIFO are cleared, associated bits in RCR1, RISR0 and RISR1 are reset.

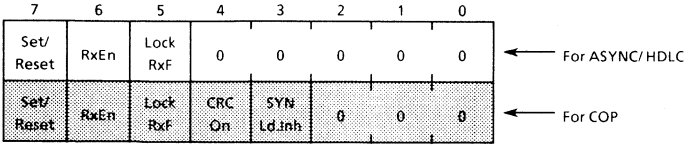
Flush RxFIFO
0 No operation
1 The RxFIFO is cleared, all data is lost

Enter Hunt Phase ←COP/HDLC
0 No operation
1 Receiver enters the Hunt Phase, synchronization is lost.

Reset CRC Checker ←COP/HDLC
0 No operation
1 All bits of the CRC checker are loaded with the selected value ("1" for HDLC)

Receive CRC ←COP
0 No operation
1 The character length is temporarily switched to 8 bits for the next two characters to be received.

Receive Command Register 1 (RCR1), offset 55/75$_H$ (channel A/B):



SYN Character Load Inhibit ←COP
0 SYN characters are treated like normal characters
1 SYN characters are not transferred to the RxFIFO and are excluded from CRC generation.

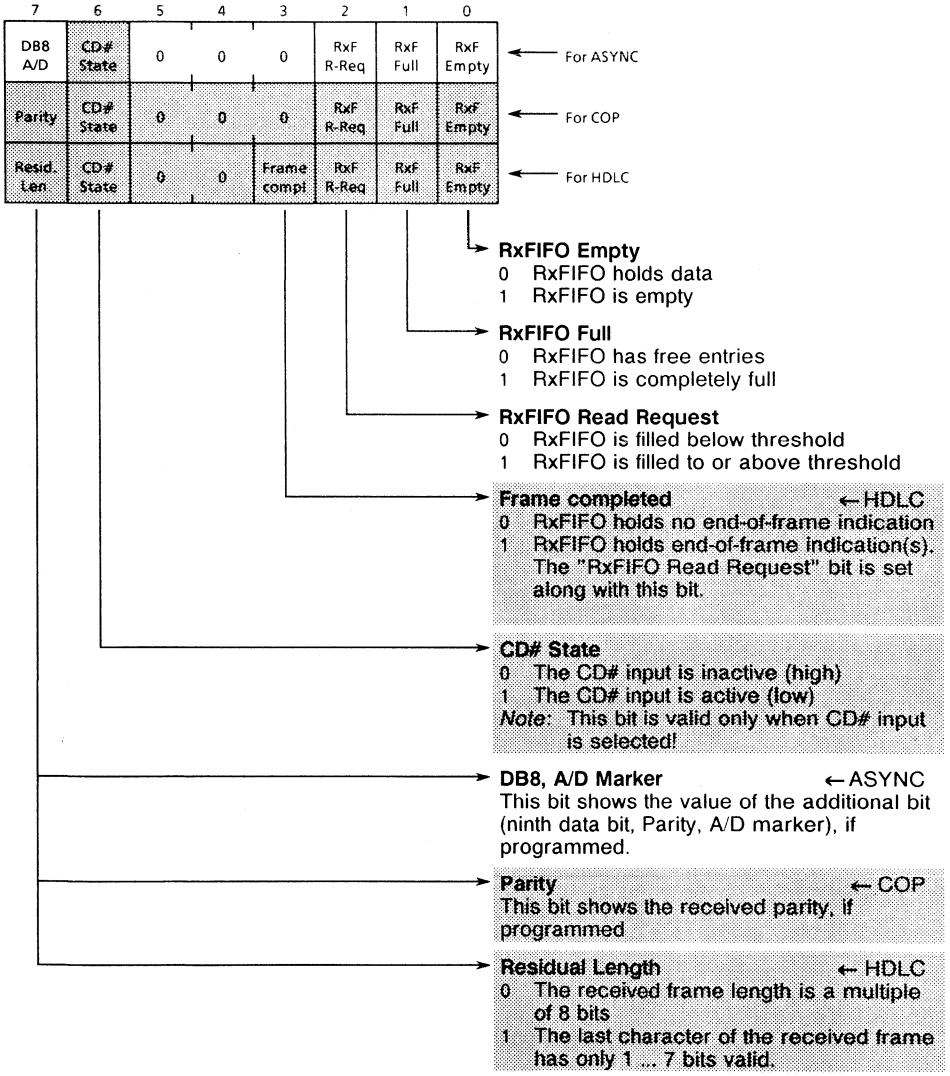
CRC On/Off ←COP
0 CRC checker disabled
1 CRC checker active (enabled)

Lock RxFIFO
0 Received data is transferred from the RxShift register to the RxFIFO
1 The RxFIFO is locked, completely received data is lost. (This bit can be reset by Automatic Receive Control)

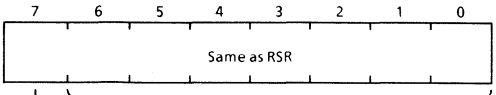
Rx Enable
0 The receiver is disabled
1 The receiver is active (operation depends on additional receiver control)

Set/Reset
The value of this bit is written to the command bits marked (with "1") in the other bit positions of this register.

Receive Status Register (RSR), offset 56/76$_H$ (channel A/B):



RSR 16-bit Extension (RSRX), offset $57/77_H$ (channel A/B):



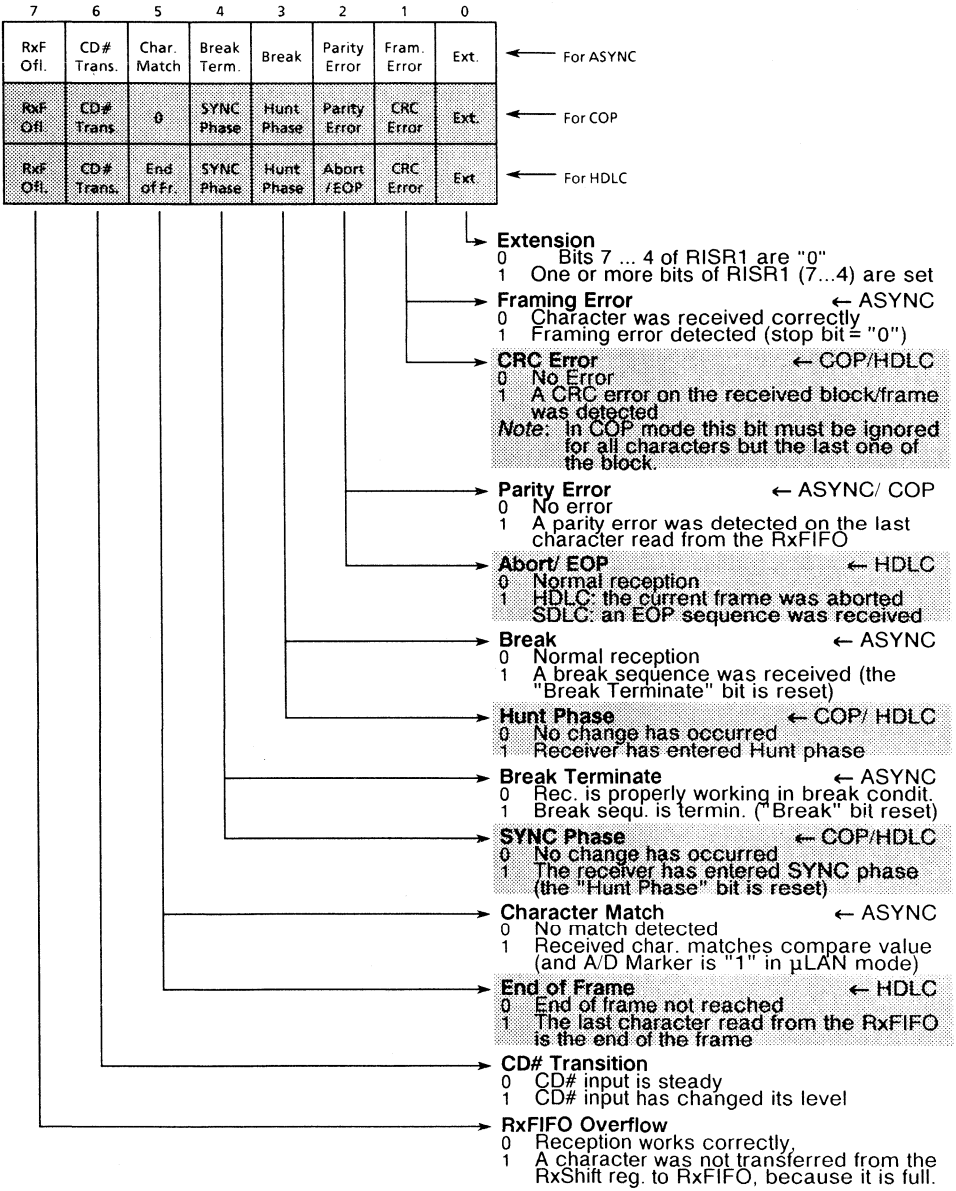
Duplicated
The values of these bit positions are equal to the corresponding bits of the RSR.

DB8, A/D Marker ← ASYNC

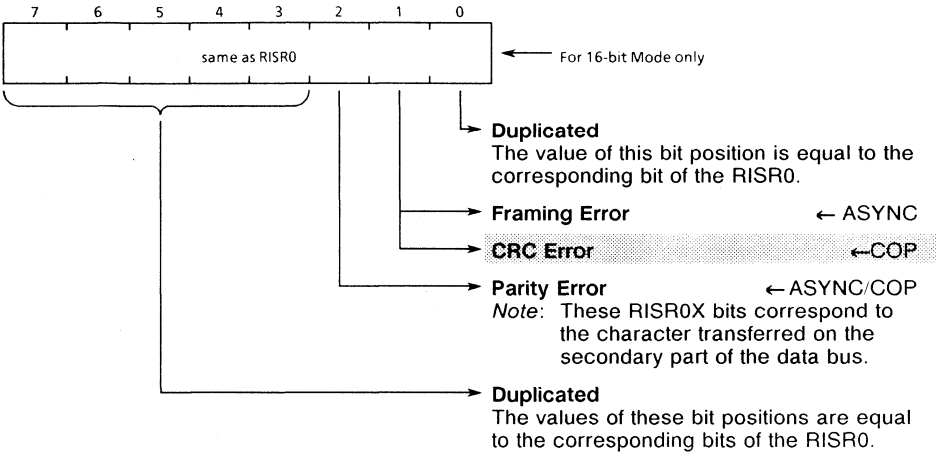
Parity ← COP

Note: This bit of the RSRX corresponds to the character transferred on the secondary part of the data bus.

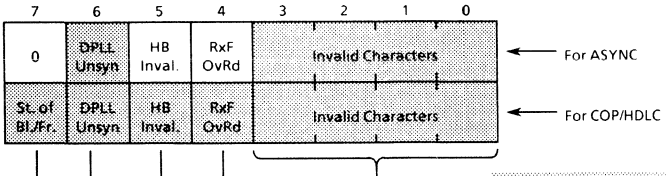
Receive Interrupt Status Register 0 (RISR0), offset 58/78$_H$ (channel A/B):



RISR0 16-bit Extension (RISR0X), offset $59/79_H$ (channel A/B):



Receive Interrupt Status Register 1 (RISR1), offset 5A/7A$_H$ (channel A/B):



Invalid Characters
Indicates the number of the bytes tried to read from the RxFIFO (unsuccessful) (valid if RxFIFO "Overread" = "1"

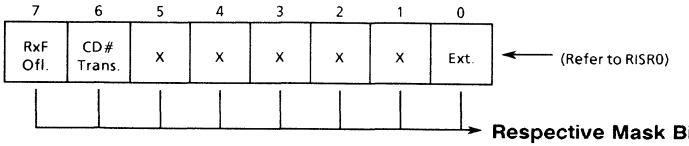
RxFIFO Overread
0 All read accesses valid
1 Some read accesses were invalid (see "Invalid Characters")

High Byte Invalid
0 16-bit read access is valid
1 Only the lower 8 bits of the word are valid

DPLL Unsynchronized
0 DPLL works correctly
1 DPLL has lost synchronization
Note: valid only, if the DPLL is active

Start of Block/Frame ← COP/HDLC
0 Receiver is idling or within a block/frame
1 The first byte of a block or frame was received
Note: The first byte may be a SYN character, if "SYN Character Load Inhibit" is "0" (COP mode)

Receive Interrupt Mask Register (RIMR), offset 5B/7B$_H$ (channel A/B):



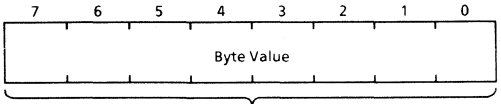
Respective Mask Bit

0 The respective condition also generates an interrupt.

1 The respective condition is indicated in the RISR0, but no interrupt is generated.

Note: "X" stands for the different meanings of these bits in the different modes according to RISR0.

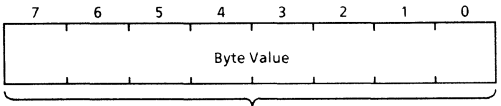
Data Register (DR) for Transmitter/Receiver, offset 5E/7E$_H$ (channel A/B):



Write Access
Transfers data to the TxFIFO

Read Access
Transfers data from the RxFIFO

DR 16-bit Extension (DRX), offset 5F/7F$_H$ (channel A/B):



Write Access
Transfers data to the TxFIFO
- Before the DR-byte in Mot. Bus Mode
- After the DR-byte in Intel Bus Mode

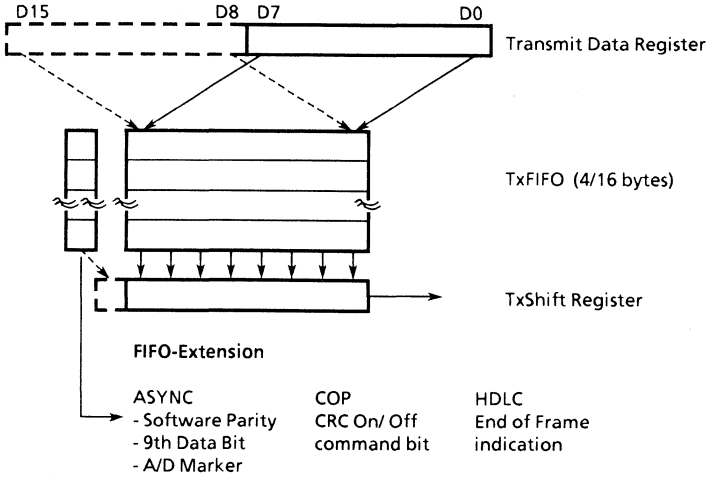
Read Access
Transfers data from the RxFIFO
- holds first char. in Motorola Bus Mode
- holds second char. in Intel Bus Mode

Note: Transfers from and to the DRX are executed only, if the respective FIFO has a free entry or a valid character, respectively.

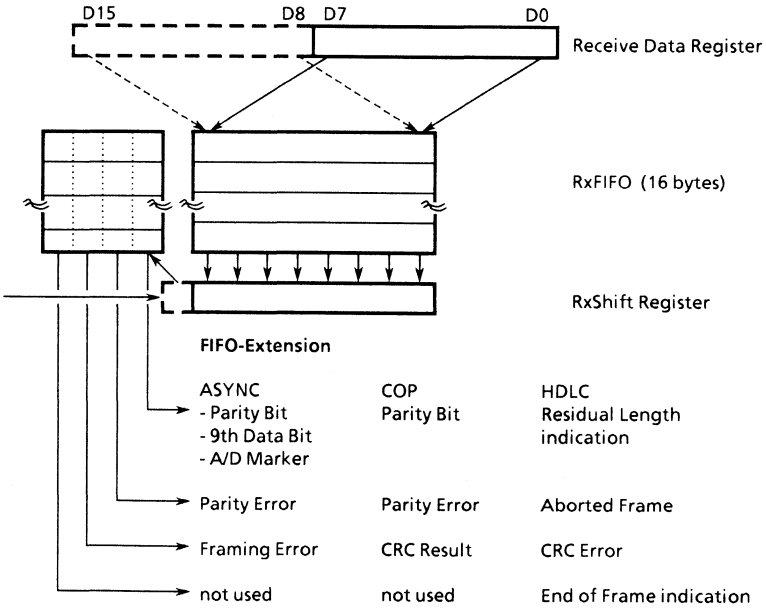
FIFO Structure

The receive and transmit FIFOs of the USIC store additional control information along with the data (see figures below). This control information is processed, when the corresponding data is processed.

The Transmit FIFO:



The Receive FIFO:



Parallel Interface Operation

The USIC's parallel interface provides a maximum of three 8-bit I/O ports (PA, PB, PC) and 9 input lines (T0IN, T0GATE, T1IN, T1GATE, INTE, TxCB, RxCB, CTSA#, CTSB#). All these lines may be used for general purpose input or output (port lines only), or may serve for additional control functions (see pin description for summary).

The following sections will describe how to operate the three 8-bit I/O ports and will list their alternate functions. The nine additional input lines are described in the chapters corresponding to their primary function.

Parallel Port A

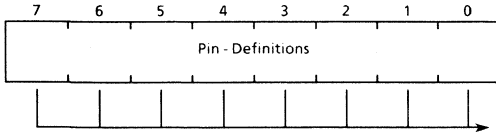
The USIC's port A can be used in three major modes:

- General purpose input or output
- Set of control lines (LDE#/BHE#, EODT#, EODR#, CDB#, RTSA#, RTSB#, RDYB, STB#/ACK#) as shown in the "Alternate Pin Definitions"
- Set of level or edge triggered interrupt lines.

The interrupt line mode may be combined with the other two modes. The transition detection logic may operate independently from the interrupt control unit and allows to monitor signal transitions on the port A lines.

Seven registers control port A operation:

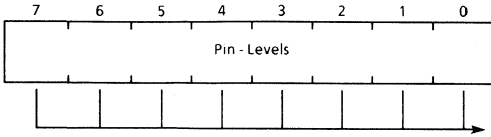
Port A Control Register (PACR), offset 10_H:



Pin Definition

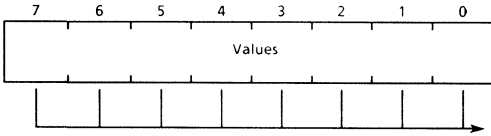
0 The corresponding port line is an input.
1 The corresponding port line is an output

Port A Pin State Register (PAPSR), offset 11_H:



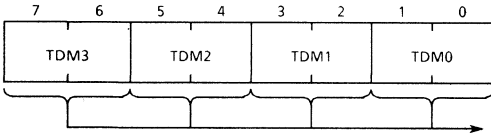
Pin Level
The actual level at the corresponding pin can be read, independent from its current function.
Note: This register can be read only.

Port A Output Latch (PAOL), offset 12_H:



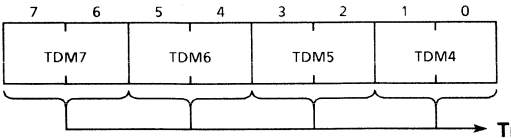
Value
The values written to the output latch control the level of those pins used for output. The PAOL may be read back.

Transition Detect Mode Register 0 (TDMR0), offset 13_H:



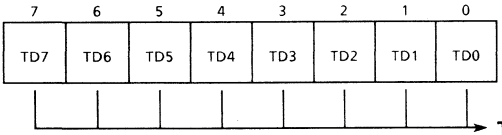
Transition Detect Mode for pins PA0-3
0 0 Transition detection disabled,
The detection latch will always read out zero.
0 1 Positive Edge Triggered
The detection latch is set on a rising edge of the pin level (low - high)
1 0 Negative Edge Triggered
The detection latch is set on a falling edge of the pin level (high - low)
1 1 Transition Triggered
The detection latch is set, whenever the pin level changes

Transition Detect Mode Register 1 (TDMR1), offset 14_H:



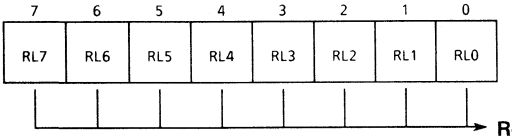
Transition Detect Mode for pins PA4-7
Programming identical to TDMR0.

Transition Latch Register (TLR), offset 15_H:



Transition Detected
0 Pin has kept its level.
1 A transition has occurred as programmed via TDMR0/1.
Note: This information always refers to the time the latch has last been reset.

Transition Latch Reset Register (TLRR), offset 16_H:



Reset Latch
0 No operation
1 Reset detection latch with the rising edge of WR# (DS#).

Parallel Port B

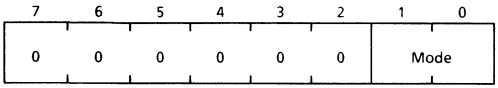
The USIC's port B can be used in three major modes:

- Standard general purpose input or output
- Handshake controlled general purpose input or output
- Upper half of the 16-bit data bus

If port B is selected to serve as upper data bus half, all other programming is invalid and disregarded.

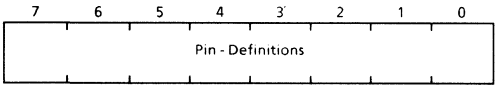
Four registers control port B operation:

Port B Control Register 0 (PBCR0), offset 17_H:



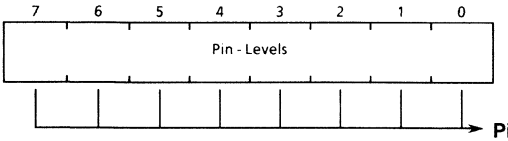
Mode Control
0 X Standard general purpose input or output (as defined in PBCR1)
1 0 Handshake controlled input
1 1 Handshake controlled output

Port B Control Register 1 (PBCR1), offset 18_H:



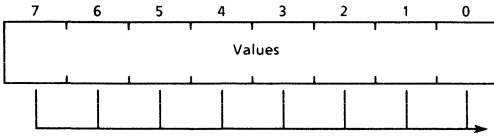
Pin Definition
0 The corresponding port line is an input
1 The corresponding port line is an output

Port B Pin State Register (PBPSR), offset 19_H:



Pin Level
The actual level at the corresponding pin can be read, independent from its current function.
Note: This register can be read only.

Port B Output Latch (PBOL), offset $1A_H$:



Value
The values written to the output latch control the level of those pins used for output. The PBOL may be read back.

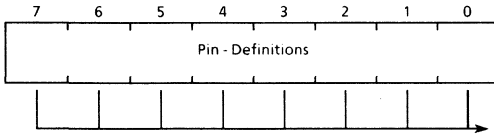
Parallel Port C

The USIC's port C can be used in two major modes:

- General purpose input or output
- Set of control lines to support interrupt unit, DMA control or serial channel B

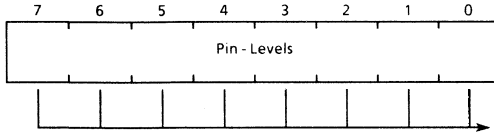
Three registers control port C operation:

Port C Control Register (PCCR), offset $1B_H$:



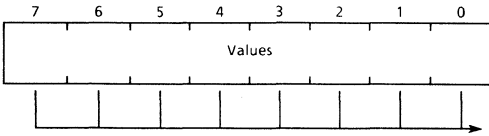
Pin Definition
0 The corresponding port line is an input
1 The corresponding port line is an output

Port C Pin State Register (PCPSR), offset $1C_H$:



Pin Level
The actual level at the corresponding pin can be read, independent from its current function.
Note: This register can be read only.

Port C Output Latch (PCOL), offset $1D_H$:

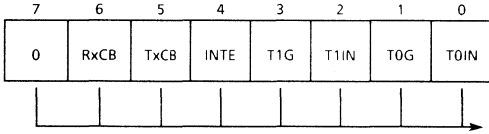


Value
The values written to the output latch control the level of those pins used for output. The PCOL may be read back.

Additional Input lines

9 additional pins of the USIC may be used for general purpose input, if their native function is not required. The CTS# lines can be monitored through the transmit status registers, the other 7 lines can be sampled through a special register:

Pin State Register (PSR), offset $1F_H$:



Pin Level
The actual level at the corresponding pin can be read, independent from its current function.
Note: This register can be read only.

The PSR can be read even if the corresponding lines are used for control. Please note, however, that the information may be useless, if the signal applied to the control lines changes frequently.

Timer/Counter Operation

The three timers/counters of the USIC's timer/counter unit can be programmed to generate a variety of output signals from a series of input signals.

Because the state of the timer/counter unit after power-up is undefined, each counter must be programmed before it can be used. This is done by writing a control word and an initial count into the appropriate registers.

The programming sequence may be arbitrary, provided that two rules are obeyed to:

- the command word must be written before the corresponding initial count
- the initial count must follow the programmed sequence (see Read/Write Control)

Information from the counters can be obtained using one of three different methods:

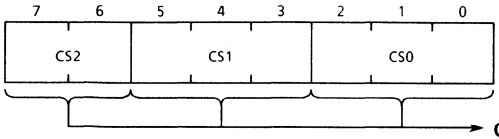
- Direct Read operation
  The contents of a counting element may be read directly by the host. To prevent undefined results due to a changing count during read, the counter should be stopped for reading.
- Counter Latch Command
  The contents of a counting element may be copied to the counter output latch (with the counter latch command) and be read from there by the host. This approach allows to read a counter "on-the-fly" without having to stop it.
- Read Back Command
  The Read Back Command allows to latch the contents and/or the status of one or multiple counters. On reading status and contents of a counter the status is always output first.

Note: **The shaded options are not available for timer/counter 2.**

Input Signal Selection

The counting elements can be clocked by a number of external and internal clock signals. The counter clock select register chooses from 8 (counter 0 and 1) or 4 (counter 2) different sources.

Counter Clock Select Register (CCSR), offset 24_H:



Clock Source

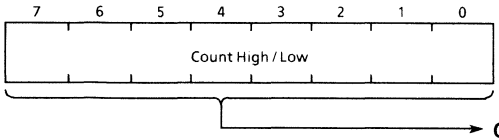
0 0 0	System Clock CLK
0 0 1	Receiver A Character Strobe 1)
0 1 0	Receiver B Character Strobe 1)
0 1 1	Transmitter B Character Strobe 1)
1 0 0	Timer clock input pin
1 0 1	Baudrate generator 0
1 1 0	Baudrate generator 1
1 1 1	Transmitter A Character Strobe 1)

Note 1):
A count pulse is generated for each character transferred to or from the FIFO.

Timer/Counter value programming

The 16-bit values for each timer are loaded via the respective counter register (CRn) as programmed in the CCWR (R/W control). High byte, low byte or both are loaded via the counter registers.

Counter Register 0/1/2 (CR0/1/2), offset 20_H / 21_H / 22_H:



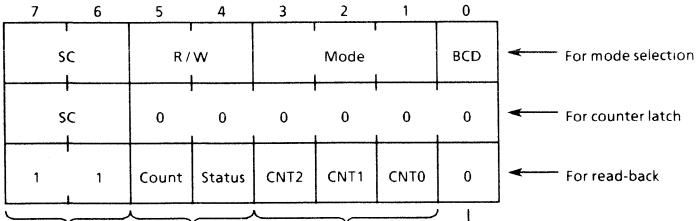
Counter Init Value(s)
Accepts the low and/or high byte (as programmed in the CCWR) to specify the init value for the respective counter.

Operating Mode Selection

The counter control word register accepts commands to

- program the operating mode of a counter
- issue the counter latch command
- issue the read-back command.

Counter Control Word Register (CCWR), offset 23_H:



BCD ← Mode
0 The selected element is a 16-bit binary counter
1 The selected element is a 4-decade Binary-Coded-Decimal counter

Mode ← Mode
0 0 0 Select mode 0
0 0 1 Select mode 1
0 1 0 Select mode 2
0 1 1 Select mode 3
1 0 0 Select mode 4
1 0 1 Select mode 5

CNTn (counter select) ← Read-back
0 Counter **n** not affected
1 Command applies to counter **n**

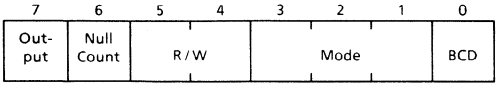
Status# ← Read-back
0 Latch status of selected counter(s)
1 No operation

R/W (Read/Write control) ← Mode
0 0 See counter latch command
0 1 Read/write least significant byte only
1 0 Read/write most significant byte only
1 1 Read/write least significant byte first, then most significant byte

Count# ← Read-back
0 Latch contents of selected counter(s)
1 No operation

SC (Select Counter) ← Mode/ C. latch
0 0 Operation applies to counter 0
0 1 Operation applies to counter 1
1 0 Operation applies to counter 2
1 1 See Read-back command

After issuing a Read-Back command that latches a counter's status, the first read access to that counter provides the following status information:



BCD, Mode, R/W
These fields show the current operating mode as programmed via the CCWR.

Null Count
0 The initial count loaded was copied to the counting element
1 The initial count loaded is not yet copied to the counting element

Output
This bit shows the current level of the counter's output pin.
Note: Counter 2 does not provide an output pin!

Mode Definitions

Conventions:

CLK pulse - a falling edge after a rising edge on a counter's CLK input

Trigger - a rising edge on a counter's GATE input

Counter loading - copying a count value from the count register (loaded by the host) to the counting element

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After writing the control word and the initial count the counter's output is low. The first CLK pulse loads the respective counter, the following pulses count it down. When the counter reaches zero, its output goes high and remains high, until the counter is reprogrammed. If a two-byte count is written, counting is disabled between the two write accesses. Counting may also be disabled via the GATE input ("0"). Note that GATE = "0" does not prevent the loading of the counter on the next CLK pulse after programming.

The counter itself can be reprogrammed any time even if it is running (watch two-byte operation).

Mode 1: Hardware-Retriggerable Single-Shot

The counter's output will be initially high. It will go low on the CLK pulse following a trigger to begin the single-shot pulse, and will remain low until the counter reaches zero. The output will then go high and remain high until the CLK pulse after the next trigger.

After writing the control word and initial count, the counter is armed. A trigger results in loading the counter and setting the output low on the next CLK pulse, thus starting the single-shot pulse. An initial count of *N* will result in a single-shot pulse *N* CLK cycles in duration. The single-shot is retriggerable, hence the output will remain low for *N* CLK pulses after any trigger. The single-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on the output.

If a new count is written to the counter during a single-shot pulse, the current single-shot is not affected unless the counter is retriggered. In that case the counter is loaded with the new count and the pulse continues until the new count expires.

Note that this mode is not available on timer/counter 2!

Mode 2: Rate Generator

This mode functions like a divide-by-*N* counter. It is typically used to generate a real-time clock interrupt. The counter's output will initially be high. When the initial count has decremented to 1, the output goes low for one CLK pulse. It then goes high again, the counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated infinitely. For an initial count of *N*, the sequence repeats every *N* CLK cycles.

GATE = "1" enables counting; GATE = "0" disables counting. If GATE goes low during an output pulse, the output is set high immediately. A trigger reloads the counter with the initial count on the next CLK pulse. The output goes low *N* CLK pulses after the trigger. Thus the GATE input can be used to synchronize the counter.

Note that this feature is not available on timer/ counter 2.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. The output goes low *N* CLK pulses after the initial count is written. This allows the counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise the new count will be loaded at the end of the current counting cycle. In mode 2 a count value of 1 is illegal.

Mode 3: Square Wave Generator

Mode 3 is similar to mode 2 except for the duty cycle of the counter's output. This will initially be high. When half the initial count has expired, the output goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated infinitely. An initial count of *N* results in a square wave with a period of *N* CLK cycles.

GATE = "1" enables counting; GATE = "0" disables counting. If GATE goes low while the output is low, this is set high immediately; no CLK pulse is required. A trigger reloads the counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the counter.

Note that this feature is not available on timer/ counter 2.

After writing a control word and initial count, the counter will be loaded on the next CLK pulse. This allows the counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the counter will continue from the new count. Otherwise the new count will be loaded with the new count on the next CLK pulse and counting will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: The output is initially high. The initial is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, the output changes value and the counter is reloaded with the initial count. The above process is repeated infinitely.

Odd counts: The output is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, the output goes low and the counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, the output goes high again and the counter is reloaded with the initial count minus one. The above process is repeated infinitely. So for odd counts the output will be high for $(N + 1) / 2$ counts and low for $(N - 1) / 2$ counts.

Mode 4: Software-Triggered Strobe

The counter's output will be initially high. When the initial count expires, the output will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = "1" enables counting; GATE = "0" disables counting. GATE has no effect on the output.

After writing a control word and initial count the counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of *N* the output does not strobe low until *N* + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.

2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. The output strobes low *N* + 1 CLK pulses after the new count of *N* is written.

Mode 5: Hardware-Triggered Strobe

The counter's output will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, the output will go low for one CLK pulse and then go high again.

After writing the control word and initial count the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of *N* the output does not strobe low until *N* + 1 CLK pulses after a trigger. A trigger results in the counter being loaded with the initial count on the next CLK pulse. The counting sequence is not retriggerable. The output will not strobe low for *N* + 1 CLK pulses after any trigger. GATE has no effect on the output.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Note that this mode is not available on timer / counter 2.

Counter Operation

The counters are loaded or decremented on the falling edge of CLK.
The minimum initial count is "2" for modes 2 and 3, it is "1" for all other modes.
The maximum initial count is "0" for all modes, which equals "2^{16}" in Binary mode and "10^4" in BCD mode.

When a counter reaches zero, it will continue counting rather than stop. In modes 2 and 3, which are periodic, the counter is automatically reloaded with the corresponding initial count. In all other modes the counter "wraps around" to the largest possible count, i.e. "$FFFF_H$" in Binary mode and "9999" in BCD mode.

The GATE inputs can be used to control the operation of timers/counters 0 and 1 (see table below).

GATE Pin Operation Summary

Mode	Signal Status		
	Low or Going Low	Rising	High
0	Disables Counting	-	Enables Counting
1	-	1) Initiates Counting 2) Resets Output after Next CLK	-
2	1) Disables Counting 2) Sets Outputs immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Outputs immediately High	Initiates Counting	Enables Counting
4	Disables Counting	-	Enables Counting
5	-	Initiates Counting	-

Interrupt Request Generation

The outputs of all three timers/counters can generate internal interrupts via edge detector flip-flops.

These flip-flops are
- **set** on the rising edge of the counter's output.
- **reset** when the corresponding interrupt vector is placed on the bus.

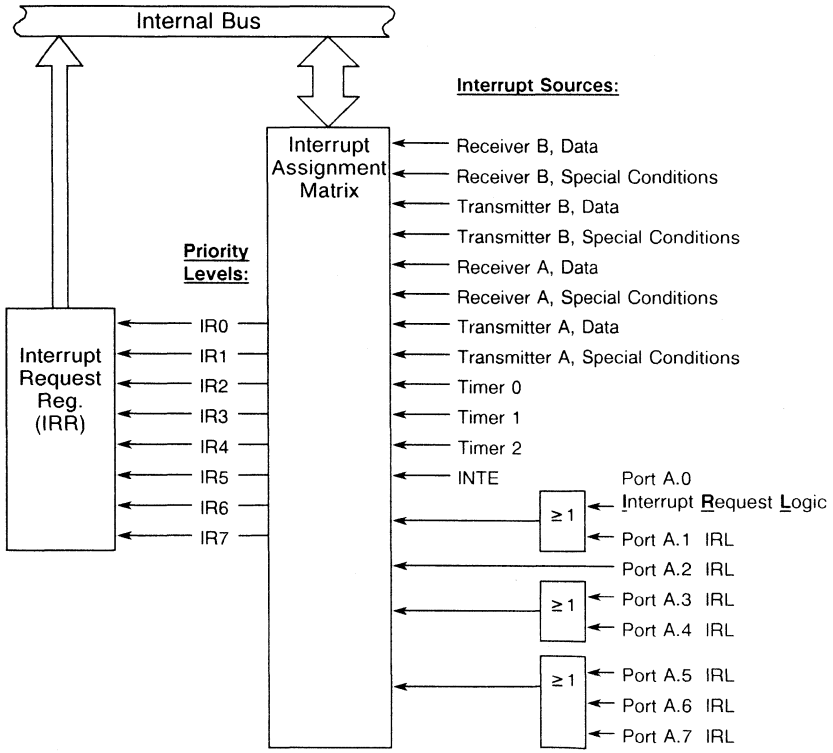
Interrupt Control Operation

The USIC's interrupt control unit connects up to 11 internal interrupt sources and up to 9 external interrupt sources (or 16, if a cascaded slave is used) to the host processor's interrupt input. Most interrupt sources can be individually assigned to one of eight priority levels.

Interrupt Sources

The interrupt control unit accepts interrupts from the serial interface unit and the timer/counter unit as well as from port A's interrupt request logic and from external sources via INTE (direct or cascaded).

Interrupt Assignment to Priority Levels



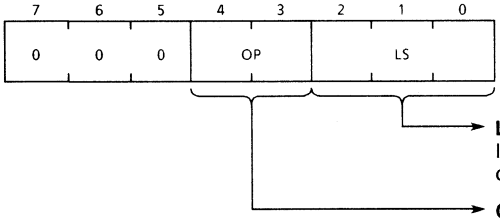
Priority Assignment

Each of the USIC'S 16 interrupt sources can individually be assigned to one of 8 priority levels. This is done by programming the Interrupt Assignment Matrix through the select and control registers (see description below). Normally several sources will share the same priority level (Note, however, that the generated interrupt vectors are related to the interrupt source rather than to the level). If more than one interrupt request is pending for a given level, the numerically smallest vector (see table) is output first, then another request for the same level is generated.

The specific Set/Reset command operates on those interrupt sources marked within the select registers.

Note:
An interrupt source, which is not assigned to any priority level, is disconnected from the interrupt logic. I.e. the interrupt assignment matrix can also be used as an interrupt mask to enable and disable certain interrupt sources.

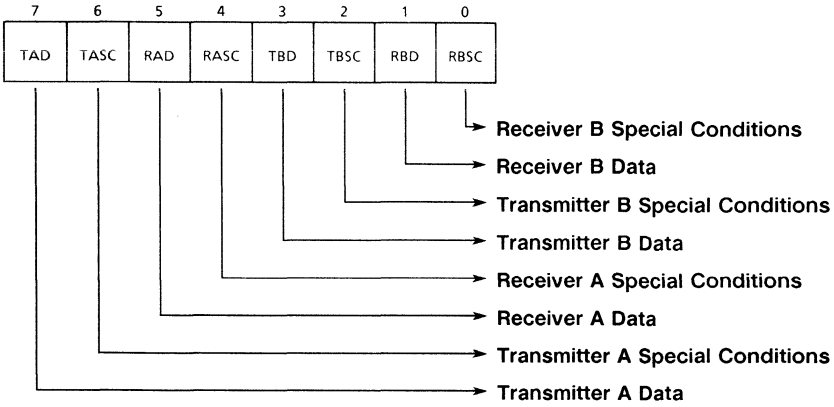
Interrupt Assignment Control Register (IACR), offset 32_H:



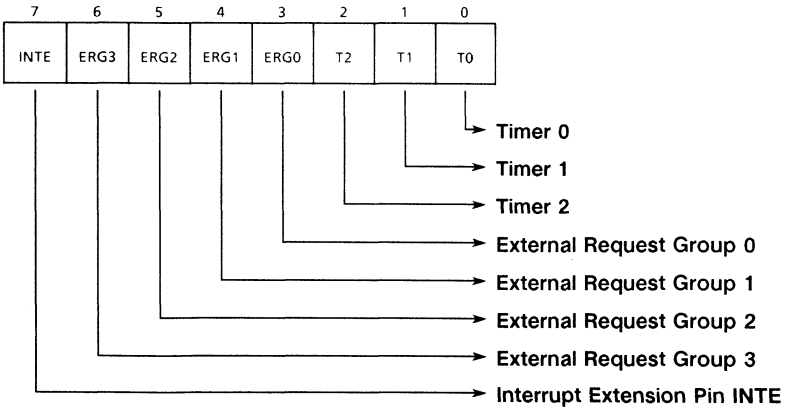
Level Select
Is the binary coded interrupt priority level the operation refers to (except "11").

Opcode
0 0 Read back assignments of level LS
0 1 Set assignments for level LS
1 0 Reset assignments for level LS
1 1 Reset all assignments

Interrupt Assignment Source Select 0 (IASS0), offset 33_H:



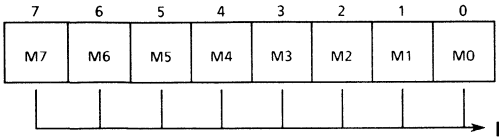
Interrupt Assignment Source Select 1 (IASS1), offset 34_H:



Special control is provided for interrupts generated via the Port A pins. Each individual input can be masked, can be operated in one of two different modes and can be checked for pending interrupts.

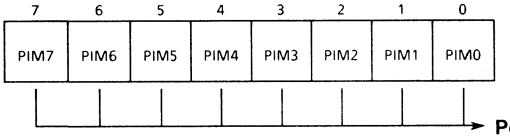
Three special registers are provided for these purposes:

Port Interrupt Request Mask Register (PIRMR), offset 38_H:



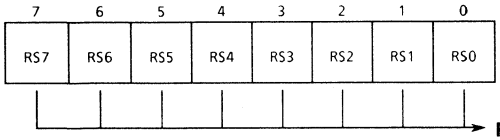
Mask Bit
0 Corresponding Port A Pin can accept interrupts
1 Corresponding Port A Pin is masked

Port Interrupt Mode Register (PIMR), offset 39_H:



Port Interrupt Generation Mode
0 Generate request, if pin is at high level
1 Generate request, if transition detection latch is at high level

Port Interrupt Request Status Register (PIRSR), offset $3A_H$:



Request Status
0 No request from corresponding pin
1 Corresponding pin has request pending

Pending interrupts for the different priority levels are indicated in the Interrupt Request Register IRR. During an interrupt acknowledge sequence the request with the currently highest priority generates its programmed vector. This is indicated in the In-Service Register ISR. This register indicates which priority levels are currently being serviced. The individual sources which have interrupts pending or are in-service can be read via ISR0 and ISR1.

The vectors that are sent to the CPU consist of two parts:

- The lower 4 bits identify the requesting source (see table below).
- The upper 4 bits are programmable via ICW2 and can be used to identify requesting devices (e.g. different USICs).

Interrupt Sources and Vector Offsets:

D3 - D0 of Interrupt Vector		Associated Interrupt Source
0000	(0H)	Receiver B, Special Conditions
0001	(1H)	Receiver B, Data (FIFO threshold matched)
0010	(2H)	Transmitter B, Special Conditions
0011	(3H)	Transmitter B, Data
0100	(4H)	Receiver A, Special Conditions
0101	(5H)	Receiver A, Data
0110	(6H)	Transmitter A, Special Conditions
0111	(7H)	Transmitter A, Data
1000	(8H)	Timer 0
1001	(9H)	Timer 1
1010	(AH)	Timer 2
1011	(BH)	External Request Group 0 (Port Interrupt Requests 0,1)
1100	(CH)	External Request Group 1 (Port Interrupt Request 2)
1101	(DH)	External Request Group 2 (Port Interrupt Requests 3,4)
1110	(EH)	External Request Group 3 (Port Interrupt Requests 5,6,7)
1111	(FH)	INTE

Interrupt Sequence

- Active Interrupt sources are evaluated and generate an INT signal to the CPU.
- The CPU acknowledges by sending one (Motorola Bus Mode) or two (Intel Bus Mode) INTA# pulses.
- During the first INTA# cycle the highest priority ISR-bit and SISR-bit is set, and the respective IRR-bit and SIRR-bit is reset (only, if no other source on this level is active).
- During the last INTA# cycle the USIC provides the interrupt vector on data lines D7 ... D0.
- The ISR-bit and SISR-bit is reset, if an appropriate EOI command is received from the CPU.

Note:
In Motorola Bus Mode the terms "first" and "last" INTA# cycle both refer to the one INTA# cycle that occurs.

Interrupt Controller Core Programming

The USIC's interrupt controller core is programmed through 2 to 4 initialization command words (ICWs) and up to 3 operation control words (OCWs) similar to the standard SAB 82C59A. Like in the standard device the command/control words are entered into two locations, the Interrupt Core Control Registers (ICCR0, ICCR1).

Interrupt Core Control Register 0 (ICCR0), offset 30_H:

Is used to enter ICW1s, OCW2s and OCW3s and to read the IRR and ISR.

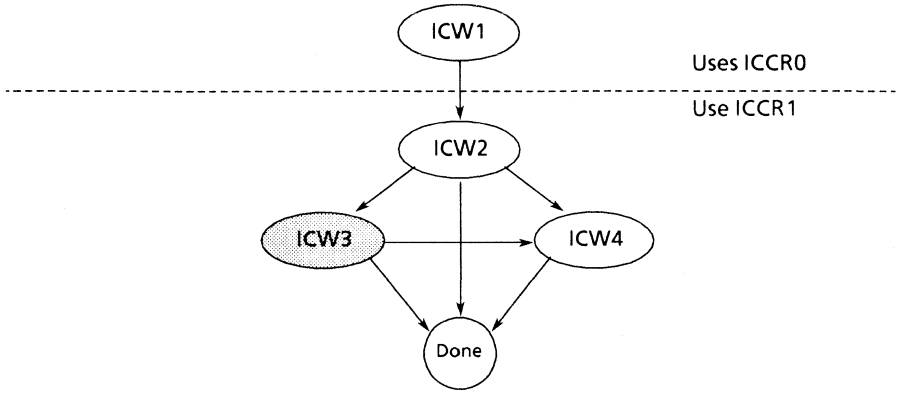
Interrupt Core Control Register 1 (ICCR1), offset 31_H:

Is used to enter ICW2s to ICW4s and OCW1s and to read the IMR.

Initialization Command Words

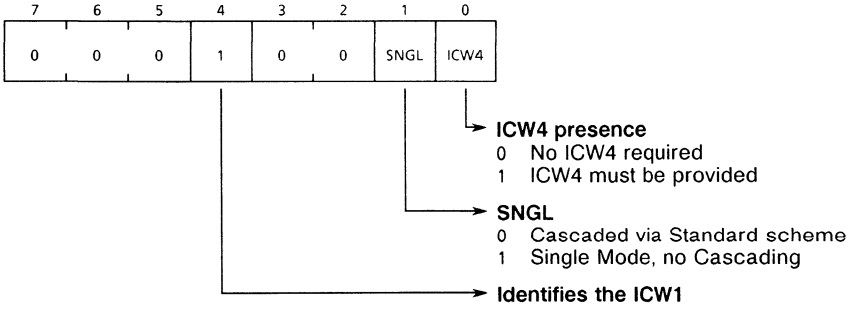
A sequence of ICWs teaches the interrupt control unit which operating mode is desired. According to the specific operating mode (see ICW description) 2, 3 or 4 ICWs must be written by the CPU (see figure).

Possible ICW Sequences

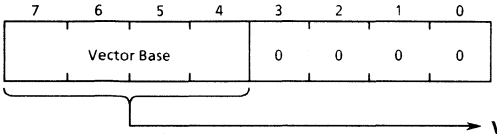


Note:
The shaded command options are not available/necessary, if the USIC is operating in Motorola Bus Mode.

Initialization Command Word 1 (into ICCR0):

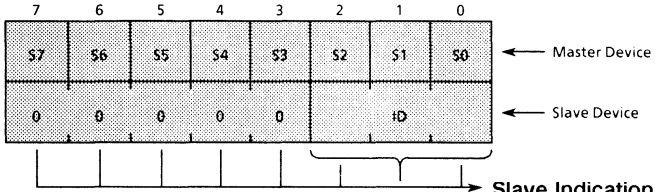


Initialization Command Word 2 (into ICCR1):



Vector Base
Specifies the interrupt vector base to which the vector offsets (see table) are added to form the complete interrupt vectors for the CPU

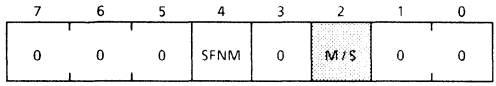
Initialization Command Word 3 (into ICCR1):



Slave Indication ← Master
0 This priority level has regular request inputs
1 This priority level has a slave device connected
Note: Only one level (INTE) can have a slave connected

Identification ← Slave
Programs the slave ID which the slave device will compare with the CAS input during interrupt acknowledge cycles

Initialization Command Word 4 (into ICCR1):



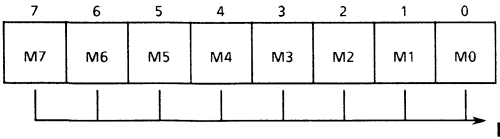
Master/Slave Select
0 This device is a slave device
1 This device is the master device (Default after RESET)

Special Fully Nested Mode
0 Standard Nested Mode
1 Special Fully Nested Mode

Operation Control Words

Once the interrupt control unit has been initialized, three different control words can be used to control and check the running operation:

Operation Control Word 1 (into ICCR1):

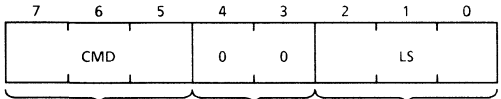


Mask Bit

0 Interrupts of the corresponding level are enabled

1 Interrupts of the corresponding level are masked

Operation Control Word 2 (into ICCR0):



Level Select
Is the binary coded interrupt priority level the command acts upon

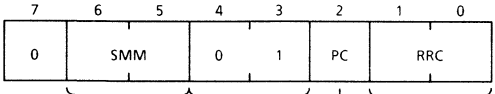
Identify the OCW2

Command

0 0 0 reserved
0 0 1 Non specific EOI command
0 1 0 No operation
0 1 1 Specific EOI command [1]
1 0 0 reserved
1 0 1 Non specific EOI command with rotation
1 1 0 Set level <LS> to lowest priority [1]
1 1 1 Specific EOI command which sets level <LS> to lowest priority [1]

Note [1]:
This command uses the OCW2's LS field

Operation Control Word 3 (into ICCR0):



Read Register Command
0 X No operation
1 0 Select IRR for read access via ICCR0 (Default after RESET)
1 1 Select ISR for read access via ICCR0

Poll Command
0 No operation
1 Poll Command: output interrupt ID during next read access to ICCR0

Identify the OCW3

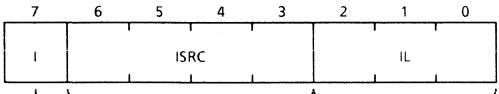
Special Mask Mode
0 X No operation
1 0 Disable special mask mode
1 1 Enable special mask mode

Polling

During Polling the processor uses read accesses to input the interrupt vectors rather than using the INT/INTA# mechanism. This mode is chosen either, if the INT line to the processor cannot be used, or in order to expand the number of priority levels beyond 64. After issuing a poll command the processor can read a byte (see Interrupt ID description below) which tells,

- if there is a pending interrupt anyway, and if yes,
- which source is requesting (see table)
- which priority level is associated with the source.

Interrupt ID for Polling (from ICCR0):



Interrupt Level
Is the binary coded highest priority level which has an interrupt pending

Interrupt Source
Identifies the requesting interrupt source as listed in the vector offset table

Indicator
0 There is no interrupt pending
1 Interrupt pending, see ISRC, IL

Status Information

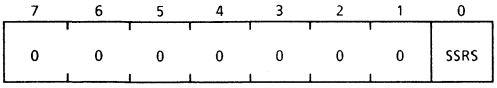
The following additional status information on the interrupt control unit can be obtained:

- Interrupt Request Register (IRR) indicates, which priority levels have interrupts pending (read via ICCR0).
- In-Service Register (ISR) indicates, which priority levels are currently being serviced (read via ICCR0).
- Interrupt Mask Register (IMR) indicates, which priority levels are enabled or masked (read via ICCR1).
- Source Interrupt Request Registers (SIRR0, SIRR1) indicate, which sources have interrupts pending (read via ISR0, ISR1).
- Source In-Service Registers (SISR0, SISR1) indicate, which interrupts (which sources) are currently in service (read via ISR0, ISR1).

Notes:

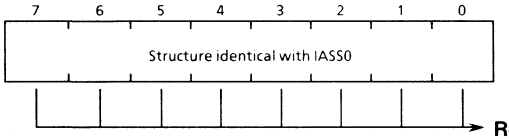
- The poll command overrides status information when reading the ICCR0.
- SIRRx or SISRx are selected via SSSR, see description below.

Source Status Select Register (SSSR), offset 35_H:



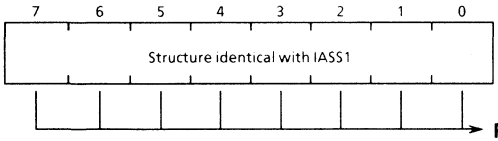
Source Status Register Select
0 Read SIRR0, SIRR1 via ISR0, ISR1 (Default after RESET)
1 Read SISR0, SISR1 via ISR0, ISR1

Interrupt Status Register 0 (ISR0), offset 36_H:



Respective Source
0 No interrupt pending or in service
1 This source has an interrupt pending or currently in service

Interrupt Status Register 1 (ISR1), offset 37_H:



Respective Source
0 No interrupt pending or in service
1 This source has an interrupt pending or currently in service

Special Mask Mode

When a specific priority level is currently active (i.e. In-Service bit is set), in normal mode all interrupts from lower levels are inhibited. In Special Mask Mode all other levels are enabled. The IMR selects the levels which are enabled in Special Mask Mode. This selection may be altered dynamically by the running service routine.

Special Fully Nested Mode

In normal nested mode all interrupts from a priority level which is currently active (i.e. In-Service bit is set) are inhibited.

In special fully nested mode interrupts from the currently active level will also be serviced. This can be useful, if a cascaded slave is associated with that (master) level. Also higher levels of the slave can interrupt the active service routine.

Note:
If the special fully nested mode is used in such a cascaded configuration, the software has to check (when leaving a service routine), whether the interrupt serviced was the only one from that slave! This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI command can be sent to the master, too. If not, no EOI command should be sent.

Summary Special Modes:

Operating Mode	Priority Level		
	Lower	Active	Higher
Normal Mode	inhibited	inhibited	enabled [1]
Sp.Mask Mode	enabled [1]	inhibited	enabled [1]
Sp.F.Nested Mode	inhibited	enabled [1]	enabled [1]
SMM + SFNM	enabled [1]	enabled [1]	enabled [1]

Note[1]: I.e. an interrupt will be serviced, if it is not masked by an IMR bit.

End of Interrupt

When an interrupt request is acknowledged, the corresponding priority level is indicated by setting the respective In-Service bit in the ISR. This bit must be reset in order to reenable interrupts from this and lower levels (except special fully nested mode and special mask mode).

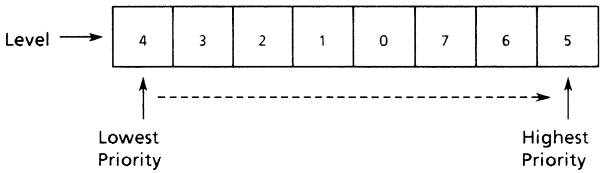
Two ways are possible to reset the ISR bits:

- **Non-specific EOI command** (OCW2)
  A non-specific EOI command resets the highest ISR bit which is set. This command can be used in systems which preserve the fully nested structure.
- **Specific EOI command** (OCW2)
  A specific EOI command resets the ISR bit which is specified in the LS-field of the OCW2. This command is used in systems which have structures other than fully nested (e.g. special fully nested mode).

  Note: A specific EOI command will not reset an ISR bit which is masked by an IMR bit, if the special mask mode is active!

Priority Rotation

Initially level 0 has highest and level 7 has lowest priority. To change this fixed rule the priorities of the different levels can be rotated. Hereby a specific level receives lowest priority, the other levels are changed accordingly. If for example level 4 receives lowest priority, the situation would look like this:



There are three ways to rotate priorities (using OCW2):

- Set Level Command (CMD = 110)
  Explicitely specifies the level to receive lowest priority.
- Specific EOI Command (CMD = 111)
  The normal specific EOI command can be used to specify the lowest priority level.
- Non-Specific EOI Command (CMD = 101)
  The non-specific EOI command can be used to assign lowest priority to the level which was serviced recently.

Interrupt Duration

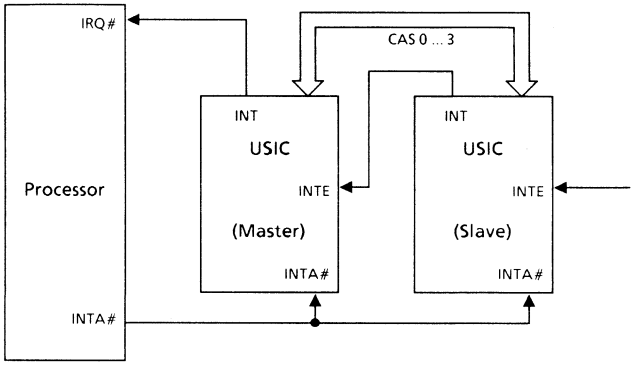
An interrupt is recognized by a high level on the IRx line. Before the EOI command is issued the appropriate interrupt must be removed, or another request is generated to the host processor. If the interrupt disappears before the falling edge of the first INTA# pulse, a level 7 request will be generated, but ISR bit 7 will not be set. This "Default IR7" can be used to detect noise glitches. The service routine can check (from ISR.7), if it was activated by a real interrupt or a default.

Cascading

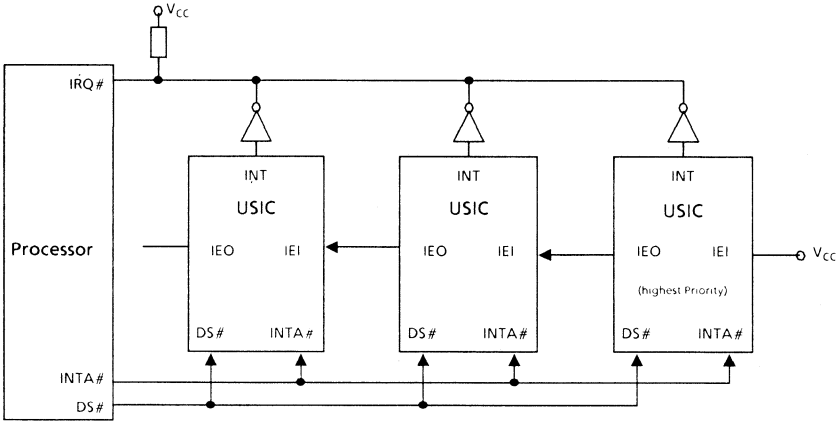
The USIC's interrupt control unit can be cascaded with other USIC ICUs, SAB 82C59As, etc. in three different modes:

- Slave Device with standard cascading (Intel bus mode)
  The USIC's ICU is controlled by the master device via the 3 cascade lines.
- Master Device with standard cascading (Intel bus mode)
  The USIC's ICU controls another interrupt controller via the 3 cascade lines. This device must be connected to the INTE input.
- Daisy chain cascading (Motorola bus mode)
  The USIC outputs its interrupt vector on DS# activation, if its IEI input is active. The USIC will deactivate its IEO output, if its IEI input is inactive, or if it has an interrupt pending (IEI active).

Standard Cascading



Daisy Chain Cascading



Absolute Maximum Ratings

Ambient temperature under bias	0 to +70°C
Storage temperature	−65 to +150°C
Supply Voltage [1]	−0.5 to +7 V
Input Voltage [1]	−1.0 to V_{CC} +0.5V
Output Voltage [1]	−0.5 to V_{CC} +0.5V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_C = 0 to 100°C; V_{CC} = +5V ± 5 %

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage (except XTAL2)	V_{IL}	−0.5	0.8	V	
XTAL2 input low voltage	V_{XIL}	−0.3	0.8	V	
Input high voltage (except XTAL2)	V_{IH}	2.0	V_{CC} + 0.5	V	
XTAL2 input high voltage	V_{XIH}	V_{CC} − 0.8	V_{CC} + 0.3	V	
Output low voltage	V_{OL}	−	0.4	V	I_{OH} = 2.5 mA
Output high voltage	V_{OH}	3.0 V_{CC}−0.4	− −	V V	I_{OH} = −2.5 mA I_{OH} = −100µA
Input load current	I_{IL}	−	±10	µA	$0V < V_{IN} < V_{CC}$
Output leakage current	I_{OFL}	−	±10	µA	$0V < V_{OUT} < V_{CC}$
Power supply current	I_{CC}	− −	60 30	mA mA	T_C = 25° T_C = 100°C

1) With respect to ground.

2) V_{CC} = 5.5 V, V_{IN} = V_{CC} or GND, outputs open, all clock inputs driven with 10MHz clocks.

Capacitance

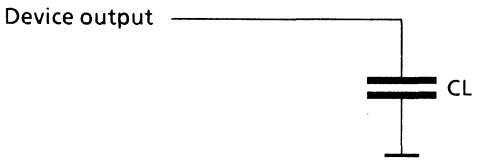
T_C = 25°C, V_{CC} = GND = 0V, f_c = 1MHz

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Capacitance of inputs	C_{IN}	−	5	pF	3)
Capacitance of I/O	C_{IO}	−	20	pF	3)
Capacitance of outputs	C_{OUT}	−	15	pF	3)

3) Unmeasured pins returned to ground.
Not 100% tested, guaranteed by design characterization.

AC Testing Waveforms

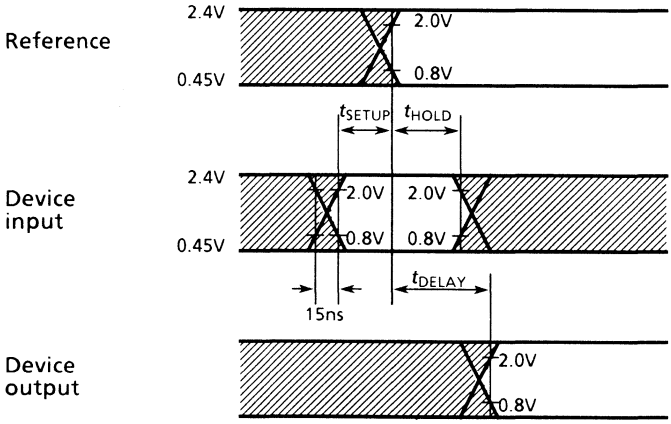
Test Loading on Outputs



CL = 150 pF on data bus lines.

CL = 80 pF on other output lines.

Setup, Hold and Delay Time Measurement-General



Note: Inputs are driven to 2.4 V for a logical "1", and are driven to 0.45 V for a logical "0".

Timing Arrangement

The AC characteristics are listed according to the several functional units of the USIC. Each section presents the timing parameters along with the waveform figures.

Note: AC timings are referenced to 0.8V and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noticed.

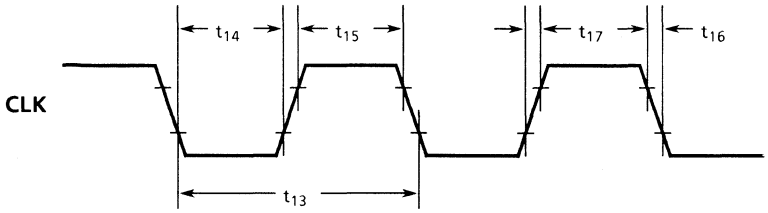
AC Characteristics SAB 82556 / Bus Interface

T_C = 0 to 100°C; V_{CC} = +5V ± 5 %

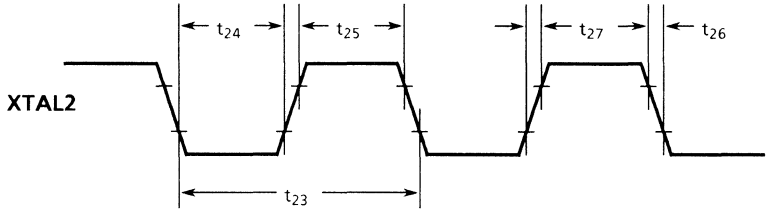
Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Address, CS#, DACK# stable before CMD active	t_1	20	-	ns	-
DACK# active hold after command active	t_2	20	-	ns	-
Command pulse width	t_3	80	-	ns	-
Command recovery for access to same register access to different registers	t_4	60 100	- -	ns ns	- -
Address hold time after command inactive	t_5	5	-	ns	-
Data setup time to WR# ↑, DS# ↑	t_6	60	-	ns	-
Data hold time after WR# ↑, DS# ↑	t_7	5	-	ns	-
Address to data valid	t_8	-	90	ns	-
RD# ↓, DS# ↓ to data valid	t_9	-	60	ns	-
Data hold after RD# ↑, DS# ↑	t_{10}	5	-	ns	-
RD#, DS# inactive to data bus float	t_{10A}	-	50	ns	-
R/W# setup before DS# ↓	t_{11}	10	-	ns	-
R/W# hold after DS# ↑	t_{12}	0	-	ns	-
System clock cycle time	t_{13}	50	-	ns	-
System clock low time	t_{14}	20	-	ns	-
System clock high time	t_{15}	20	-	ns	-
System clock fall time	t_{16}	-	15	ns	-
System clock rise time	t_{17}	-	15	ns	-
DRQR, DRQT deactivation after DACK# ↓	t_{18}	-	20	ns	-
DRQR deactivation after RD# ↓, DS# ↓, DRQT deactivation after WR# ↓, DS# ↓	t_{19}	-	35	ns	-
EODR# active after RD# ↓	t_{20}	-	50	ns	-
DRQR deactivation after RD# ↑, DS# ↑, DRQT deactivation after WR# ↑, DS# ↑	t_{21}	-	50	ns	-
DRQT deactivation after EODT# ↓	t_{22}	-	20	ns	-
Clock generator cycle time (Crystal or external clock)	t_{23}	58	1000	ns	-
X2 Input low time [1]	t_{24}	20	-	ns	-
X2 Input high time [1]	t_{25}	20	-	ns	-
X2 Input fall time	t_{26}	-	15	ns	-
X2 Input rise time	t_{27}	-	15	ns	-

1) Duty Cycle 45%:55% to 55%:45%

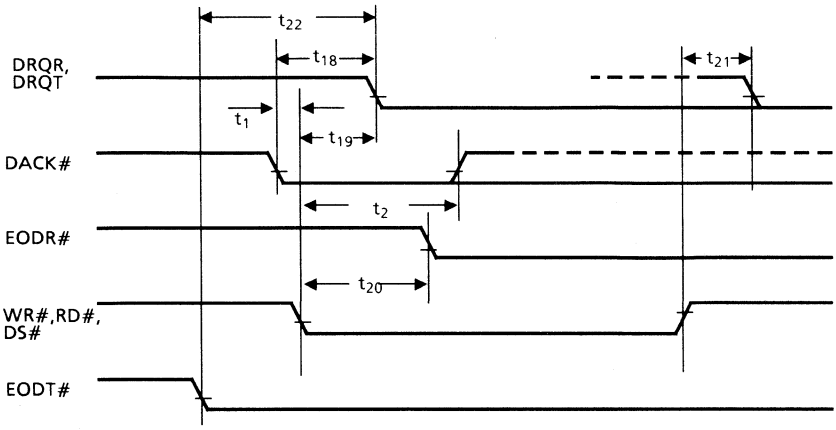
System Clock Signal



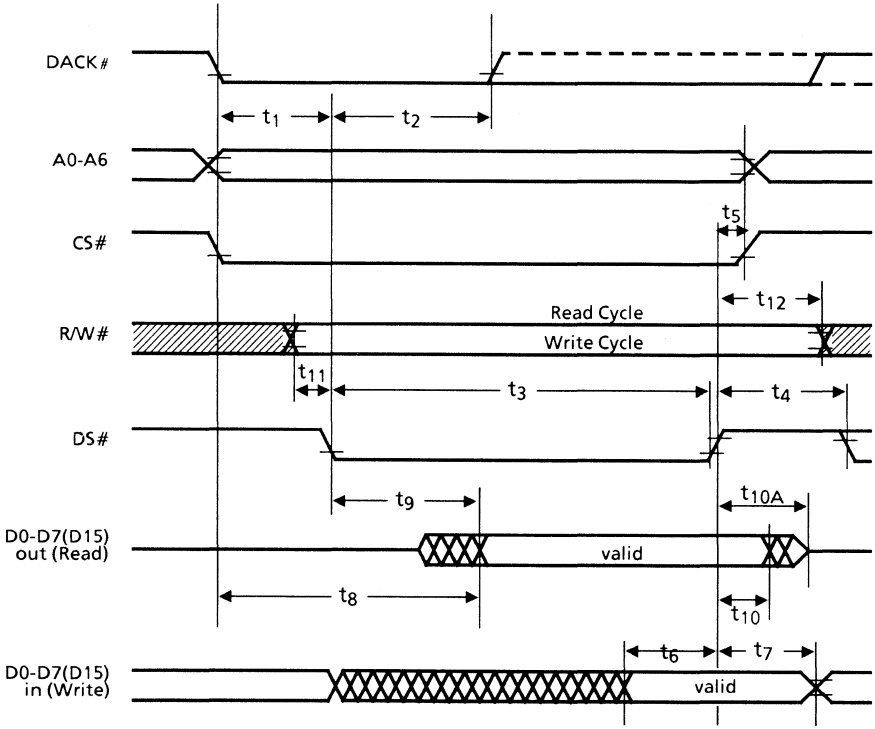
External Clock Signal



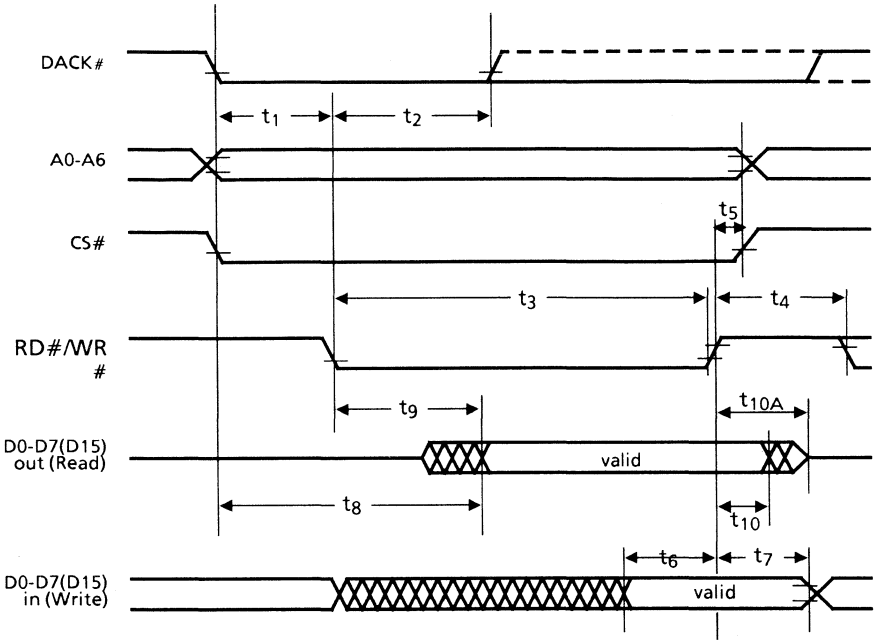
DMA Timing



Access Timing (Motorola Bus Mode)



Access Timing (Intel Bus Mode)

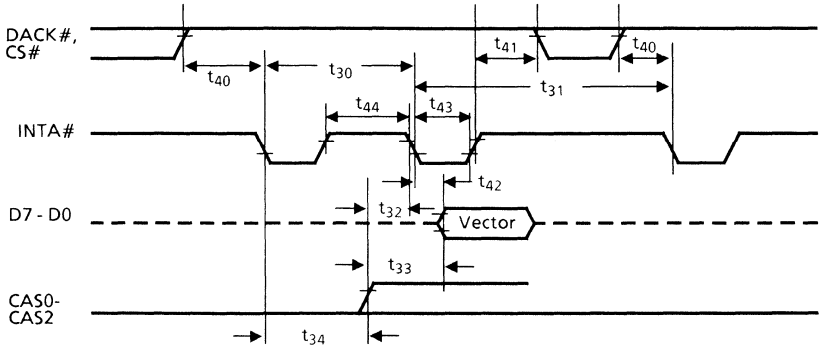


AC Characteristics SAB 82556 / Interrupt Control Unit

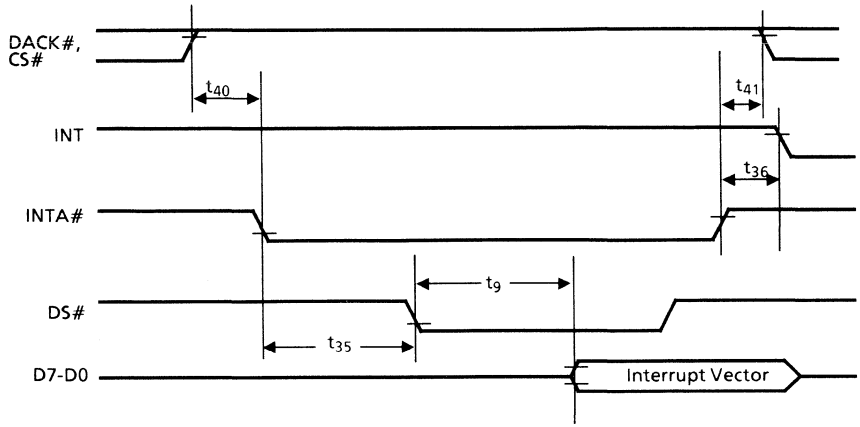
T_C = 0 to 100°C; V_{CC} = +5V ± 5 %

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
End of INTA# pulse to next INTA# pulse within INTA cycle	t_{30}	100	-	ns	-
End of INTA# pulse to next INTA# sequence	t_{31}	200	-	ns	-
Cascade address setup to 2nd INTA# pulse	t_{32}	40	-	ns	-
Cascade address valid to data valid	t_{33}	-	200	ns	-
Cascade address valid from INTA# ↓	t_{34}	-	200	ns	-
INTA# setup to DS# ↓	t_{35}	60	-	ns	-
INT inactive after INTA# ↑	t_{36}	-	20	ns	-
IEO valid after INTA# ↓ (if INT active)	t_{37}	-	20	ns	-
IEI to IEO delay	t_{38}	-	20	ns	-
IEI setup to DS# ↓	t_{39}	20	-	ns	-
DACK#, CS# inactive before INTA# active	t_{40}	30	-	ns	-
DACK#, CS# hold after INTA# inactive	t_{41}	30	-	ns	-
INTA# active to interrupt vector valid	t_{42}	-	60	ns	-
INTA# pulse width	t_{43}	160	-	ns	-
End of INTA# to next INTA# within an INTA# sequence only	t_{44}	160	-	ns	-

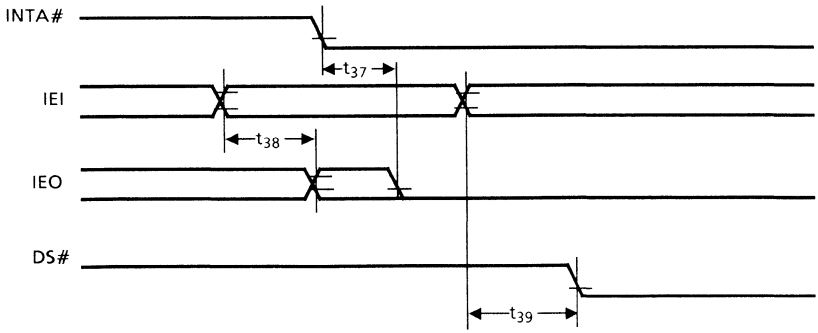
Two Cycle Interrupt Vector Output



Single Cycle Interrupt Vector Output



Daisy Chain Cascade Control Timing

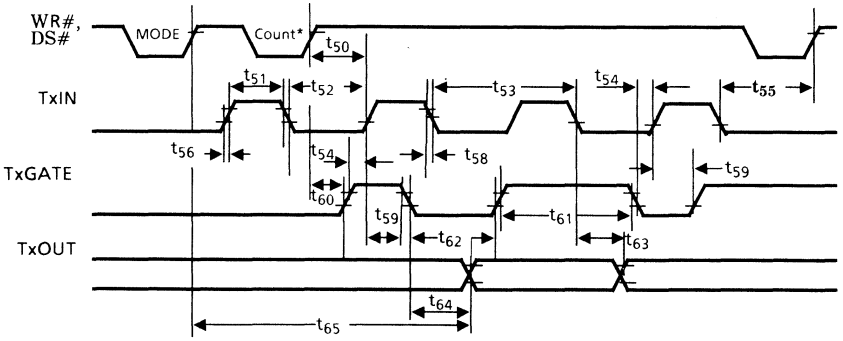


AC Characteristics SAB 82556 / Timer Unit

T_C = 0 to 100°C; V_{CC} = +5V ± 5 %

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Clock delay for loading	t_{50}	0	55	ns	-
High pulse width (clock)	t_{51}	30	-	ns	-
Low pulse width (clock)	t_{52}	30	-	ns	-
Clock period	t_{53}	100	-	ns	-
Gate setup to clock ↑	t_{54}	40	-	ns	-
Clock setup for count latch	t_{55}	-40	40	ns	-
Clock rise time	t_{56}	-	25	ns	-
Clock fall time	t_{58}	-	25	ns	-
Gate hold time after clock ↑	t_{59}	-	50	ns	-
Gate delay for sampling	t_{60}	-5	40	ns	-
Gate width high	t_{61}	50	-	ns	-
Gate width low	t_{62}	50	-	ns	-
Output delay from clock ↓	t_{63}	-	100	ns	-
Output delay from gate ↓	t_{64}		-	ns	-
Output delay from MODE writing	t_{65}	-	240	ns	-

Timer Unit Control Timing



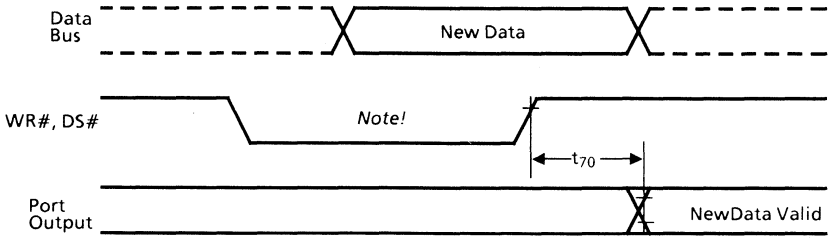
*: Last byte of count being written

AC Characteristics SAB 82556 / Parallel Interface Unit

T_C = 0 to 100°C; V_{CC} = +5V ± 5 %

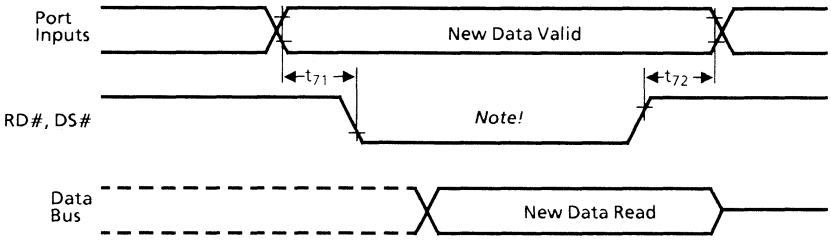
Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Port output valid after WR#,DS# ↑	t_{70}	-	200	ns	-
Port data set up before RD#, DS# ↓	t_{71}	20	-	ns	-
Port data hold after RD#, DS# ↑	t_{72}	0	-	ns	-
Port A pulse width for transition detection	t_{73}	20	-	ns	-
Port A interrupt request to INT ↑ delay	t_{74}	-	300	ns	-
WR#, DS# ↑ to output RDYB inactive	t_{75}	-	200	ns	-
Input ACK# ↓ to RDYB ↑	t_{76}	-	200	ns	-
ACK# input hold time to RDYB ↓	t_{77}	0	-	ns	-
ACK# pulse width	t_{78}	t_{76}	-	ns	-
Port data set up before STB# ↓	t_{79}	20	-	ns	-
Port data hold after STB# ↑	t_{80}	0	-	ns	-
STB# pulse width	t_{81}	t_{82}	-	ns	-
RDYB inactive output delay from STB# ↓	t_{82}	-	200	ns	-
RDYB active output delay from RD#, DS# ↑	t_{83}	-	200	ns	-

Basic Output to Ports



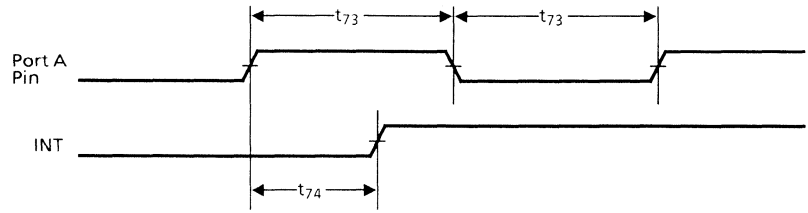
Note: R/W# assumed low for Motorola bus mode

Basic Input from Ports

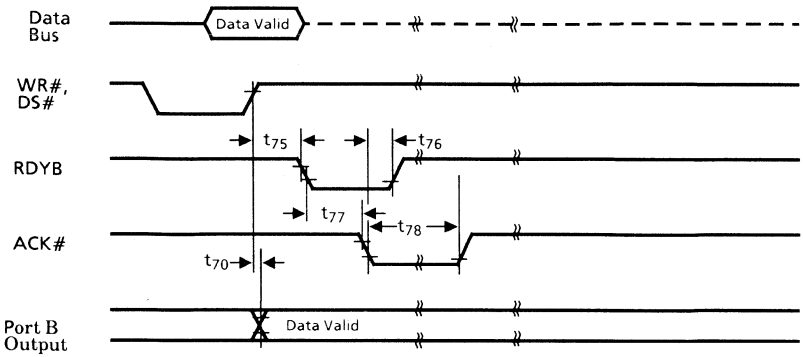


Note: R/W# assumed high for Motorola bus mode

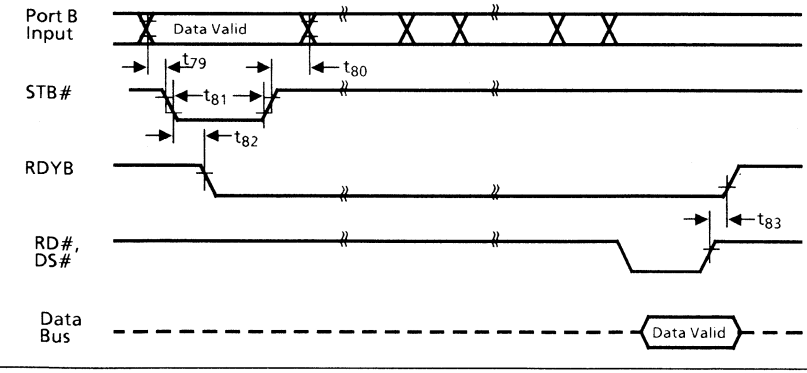
Port A Pulse Recognition and Interrupt Generation



Output on Port B in Handshake Mode



Input on Port B in Handshake Mode

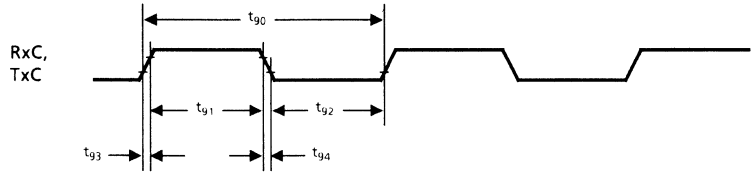


AC Characteristics SAB 82556 / Serial Interface Unit

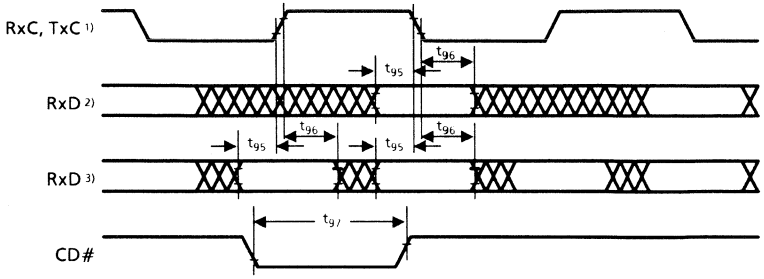
T_C = 0 to 100°C; V_{CC} = +5V ± 5 %

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Serial clock period	t_{90}	240	-	ns	-
Serial clock high time	t_{91}	90	-	ns	-
Serial clock low time	t_{92}	90	-	ns	-
Serial clock rise time	t_{93}	-	15	ns	-
Serial clock fall time	t_{94}	-	15	ns	-
Receive data setup time	t_{95}	0	-	ns	-
Receive data hold time	t_{96}	30	-	ns	-
CD# pulse width	t_{97}	100	-	ns	-
Transmit data delay time	t_{98}	-	50	ns	-
Collision data setup time	t_{99}	0	-	ns	-
Collision data hold time	t_{100}	30	-	ns	-
RTS# delay time	t_{101}	30	70	ns	-
CTS# pulse width	t_{102}	100	-	ns	
Receive strobe delay time	t_{103}	30	-	ns	-
Receive strobe setup time	t_{104}	30	-	ns	-
Receive strobe hold time	t_{105}	30	-	ns	-
Transmit strobe delay time	t_{106}	30	-	ns	-
Transmit strobe setup time	t_{107}	70	-	ns	-
Transmit strobe hold time	t_{108}	30	-	ns	-

External Clock Timing

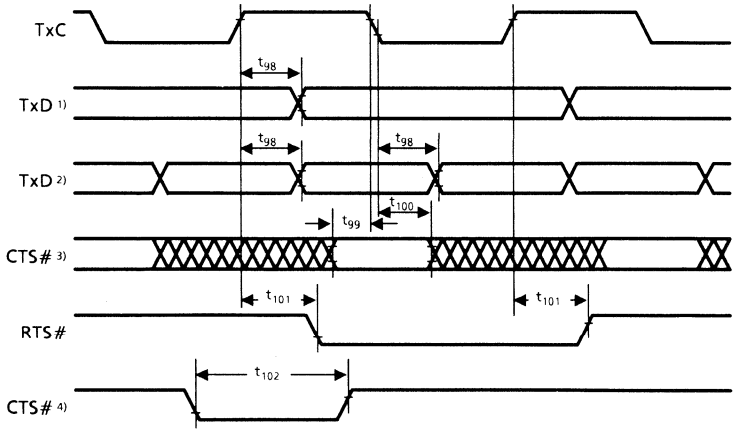


Receive Cycle Timing with External Clocking



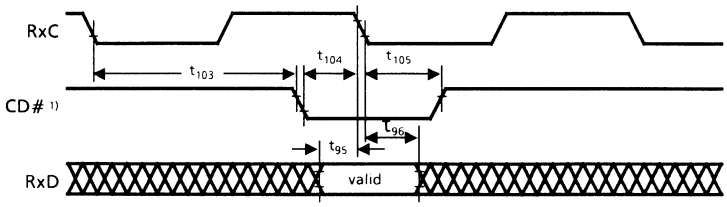
1): Whichever Supplies the Clock
2): NRZ, NRZI and Manchester Coding
3): FM0 and FM1 Coding

Transmit Cycle Timing with External Clocking



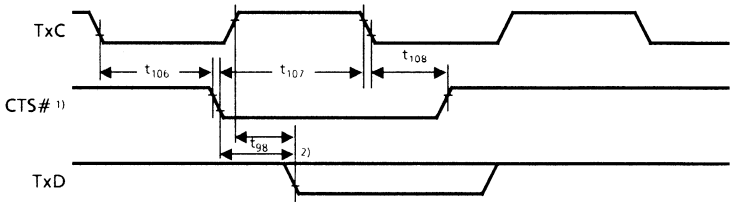
1): NRZ, NRZI Coding
2): FM0,FM1 and Manchester Coding
3: Collision Detection, Feedback Data Input
4: Non-Auto Mode, Auto Mode 1,2

Receive Strobe Timing (Automatic Receive Mode 0)



1): Strobe Input

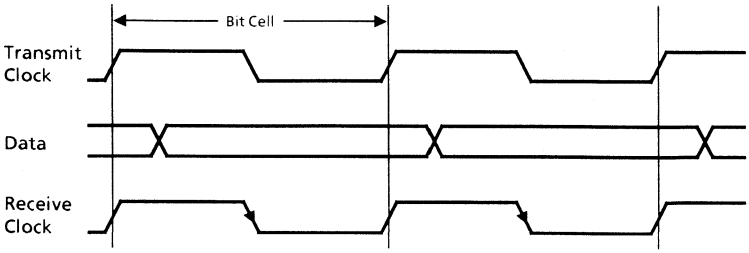
Transmit Strobe Timing (Automatic Transmit Mode 0)



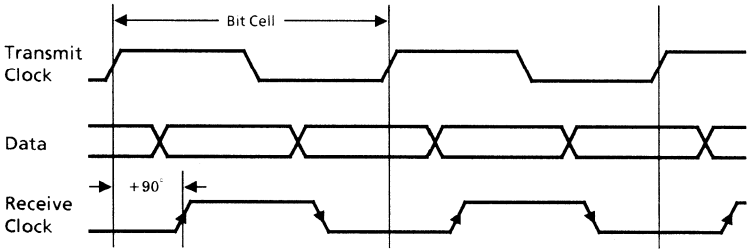
1): Strobe Input
2): Which ever comes last

Receive/Transmit Clock to Data Input/Output Correlation

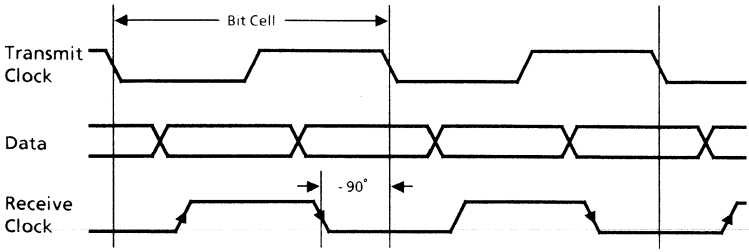
NRZ, NRZI Coding :



FM0, FM1 Coding :



Manchester Coding :



Note: Indication of active (= sampling) Receive Clock edges :

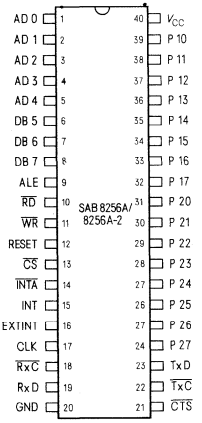
SIEMENS

Preliminary

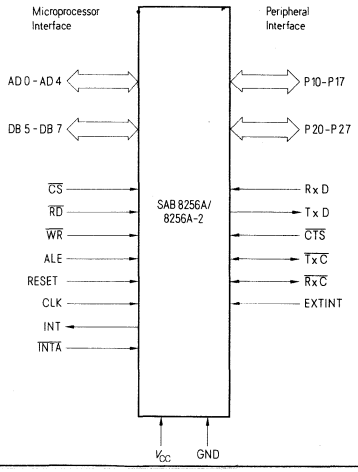
SAB 8256A, SAB 8256A-2 Programmable Multifunction UART (MUART)

- SAB 8256A is compatible with processors up to 3 MHz system clock (e. g. SAB 8085A, SAB 8048, SAB 8051).
  SAB 8256A-2 is compatible with processors up to 8 MHz system clock (e.g. SAB 8085A-2, SAB 8086 - minimum mode, SAB 80186).
- Full-duplex asynchronous serial interface with programmable 5–8 data bits, 0.75–2 stop bits, parity generation and checking.
- Internal baud rate generator programmable for 50–19, 200 Baud; 0–1 Megabaud possible with external baud rate clock.
- Interrupt controller with 8 priority levels; each level independently maskable, programmable for normal and fully nested operation with SAB 8085 and SAB 8086 processor families.
- Five programmable 8-bit counter/timers, internal or external clock, four are cascadable to two 16-bit counter/timers.
- Two 8-bit I/O ports, bit programmable for input/output, handshake mode supported.
- 40-pin dual-in-line plastic package (P-DIP-40)

Pin Configuration
P-DIP-40



Logic Symbol



SAB 8256A integrates four of the most often used peripheral functions in a microcomputer system into a 40-pin dual-in-line plastic package (P-DIP-40): serial interface, parallel interface, timer/counter and interrupt controller. It is primarily suited for systems like SAB 8048, SAB 8051, SAB 8085, SAB 8086, SAB 8088, SAB 80186 and SAB 80188 which have a multiplexed bus. With some additional circuitry, the SAB 8256A can also be used with other processors. All the functions of SAB 8256A are programmable by software, leading to a great flexibility in system design.

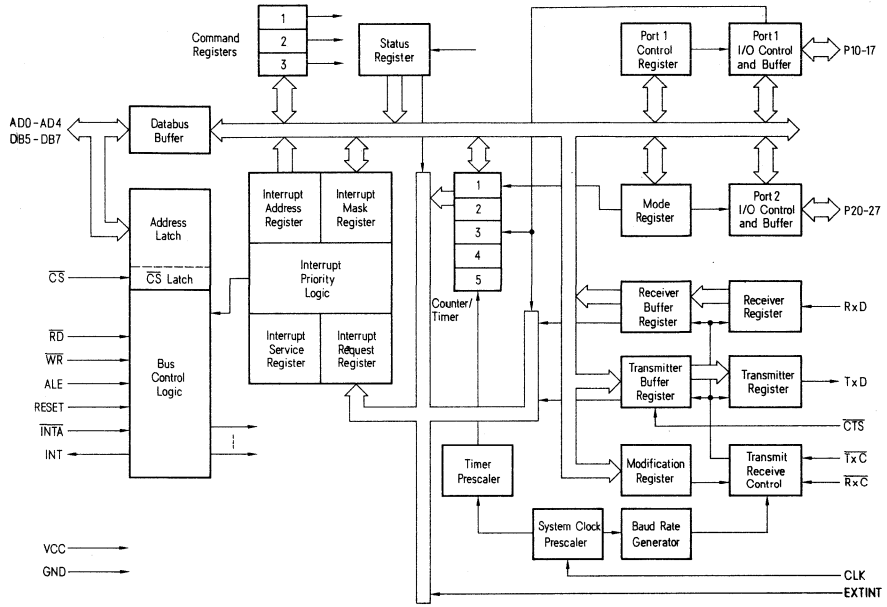
Pin Description and Functions

Symbol	Pin	Input (I) Output (O)	Functions
AD0–AD4, DB5–DB7	1–5 6–8	I/O	**Interface to Multiplexed Address/Data Bus** Bidirectional lines to 8 data bits and 5 least significant address bits which are latched internally on the falling edge of ALE.
ALE	9	I	**Adress Latch Enable** The five least significant address bits and $\overline{CS}$ are latched on the falling edge of ALE into an internal register.
$\overline{RD}$	10	I	**Read Control** The microprocessor reads data from the chip when this signal is low.
$\overline{WR}$	11	I	**Write Control** The microprocessor writes data into the chip with a low on this pin.
RESET	12	I	**Reset** A high on this pin forces the chip to its initial state. The chip remains in this state until control information is written into the chip.
$\overline{CS}$	13	I	**Chip Select** A low on this pin during ALE enables the bus interface of the chip. Neither read nor write operations are possible without this enable. The signal has no effect on the internal operation of the chip.
$\overline{INTA}$	14	I	**Interrupt Acknowledge** When this signal is low, the microprocessor informs the chip that an interrupt request is being serviced.
INT	15	O	**Interrupt Request** The chip demands interrupt service from the microprocessor with a high on this output.
EXTINT	16	I	**External Interrupt** An external source can request interrupt service through this input. The source can be either a peripheral or another SAB 8256A with its INT pin as the signal source. The input is level sensitive (high). The request must be held high until the processor acknowledges it.
CLK	17	I	**System Clock** Clock on this input is the reference clock for the timers, baud rate generator and various other functions.

Symbol	Pin	Input (I) Output (O)	Functions
$\overline{R \times C}$	18	I/O	**Receive Clock** If this pin is programmed as an output, it provides a low-to-high transition at the sampling point of each received data bit (excluding the framing bits). When programmed as an input, an externally generated receive clock must be connected to this pin. At DC, its frequency can range up to 1.024 MHz matching the receiver baud rate. The internal baud rate generator is disabled if this pin is used as input.
R×D	19	I	**Receive Data** Input for serial data, which is converted to parallel format while discarding the framing bits and then is made available for the processor.
$\overline{CTS}$	21	I	**Clear to Send** This input enables the serial transmitter. If 1, 1.5 or 2 stop bits are selected, $\overline{CTS}$ is level sensitive. As long as $\overline{CTS}$ is low, any character loaded into the transmitter buffer register will be transmitted serially. For continuous transmission, this input must be tied to low. A single negative going pulse causes the transmission of a single character previously loaded into the transmitter buffer register. If the transmitter buffer is empty, this pulse will be ignored. If this pulse occurs during the transmission of a character up to the time where 0.5 of the first (or the only) stop bit is sent out, it will be ignored. If it occurs afterwards, but before the end of the stop bits the next character will be transmitted immediately following the current one. If $\overline{CTS}$ is still high when the transmitter register is sending the last stop bit, the transmitter will enter its idle state until the next high-to-low transition on $\overline{CTS}$ occurs. If 0.75 stop bits is chosen, $\overline{CTS}$ input is edge sensitive. A negative edge on $\overline{CTS}$ results in the immediate transmission of the next character. The length of the stop bits is determined by the time interval between the beginning of the first stop bit and the next negative edge on $\overline{CTS}$. A high-to-low transition has no effect if the transmitter buffer is empty or if the time interval between the beginning of the stop bit and next negative edge is less than 0.75 bit. A high or a low level or a low-to-high transition has no effect on the transmitter for the 0.75 stop bit mode.
$\overline{T \times C}$	22	I/O	**Transmit Clock** The function of this pin can be programmed in 3 configurations. As an output it delivers the transmit clock corresponding to the baud rate. If programmed as an input, an external clock of 32 or 64 times the baud rate that is common to transmitter and receiver, or a 1× clock matching the baud rate which is used for the transmitter only, can be tied to this pin. The maximum frequency is 1.024 MHz. Thus, baud rates ranging from 0 to 16 Kbaud (64×) or from 0 to 32 Kbaud (32×) or from 0 to 1.024 Mbaud (1×) are possible. The internal baud rate generator is disabled if $\overline{T \times C}$ is selected as input.

Symbol	Pin	Input (I) Output (O)	Functions
T×D	23	O	**Transmit Data** Serial data output. The parallel data received from the processor and the framing bits added by the SAB 8256A are sent out serially over this output when the transmitter is enabled by the $\overline{CTS}$ signal.
P27–P20	24–31	I/O	**Parallel I/O Port 2** The eight general purpose I/O pins of parallel port 2 can be configured in sets of four pins (nibbles) as inputs or outputs or 8 bit I/O with handshake (control signals at port 1). In the nibble mode the output signals are latched whereas the input signals are not. In the handshake mode both inputs and outputs are latched.
P17–P10	32–39	I/O	**Parallel I/O Port 1** Each one of these 8 pins can be programmed as input or output. Alternatively these pins can serve as control pins which extends considerably the functional spectrum of the chip. The pins are assigned to special functions implicitly by programming. All outputs are latched whereas inputs are not.
V_{CC}	40	–	**Power Supply** (+5 V)
GND	20	–	**Ground** (0 V)

Block Diagram



Functional Description

Bus Interface

The bus interface unit, consisting of bus drivers, address latches and bus control logic, interfaces the SAB 8256A to the data, address and control buses of a microcomputer system. The chip is selected by the $\overline{CS}$ signal, which is latched into the chip along with address lines AD0–AD4 by the ALE signal. $\overline{WR}$ and $\overline{RD}$ signals are used to write data into and read data from SAB 8256A.
Signals INT und $\overline{INTA}$ are used to handle interrupt protocol with the processor.
RESET signal resets the chip to its initial state.

Counter/Timers

Five programmable counter/timers can be used in several modes. Each can be used as an 8-bit timer while two can alternatively serve as counters. Counter/timer 2 and timer 4 as well as counter/timers and timer 5 can be cascaded to 16-bit counter/timers. All counter/timers function as binary down-counters with a programmable initial value and generate an interrupt request on their 1 to 0 transition. An internal register is provided for the initial count of timer 5 and with an external trigger pulse it is possible to reload the initial value into timer 5 (also for cascaded counter/timer 3 and timer 5).
A common clock source with a frequency of either 1 KHz or 16 KHz is available for the timers. In addition, for counters 2, 3 and the cascaded counters, an external clock source can be provided through two pins of part 1.

Asynchronous Serial Interface

For double buffered full-duplex operations both transmitter and receiver have two registers. The received data (5 to 8 data bits, programmable) is assembled to parallel format in the receiver register, the framing bits (Start, Stop, and Parity) are stripped off and stored into the receiver buffer register. The data to be transmitted is first loaded into the transmitter buffer register and then sent out through the transmitter register.
Controlling the $\overline{CTS}$ signal, single characters on character strings can be transmitted. Baud rate clock (50 to 19,200 Baud) is generated on the chip which is common to both the receiver and the transmitter. It is also possible to provide an external baud rate clock (common or separate for receiver and transmitter) to provide baud rates from 0 to 1.024 Mbaud.

Parallel Interface

The parallel interface consists of two 8-bit ports programmable as inputs or outputs. Each pin of port 1 can be programmed separately as an input or an output. They can also be used as control pins. Port 2 can be programmed as input or output in two 4-bit groups. Port 2 can also be used as an 8-bit input or output port with handshake signals.

Assignment of Control Signals to Port 1

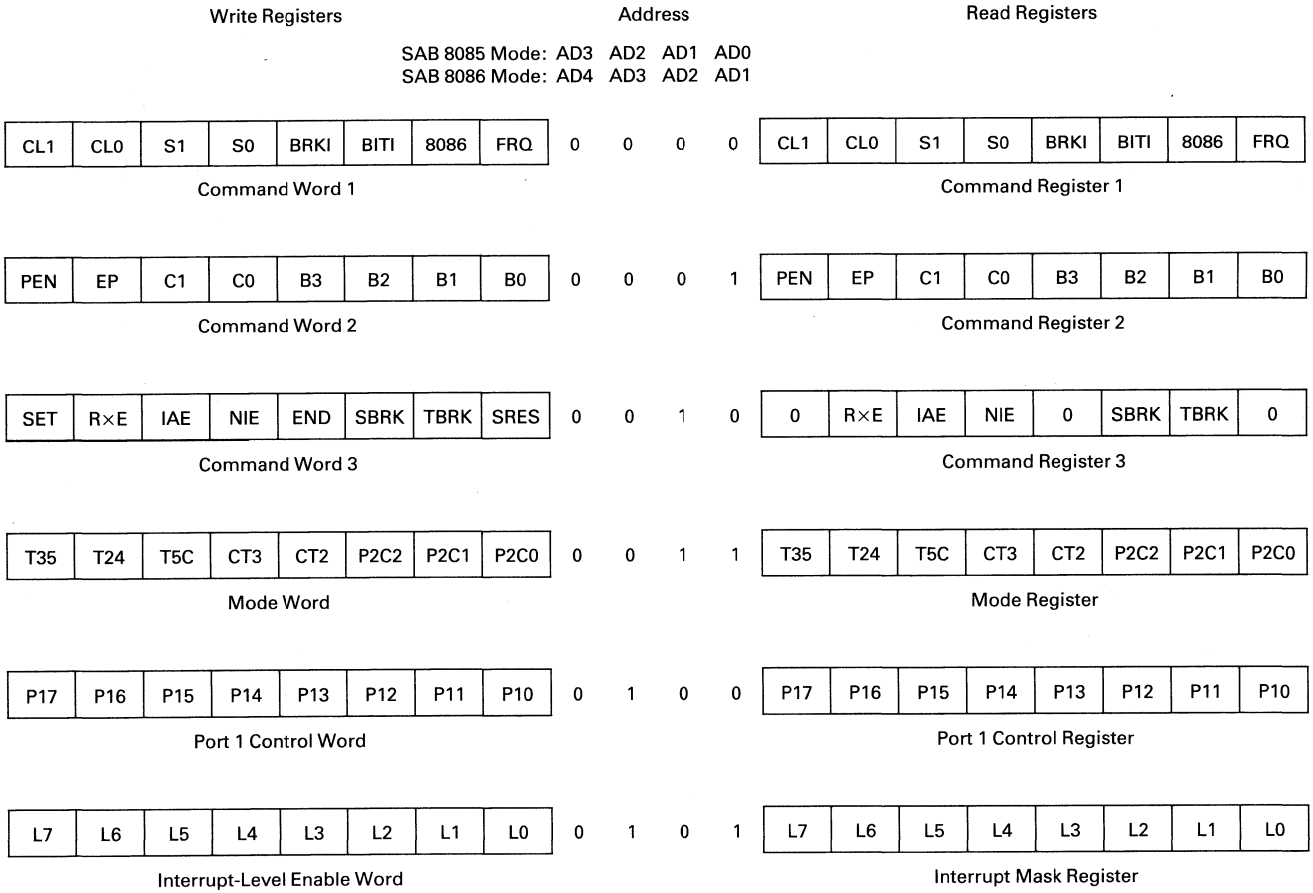
Pins Port 1	P17	P16	P15	P14	P13	P12	P11	P10
Control Function	External interrupt input	Break-In detect input	Trigger input for timer 5 (cascaded counter/ timer 3+5)	Output of the clock of the internal baudrate generator	Clock input for counter 3	Clock input for counter 2	Handshake Control Signals for Port 2	

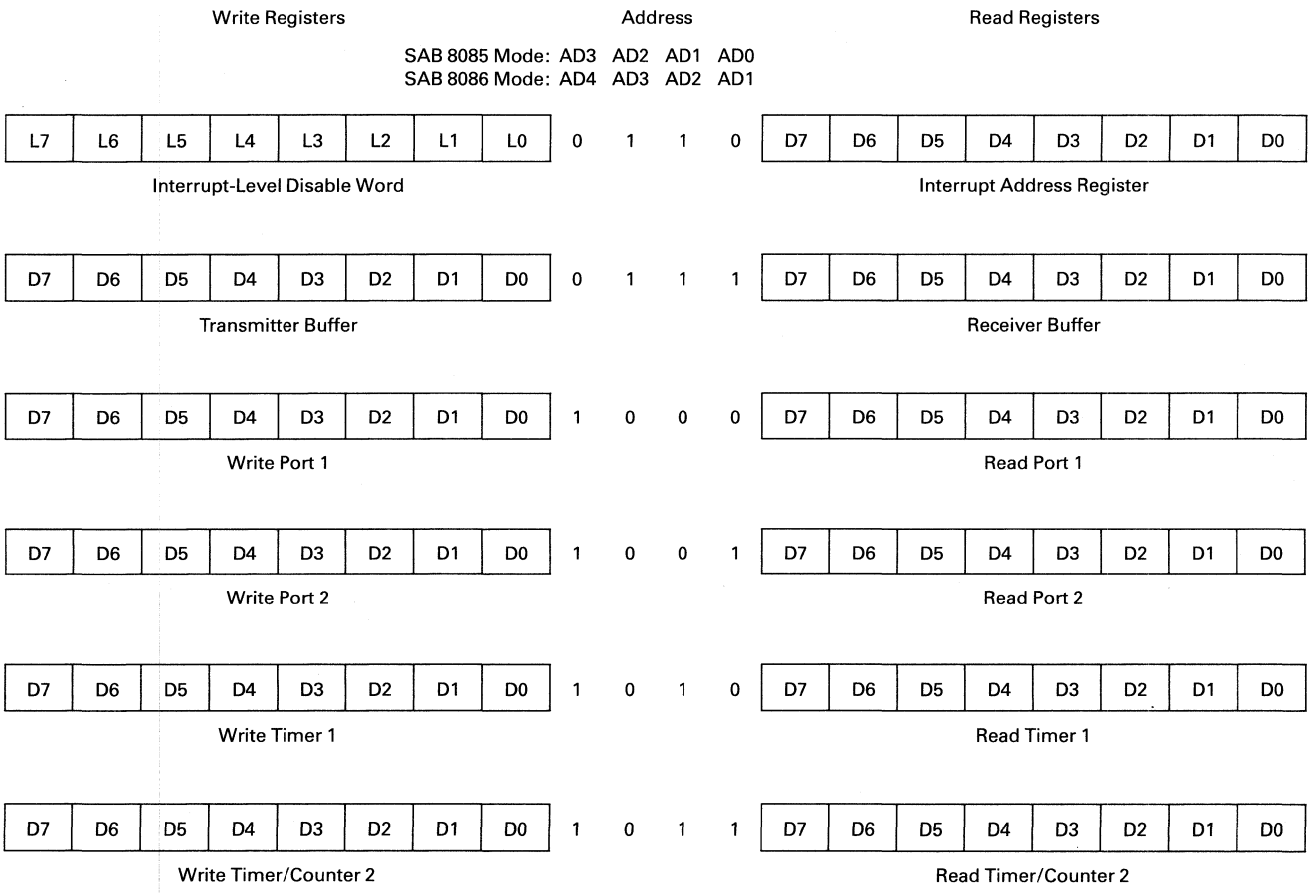
Interrupt Controller

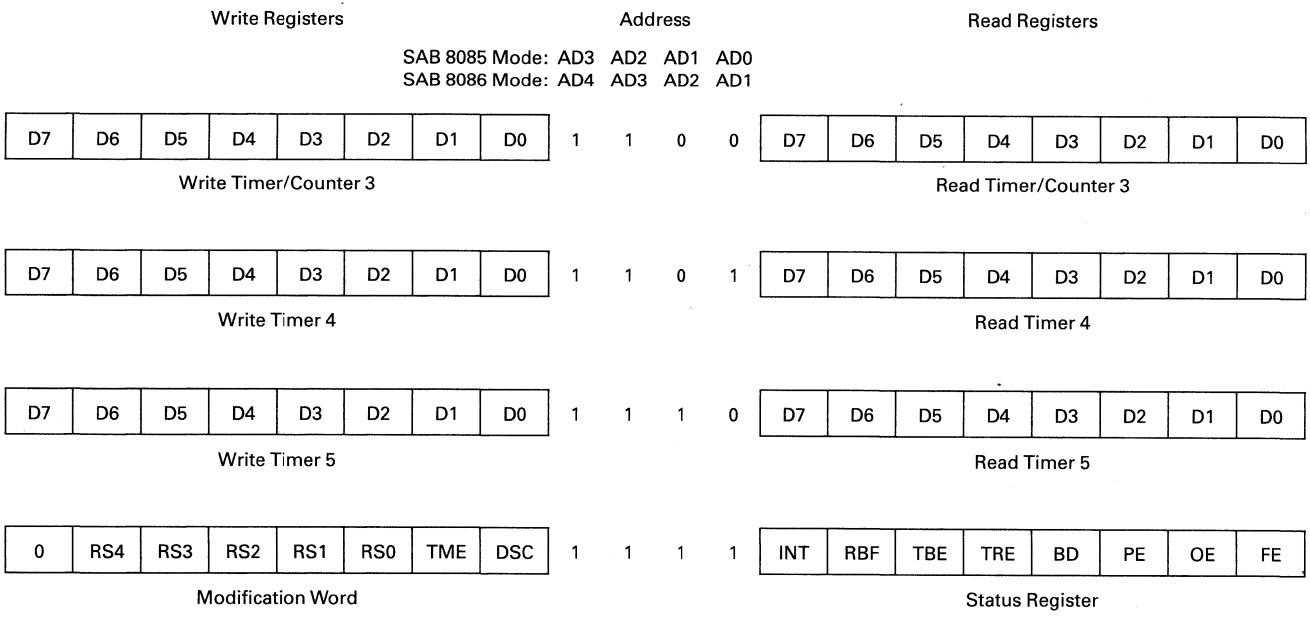
The interrupt controller manages 12 interrupt sources (10 internal and 2 external) on 8 priority levels. Normal (every interrupt request immediately recognized) and "fully nested" (recognition based on priority) mode are supported.
The interrupt controller supports various methods of connecting SAB 8256A to the processor. Firstly, the true interrupt mode (using INT and $\overline{\text{INTA}}$ signals for interrupt protocol), secondly, a combination of polling and interrupt (using INT and interrupt address registers). The interrupt protocols of SAB 8048, SAB 8085A, SAB 8086, SAB 8088, SAB 80186 and SAB 80188 are directly supported.

Programming the SAB 8256A

The functional characteristics of SAB 8256A can be programmed by writing appropriate control information into it. It is specially designed for ease of programming. Thus, it is possible to alter individual bits in certain registers like e.g. the Interrupt Mask Register and Command Register 3. All functions of SAB 8256A can be easily used because each unit (e.g. counter/timer, serial interface) has specially assigned registers which can be directly read or written.

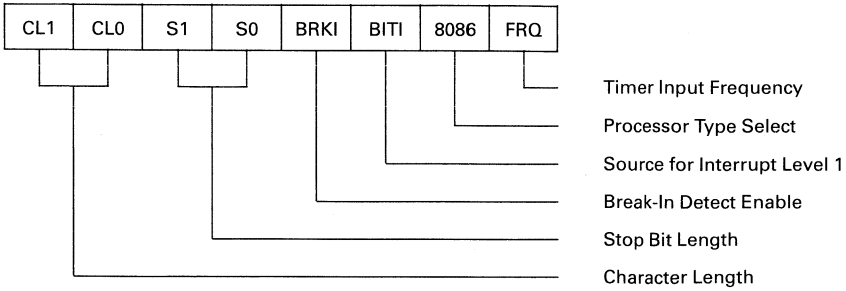

Write Registers
Address
Read Registers
SAB 8085 Mode: AD3 AD2 AD1 AD0
SAB 8086 Mode: AD4 AD3 AD2 AD1
CL1 CL0 S1 S0 BRKI BITI 8086 FRQ 0 0 0 0 CL1 CL0 S1 S0 BRKI BITI 8086 FRQ
Command Word 1
Command Register 1
PEN EP C1 C0 B3 B2 B1 B0 0 0 0 1 PEN EP C1 C0 B3 B2 B1 B0
Command Word 2
Command Register 2
SET R×E IAE NIE END SBRK TBRK SRES 0 0 1 0 0 R×E IAE NIE 0 SBRK TBRK 0
Command Word 3
Command Register 3
T35 T24 T5C CT3 CT2 P2C2 P2C1 P2C0 0 0 1 1 T35 T24 T5C CT3 CT2 P2C2 P2C1 P2C0
Mode Word
Mode Register
P17 P16 P15 P14 P13 P12 P11 P10 0 1 0 0 P17 P16 P15 P14 P13 P12 P11 P10
Port 1 Control Word
Port 1 Control Register
L7 L6 L5 L4 L3 L2 L1 L0 0 1 0 1 L7 L6 L5 L4 L3 L2 L1 L0
Interrupt-Level Enable Word
Interrupt Mask Register


Write Registers
Address
Read Registers
SAB 8085 Mode: AD3 AD2 AD1 AD0
SAB 8086 Mode: AD4 AD3 AD2 AD1
L7 L6 L5 L4 L3 L2 L1 L0
0 1 1 0
D7 D6 D5 D4 D3 D2 D1 D0
Interrupt-Level Disable Word
Interrupt Address Register
D7 D6 D5 D4 D3 D2 D1 D0
0 1 1 1
D7 D6 D5 D4 D3 D2 D1 D0
Transmitter Buffer
Receiver Buffer
D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0
D7 D6 D5 D4 D3 D2 D1 D0
Write Port 1
Read Port 1
D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 1
D7 D6 D5 D4 D3 D2 D1 D0
Write Port 2
Read Port 2
D7 D6 D5 D4 D3 D2 D1 D0
1 0 1 0
D7 D6 D5 D4 D3 D2 D1 D0
Write Timer 1
Read Timer 1
D7 D6 D5 D4 D3 D2 D1 D0
1 0 1 1
D7 D6 D5 D4 D3 D2 D1 D0
Write Timer/Counter 2
Read Timer/Counter 2

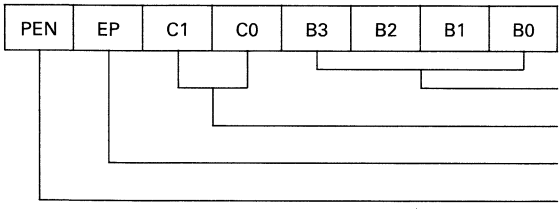

Write Registers
Address
Read Registers
SAB 8085 Mode: AD3 AD2 AD1 AD0
SAB 8086 Mode: AD4 AD3 AD2 AD1
D7 D6 D5 D4 D3 D2 D1 D0
1 1 0 0
Write Timer/Counter 3
Read Timer/Counter 3
1 1 0 1
Write Timer 4
Read Timer 4
1 1 1 0
Write Timer 5
Read Timer 5
0 RS4 RS3 RS2 RS1 RS0 TME DSC
1 1 1 1
Modification Word
INT RBF TBE TRE BD PE OE FE
Status Register

Programming

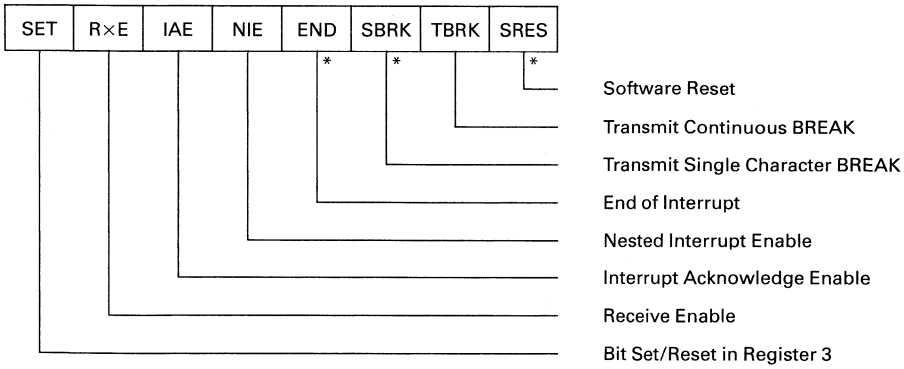
Command Word 1



Command Word 2

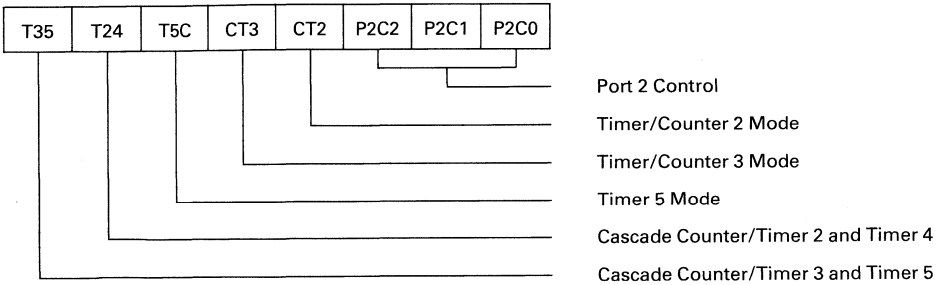


Command Word 3

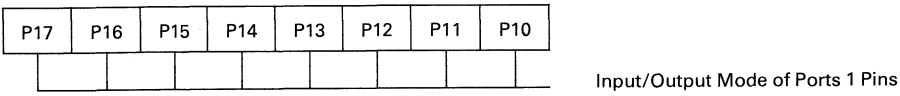


*) These bits can only be set, they are reset at the end of the operation.

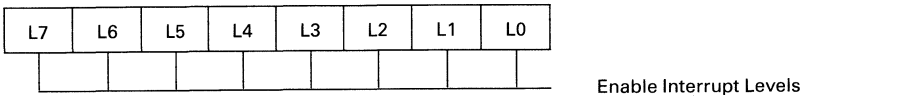
Mode Word



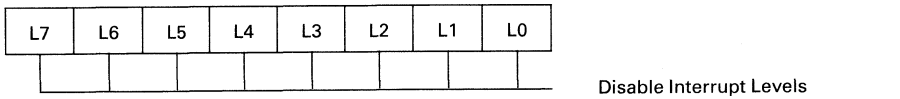
Port 1 Control World



Interrupt-Level Enable Word

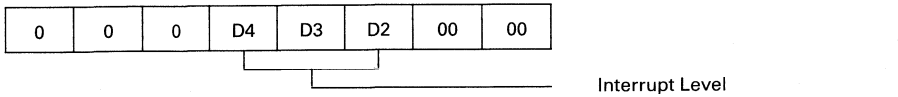


Interrupt-Level Disable Word



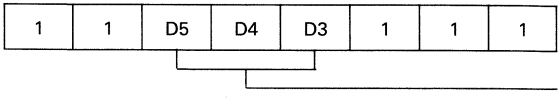
Determination of Interrupt Level

Reading the Interrupt Address Register

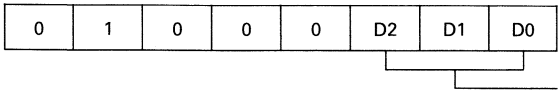


Response to $\overline{\text{INTA}}$

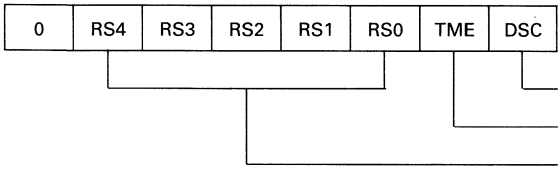
SAB 8085-Mode (RST-instruction in response to $\overline{\text{INTA}}$)



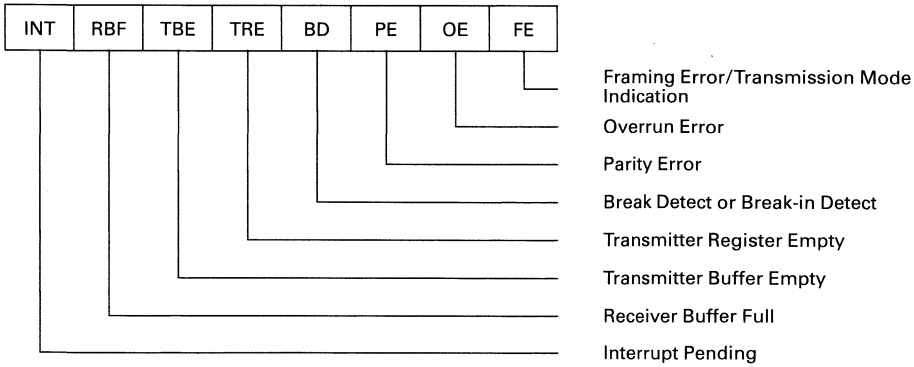
SAB 8086-Mode (Interrupt Vector in response to second $\overline{\text{INTA}}$)



Modification Word



Status Register



Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to +7 V
Power dissipation	1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V
(if not otherwise specified)

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage	V_{IL}	−0.5	0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC}+0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 2.5 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = −400 µA
Input leakage	I_{IL}	–	±10	µA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	–	±10	µA	V_{OUT} = 0 V to V_{CC}
V_{CC} supply current	I_{CC}	–	190	mA	–

Capacitance [1]

Parameter	Symbol	Limit value (max.)	Unit	Test conditions
Input capacitance	C_{IN}	10	pF	f_C = 1 MHz Unmeasured pins returned to GND
I/O capacitance	$C_{I/O}$	20	pF	

[1] This parameter is periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ± 5%; V_{SS} = 0 V

Test Conditions

Capacitive load C_L = 150 pF

The timings are with respect to the following levels:

H-level: 2.0 V
L-level: 0.8 V
Rise and fall times: 20 ns

The timings are valid for an internal clock of 1.024 MHz.

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 8256A		SAB 8256A-2			
		min.	max.	min.	max.		
$\overline{STB}\downarrow$ to $\overline{IBF}\downarrow$	t_{AC}	–	300	–	300	ns	–
$\overline{ACK}$ pulse width	t_{ACK}	t_{ADP}	–	t_{ADP}	–	–	–
Address stable to data valid	t_{AD}	–	400	–	230	ns	–
$\overline{ACK}\uparrow$ to $\overline{OBF}\downarrow$	t_{ADP}	–	300	–	300	ns	–
$\overline{OBF}\downarrow$ to $\overline{ACK}\downarrow$	t_{AED}	0	–	0	–	ns	–
$\overline{ACK}\uparrow$ to INT $\uparrow$	t_{AI}	–	1.5 t_{CY}	–	1.5 t_{CY}	–	–
Address stable to ALE $\downarrow$	t_{AL}	50	–	30	–	ns	–
$\overline{RD}$ and $\overline{WR}$ pulse widths	t_{CC}	300	–	200	–	ns	–
$\overline{RD}\uparrow$ or $\overline{WR}\uparrow$ to next ALE $\uparrow$	t_{CL}	50	–	25	–	ns	–
Counter input cycle time (P12, P13,)	t_{CPI}	2.2	–	2.2	–	µs	–
$\overline{CS}$ stable to ALE $\downarrow$	t_{CSL}	60	–	10	–	ns	–
$\overline{CTS}$ pulse width for single character transmission	t_{CTS}	[1])	–	[1])	–	–	–
System clock period	t_{CY}	300	–	195	–	ns	–
$\overline{STB}\uparrow$ to INT $\uparrow$	t_{DEI}	–	1.5 t_{CY}	–	1.5 t_{CY}	–	–
EXTINT $\uparrow$ to INT $\uparrow$	t_{DEX}	–	200	–	200	ns	–
$\overline{STB}\uparrow$ to P2 data stable	t_{DH}	10	–	10	–	ns	–
Interrupt request on P17 to INT $\uparrow$	t_{DPI}	–	1.5 t_{CY}	–	1.5 t_{CY}	–	–
P2 data stable before $\overline{STB}\downarrow$	t_{DSI}	10	–	10	–	ns	–
$\overline{T\times C}\downarrow$ to T×D data valid	t_{DTX}	–	300	–	300	ns	–
Data valid before $\overline{WR}\uparrow$	t_{DW}	250	–	150	–	ns	–
EXTINT $\downarrow$ after $\overline{INTA}\uparrow$ or $\overline{RD}\uparrow$	t_{HEA}	30	–	30	–	ns	–
INT $\downarrow$ after $\overline{INTA}\uparrow$ or $\overline{RD}\uparrow$	t_{HIA}	–	300	–	300	ns	–
$\overline{CS}$ and address valid after ALE $\downarrow$	t_{LA}	50	–	20	–	ns	–
ALE $\downarrow$ to $\overline{RD}\downarrow$ or $\overline{WR}\downarrow$	t_{LC}	60	–	20	–	ns	–
ALE pulse width	t_{LL}	100	–	50	–	ns	–

Notes see next page.

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 8256A		SAB 8256A-2			
		min.	max.	min.	max.		
Pulse width of interrupt request on P17	t_{PI}	1.1	–	1.1	–	µs	–
Counter 5 load (P15↓) before next clock pulse on P13 ↑	t_{PP}	1.1	–	1.1	–	µs	–
P1, P2 data stable before $\overline{RD}$ ↓	t_{PR}	300	–	300	–	ns	–
Data valid after $\overline{RD}$ ↓	t_{RD}	–	200	–	150	ns	–
$\overline{RD}$ ↓ to data drivers active	t_{RDE}	10	100	10	50	ns	–
Data bus float after $\overline{RD}$ ↑	t_{RDF}	10	100	10	50	ns	–
RESET pulse width	t_{RES}	300	–	300	–	ns	–
$\overline{RD}$ ↑ to $\overline{IBF}$ ↑	t_{RI}	–	300	–	300	ns	–
P1, P2 data hold after $\overline{RD}$ ↑	t_{RP}	50	–	50	–	ns	–
Data bit start to $\overline{R \times C}$ ↓	t_{RRD}	300	[2]	150	[2]	ns	[3]
$\overline{RD}$ ↑ or $\overline{WR}$ ↑ to next $\overline{RD}$ ↓ or $\overline{WR}$ ↓	t_{RV}	300	–	150	–	ns	$\overline{CS}$=low
Serial clock period (32×, 64×)	t_{SCY}	975	–	975	–	ns	–
Serial clock high (32×, 64×)	t_{SPD}	350	–	350	–	ns	–
Serial clock low (32×, 64×)	t_{SPW}	350	–	350	–	ns	–
Strobe pulse width	t_{STB}	t_{AC}	–	t_{AC}	–	–	–
Serial clock period (1×)	t_{TCY}	975	–	975	–	ns	–
Serial clock high (1×)	t_{TPD}	350	–	350	–	ns	–
Load pulse for counter 5 (P15)-high	t_{TIH}	1.1	–	1.1	–	µs	–
Load pulse for counter 5 (P15)-low	t_{TIL}	1.1	–	1.1	–	µs	–
Counter input ↑ (P12, P13) to INT ↑ at terminal count	t_{TPI}	–	2.5	–	2.5	µs	–
Serial clock low (1)	t_{TPW}	350	–	350	–	ns	–
Time between 2 read cycles onto the same counter/timer	t_{TRV}	1.1	–	1.1	–	µs	–
Data hold after $\overline{WR}$ ↑	t_{WD}	40	–	30	–	ns	–
P1, P2 data valid after $\overline{WR}$ ↑	t_{WP}	–	300	–	300	ns	–
Count clock (P12, P13) high	t_{WPH}	1.1	–	1.1	–	µs	–
Count clock (P12, P13) low	t_{WPL}	1.1	–	1.1	–	µs	–
$\overline{OBF}$ ↑ after $\overline{WR}$ ↓	t_{WPO}	–	300	–	300	ns	–
Clock fall time	t_f	–	30	–	30	ns	–
Clock high	$t_{\Phi H}$	105	–	65	–	ns	–
Clock low	$t_{\Phi L}$	105	–	65	–	ns	–
Clock rise time	t_r	–	30	–	30	ns	–

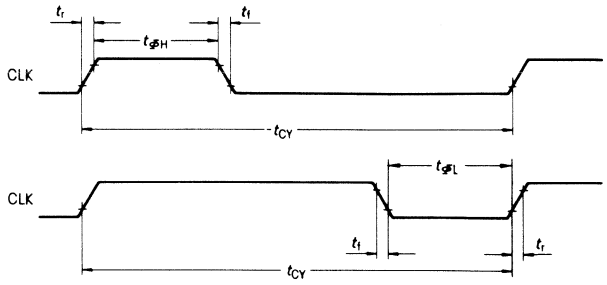
[1]) 1/32 bit length with transmitter clock with a baud rate factor of 32 or 64. 100 ns when baud rate factor = 1

[2]) 300 ns + (1/32 bit length)

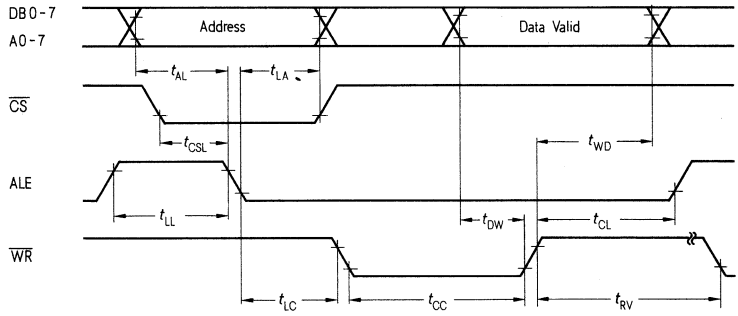
[3]) Sampling time at bit center

Waveforms

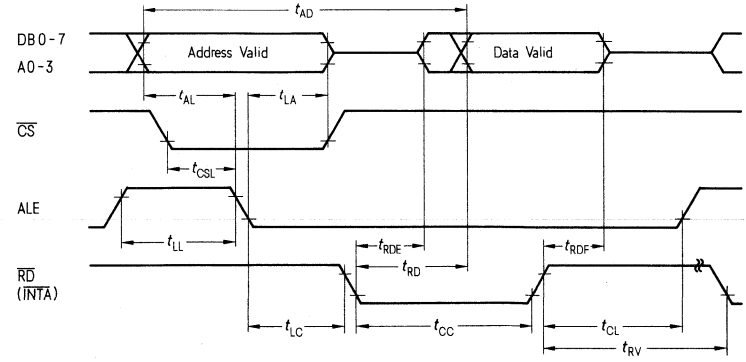
System Clock



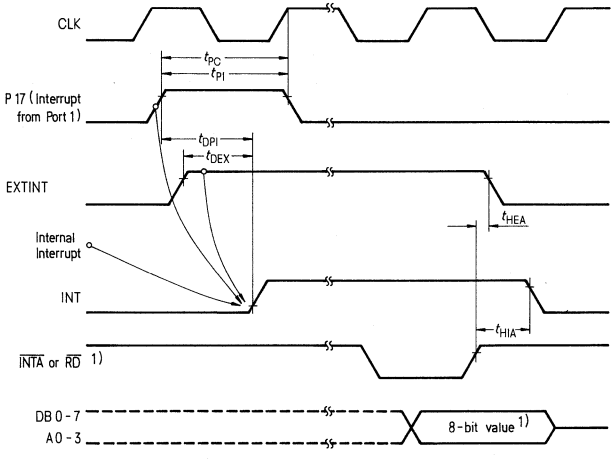
Write Cycle (Processor → SAB 8256A)



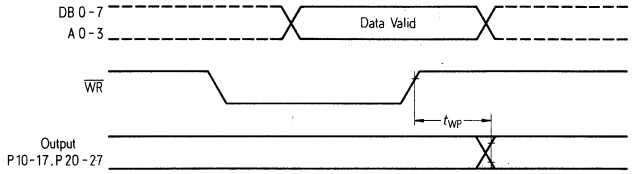
Read Cycle (SAB 8256A → Processor)



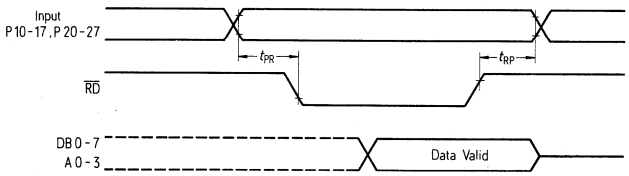
Interrupt Timings



Basic Output from Port 1 and Port 2

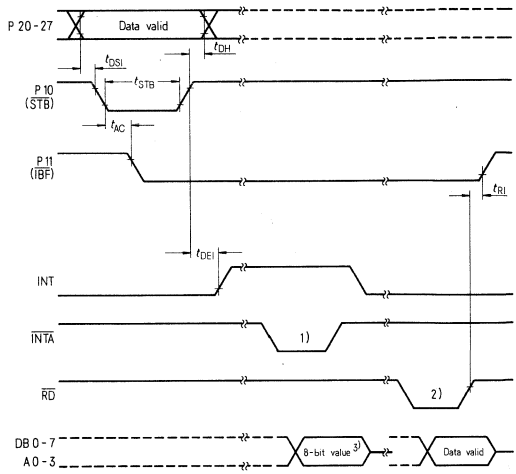


Basic Input from Port 1 and Port 2

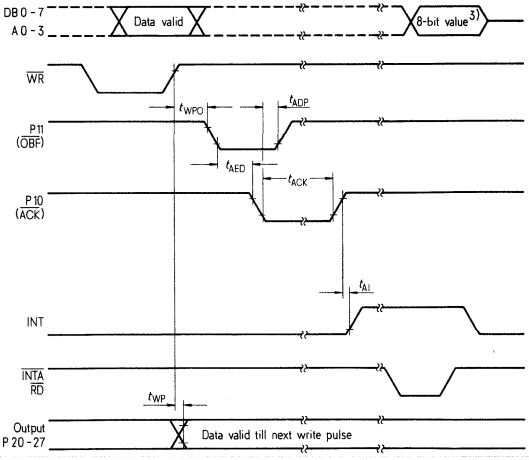


1) If INTA is enabled, RST instruction is output on INTA (SAB 8085 mode) or interrupt vector is output on second INTA (SAB 8086 mode) otherwise, interrupt address is output on a read address register operation.

Input from Port 2 in Handshake Mode
(Control Signals from Port 1)

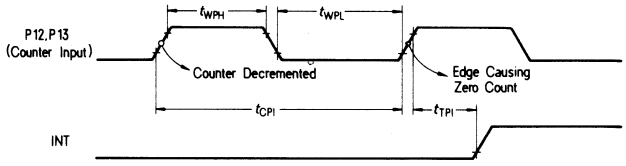


Output from Port 2 in Handshake Mode
(Control Signals from Port 1)

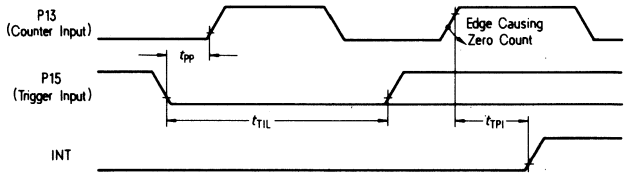


1) Instead of $\overline{\text{INTA}}$, $\overline{\text{RD}}$ can serve as interrupt acknowledge (reading the interrupt address register).
2) Read from channel 2.
3) If $\overline{\text{INTA}}$ is enabled, RST instruction is output on $\overline{\text{INTA}}$ (SAB 8085 mode) or interrupt vector is output on second $\overline{\text{INTA}}$ (8086 mode). Otherwise, interrupt address is output on a read address register operation.

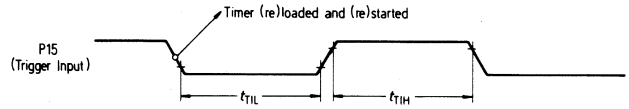
Count Pulse Timings and Zero-Crossing of Counter



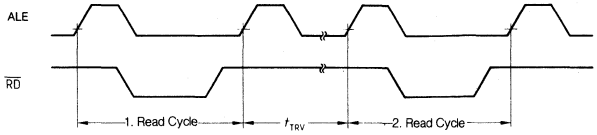
Loading Timer 5 (or Cascaded Counter/Timer 3 and 5) and Zero-Crossing of Counters (Cascaded Counter/Timer 3 and 5)



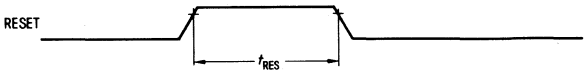
Trigger Pulse for Timer 5 (Cascaded Event Counter/Timer 3 and 5)



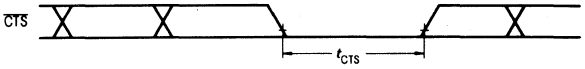
Reading Event Counters/Timers



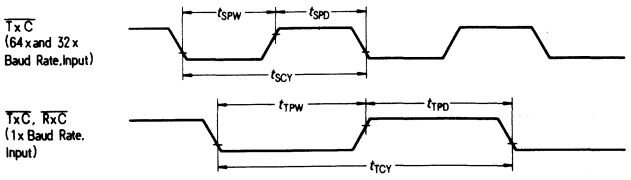
Reset Timing



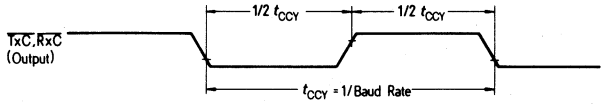
CTS for Single Character Transmission



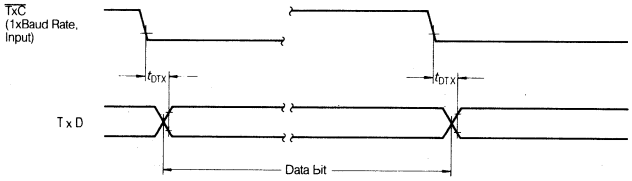
External Baud Rate Clock for Serial Interface



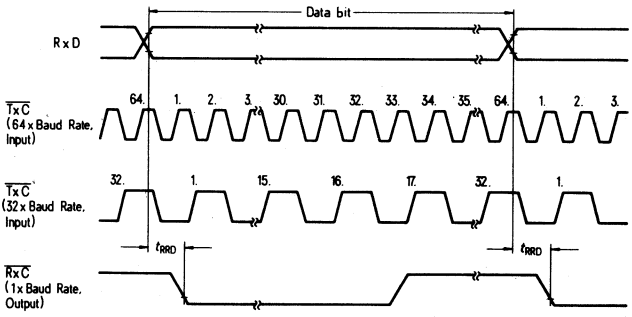
Transmitter and Receiver Clock from Internal Clock Source



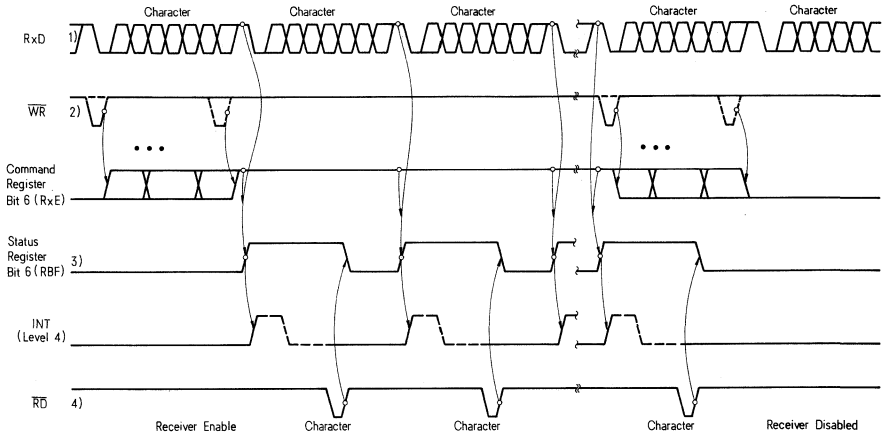
Data Bit Output on Serial Interface



Data Bit Input on Serial Interface



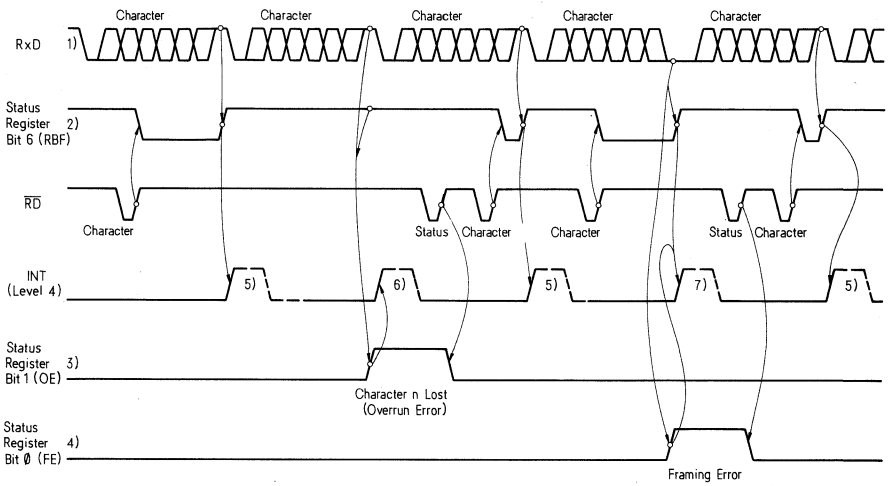
Continuous Reception of Characters on Serial Interface without Error Conditions



1) Character format for this example: 6 data bits with parity bit and one stop bit.
2) Set or reset bit 6 of command register 3 (enable receiver)
3) Receiver buffer loaded
4) Read receiver buffer register
5) Receiver is active even though no data is sent or status bit set.

No status bits are altered when $\overline{RD}$ is active.

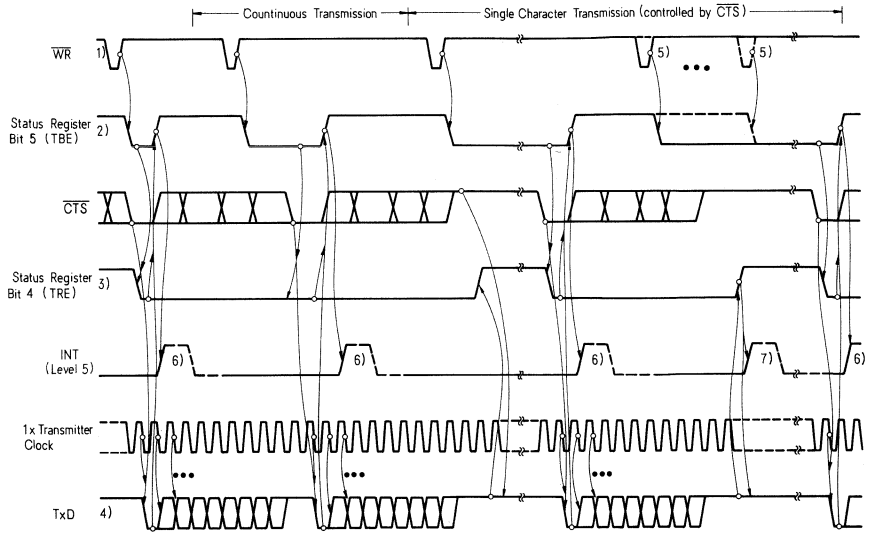
Error Conditions during Reception of Characters on the Serial Interface



1) Character format for this example: 6 data bits without parity and one stop bit
2) Receiver buffer register loaded
3) Overrun error
4) Framing error
5) Interrupt from receiver buffer register loading
6) Interrupt from overrun error
7) Interrupt from framing error and loading receiver buffer register

No status bits are altered when $\overline{RD}$ is active.

Transmission of Characters on Serial Interface

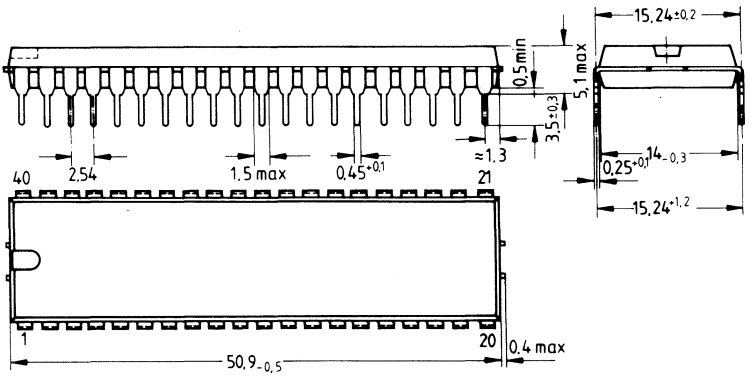


1) Load transmitter buffer register
2) Transmitter buffer register is empty
3) Transmitter register is empty
4) Character format for this example: 7 data bits with parity bit and 2 stop bits
5) Loading of transmitter buffer register must be completed before $\overline{CTS}$ goes low
6) Interrupt due to transmitter buffer register empty
7) Interrupt due to transmitter register empty

No status bits are altered when $\overline{RD}$ is active.

Package Outlines

40-Pin Dual-In-Line Plastic Package (P-DIP-40)



Ordering Information

Type	Ordering code	Description
		Programmable Multifunction UART (MUART)
SAB 8256A–P	Q 67120-Y43	3 MHz system clock (plastic package)
SAB 8256A–2–P	Q 67120-Y59	5 MHz system clock (plastic package)

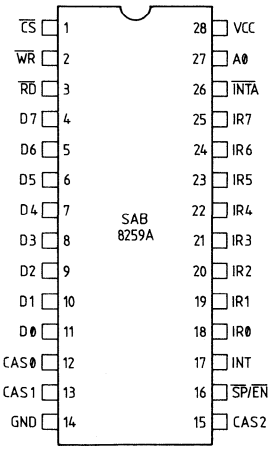
SIEMENS

Preliminary

SAB 8259A, SAB 8259A-2 Programmable Interrupt Controller

- Compatible with SAB 8086/88, SAB 80186/188 and SAB 80286 processor families
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Single +5 V supply (no clocks)
- 28-pin dual-in-line package

Pin Configuration



Pin Names

D7-D0	Data Bus (Bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS2-CAS0	Cascade Lines
$\overline{SP/EN}$	Slave Programm/Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0-IR7	Interrupt Request Inputs

The SAB 8259A programmable interrupt controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without requiring additional circuitry. The SAB 8259A is fabricated in +5 V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 28-pin DIP. The circuitry is static, requiring no clock input.

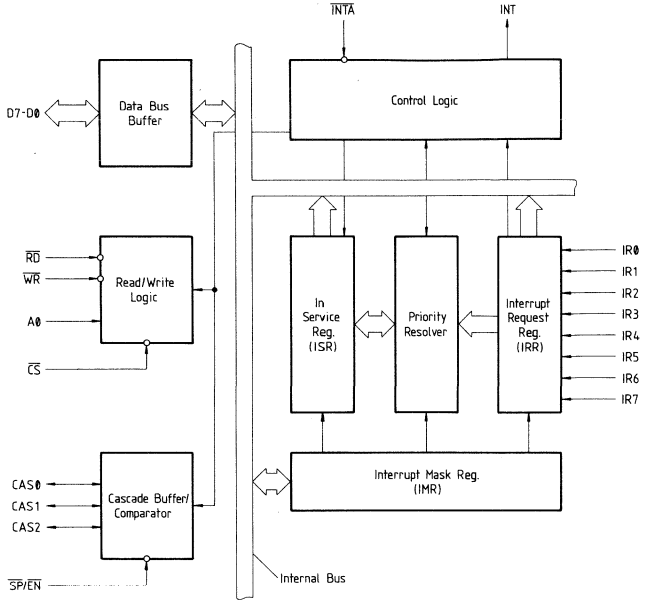
The SAB 8259A is designed to minimize the software and real-time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

Pin Definitions and Functions

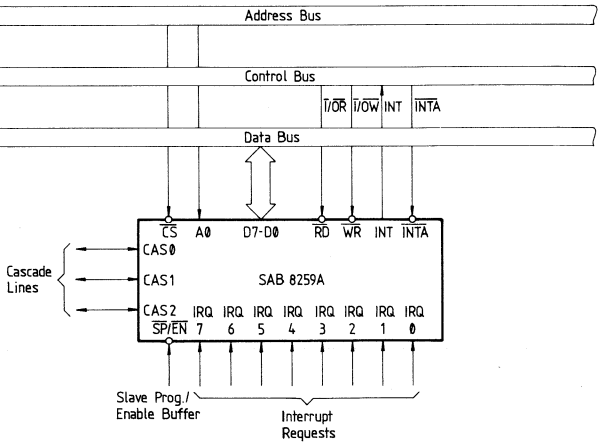
Symbol	Pin	Input (I) Output (O)	Function
$\overline{CS}$	1	I	CHIP SELECT A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the SAB 8259A. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	$\overline{WRITE}$ A low on this pin when $\overline{CS}$ is low, enables the SAB 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	$\overline{READ}$ A low on this pin when $\overline{CS}$ is low, enables the SAB 8259A to release status onto the data bus for the CPU.
D7-D0	4-11	I/O	BIDIRECTIONAL DATA BUS Control, status and interrupt vector information is transferred via this bus.
CAS0-CAS1	12, 13, 15	I/O	CASCADE LINES The CAS lines form a private SAB 8259A bus to control a multiple SAB 8259A structure. These pins are outputs for a master SAB 8259A and inputs for a slave SAB 8259A.
$\overline{SP/EN}$	16	I/O	$\overline{SLAVE\ PROGRAM/ENABLE\ BUFFER}$ This is a dual function pin. When in buffered mode it can be used as an output to control buffer transceivers (EN). When not in buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	INTERRUPT [1] This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR0-IR7	18-25	I	INTERRUPT REQUESTS Asynchronous inputs. An interrupt request can be generated by raising an IR input (low to high) and holding it high until it is acknowledged (edge triggered mode), or just by a high level on an IR input (level triggered mode).
$\overline{INTA}$	26	I	$\overline{INTERRUPT\ ACKNOWLEDGE}$ This pin is used to enable SAB 8259A interrupt-vector data onto the data bus. This is done by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	A0 ADDRESS LINE This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. It is used by the SAB 8259A to destinguish between various command words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for SAB 8086/80186/80286).
VCC	28	I	POWER SUPPLY (+5 V)
GND	14	I	GROUND (0 V)

[1] An active low signal on $\overline{WR}$ during an INT high signal may force INT to low.

Functional Block Diagram



Interface to Standard System Bus



Functional Description

General

The SAB 8259A is a device specifically designed for use in real-time, interrupt-driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other SAB 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral.
A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the SAB 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during an $\overline{\text{INTA}}$ pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The VOH level on this line is designed to be fully compatible with the SAB 8080A/8085A/8086/8088/80186/80188/80286.

$\overline{\text{INTA}}$ (Interrupt Acknowledge)

$\overline{\text{INTA}}$ pulses will cause the SAB 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the SAB 8259A.

Data Bus Buffer

This tristate, bidirectional 8-bit buffer is used to interface the SAB 8259A to the system data bus. Control words and status information are transferred through the data bus buffer.

Read/Write Control Logic

The function of this block is to accept output commands from CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the SAB 8259A to be transferred onto the data bus.

$\overline{\text{CS}}$ (Chip Select)

A low on this input enables the SAB 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{\text{WR}}$ (Write)

A low on this input enables the CPU to write control words (ICWs and OCWs) to the SAB 8259A.

$\overline{\text{RD}}$ (Read)

A low on this input enables the SAB 8259A to send the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the data bus.

A0

This input signal is used in conjunction with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all SAB 8259As used in the system. The associated three I/O pins (CAS0-2) are outputs when the SAB 8259A is used as a master and are inputs when the SAB 8259A is used as a slave. As a master, the SAB 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the data bus during the next one or two consecutive $\overline{\text{INTA}}$ pulses.

Interrupt Sequence

The powerful features of the SAB 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an SAB 8080/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The SAB 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The SAB 8259A will also release a CALL instruction code (11001101) onto the 8-bit data bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the SAB 8259A from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the SAB 8259A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte CALL instruction released by the SAB 8259A. In the AEOI[1] mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an SAB 8086/8088/80186/80188/80286 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The SAB 8259A does not drive the data bus during this cycle.
5. The CPU will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the SAB 8259A releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request was too short in duration) the SAB 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

[1] Automatic End of Interrupt

Absolute Maximum Ratings [1)]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to 7 V
Power dissipation	1 W

DC Characteristics

TA = 0 to 70°C; VCC = 5 V ±10%

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
VIL	Input low voltage	−0.5	0.8	V	–
VIH	Input high voltage	2.0	VCC +0.5 V		
VOL	Output low voltage	–	0.45		IOL = 2.2 mA
VOH	Output high voltage	2.4	–		IOH = −400 µA
VOH (INT)	Interrupt output high voltage	3.5			IOH = −100 µA
		2.4			IOH = −400 µA
ILI	Input load current	–	±10	µA	0V ≤ VIN ≤ VCC
ILOL	Output leakage current				0.45 V ≤ VOUT ≤ VCC
ICC	VCC supply current		85	mA	All outputs open
ILIR	IR input load current		−300	µA	VIN = 0V
			10		VIN = VCC

Capacitance

TA = 25°C; VCC = GND = 0V

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
CIN	Input capacitance	–	10	pF	fC = 1 MHz
CI/O	I/O capacitance		20		Unmeasured pins returned to GND

[1)] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

TA = 0 to 70°C; VCC = 5 V ±10%

Timing Requirements

Symbol	Parameter	Limit values				Unit	Test conditions
		SAB 8259A		SAB 8259A-2			
		min.	max.	min.	max.		
TAHRL	A0/$\overline{CS}$ setup to $\overline{RD}$/$\overline{INTA}\downarrow$	0	–	0	–	ns	–
TRHAX	A0/$\overline{CS}$ hold after $\overline{RD}$/$\overline{INTA}\uparrow$						
TRLRH	$\overline{RD}$ pulse width	235		160			
TAHWL	A0/$\overline{CS}$ setup to $\overline{WR}\downarrow$	0		0			
TWHAX	A0/$\overline{CS}$ hold after $\overline{WR}\uparrow$						
TWLWH	$\overline{WR}$ pulse width	290		190			
TDVWH	Data setup to $\overline{WR}\uparrow$	240		160			
TWHDX	Data hold after $\overline{WR}\uparrow$	0		0			
TJLJH	Interrupt request width (low)	100		100			[1]
TCVIAL	Cascade setup to second or third $\overline{INTA}\downarrow$ (slave only)	55		40			–
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		160			
TWHRL	End of $\overline{WR}$ to next $\overline{WR}$	190		190			
TCHCL [2]	End of command to next command (not same command type)	210		210			
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	500		500			

Timing Responses

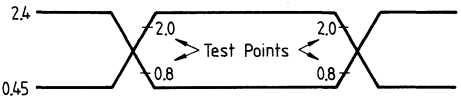
Symbol	Parameter	Limit values				Unit	Test conditions
		SAB 8259A		SAB 8259A-2			
		min.	max.	min.	max.		
TRLDV	Data valid from $\overline{RD}$/$\overline{INTA}\downarrow$	–	200	–	120	ns	C of data bus:
TRHDZ	Data float after $\overline{RD}$/$\overline{INTA}\uparrow$	10	100	10	85		max. test C =
TJHIH	Interrupt output delay	–	350	–	300		100 pF
TIALCV	Cascade valid from first $\overline{INTA}\downarrow$ (master only)		565		360		min. test C = 15 pF
TRLEL	Enable active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$		125		100		CINT = 100 pF
TRHEH	Enable inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$		150		150		C cascade = 100 pF
TAHDV	Data valid from stable address		200		200		
TCVDV	Cascade valid to valid data		300				

[1]) This is the low time required to clear the input latch in the edge-triggered mode.

[2]) Worst-case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns.

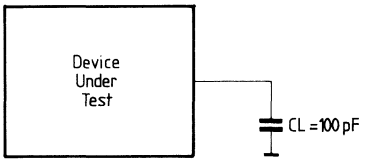
AC Testing Input, Output Waveform

Input/Output



AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

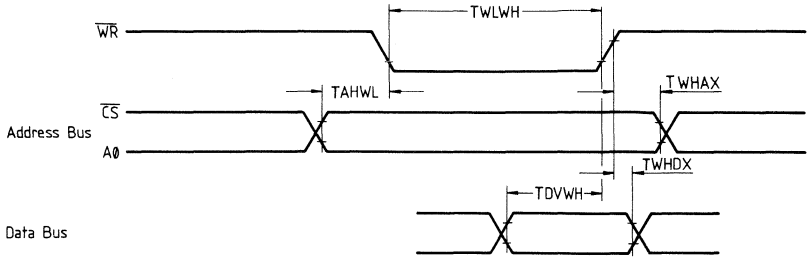
AC Testing Load Circuit



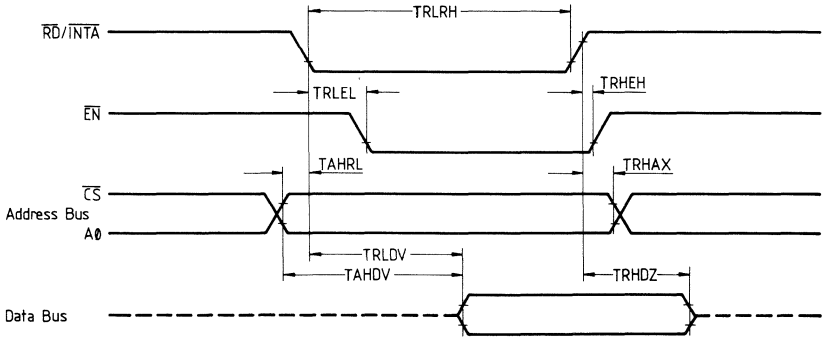
CL includes jig capacitance

Waveforms

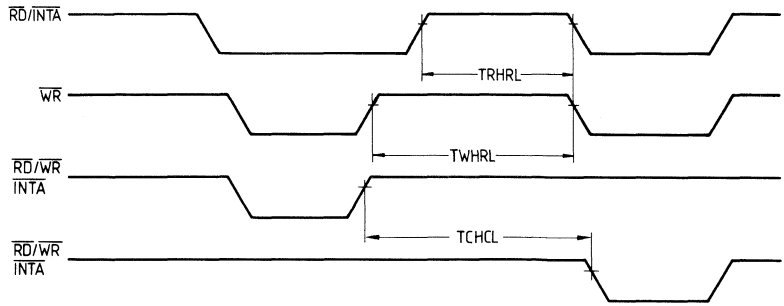
Write



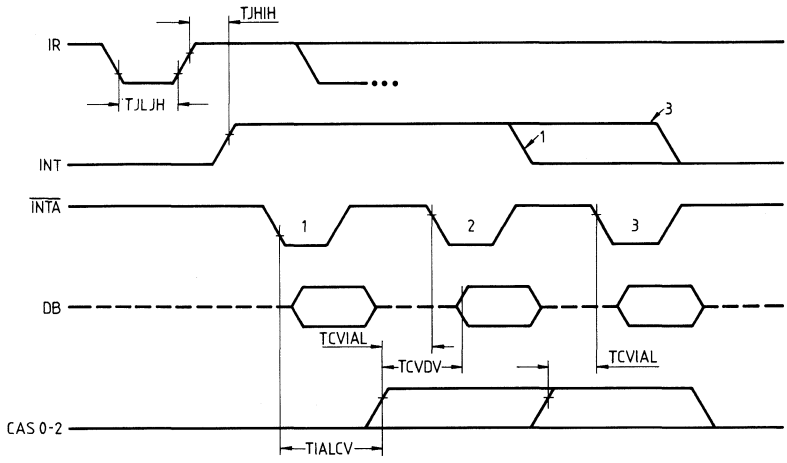
Read/INTA



Other Timings



$\overline{\text{INTA}}$ Sequence



Notes: Interrupt output must remain high at least until leading edge of first $\overline{\text{INTA}}$.
[1]) Cycle 1 in SAB 8086/88 systems, the data bus is not active.
[2]) Cycle 2.
[3]) Cycle 3 in SAB 8085 systems only.

Ordering Information

Type	Description	Ordering Code
SAB 8259A	Programmable interrupt controller, 5 MHz, plastic package	Q67120-P46
SAB 8259A-2P	Programmable interrupt controller, 8 MHz, plastic package	Q67120-P81

SIEMENS

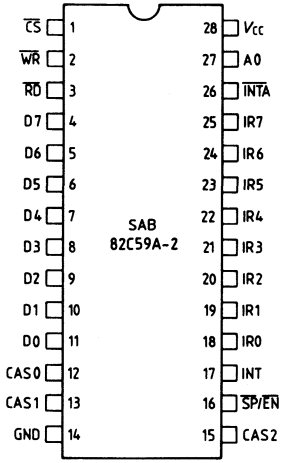
CMOS Programmable Interrupt Controller

SAB 82C59A-2

Preliminary

- Compatible with NMOS and CMOS 8085A, SAB 8086/8088, SAB 80186/80188, SAB 80286 and 80386 processor families
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Fully static design
- Low standby power dissipation
- Compatible with the industry standard NMOS SAB 8259A-2

Pin Configuration



Pin Names

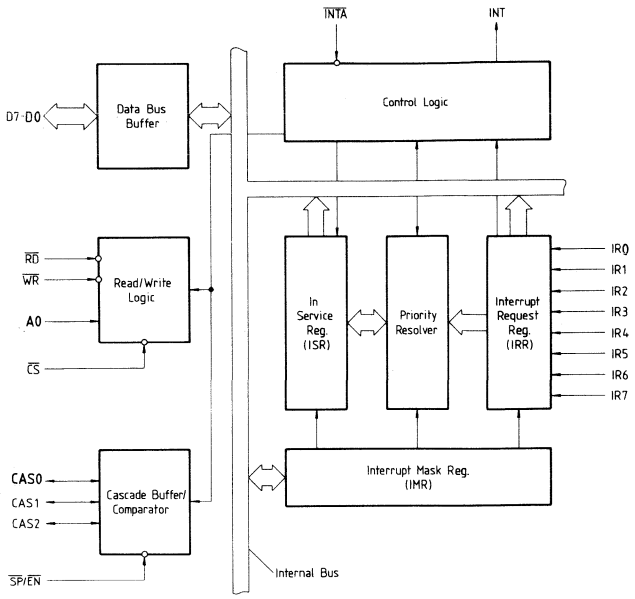
D7-D0	Data Bus (bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS2-CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Program/Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0-IR7	Interrupt Request Inputs

The SAB 82C59A-2 Programmable Interrupt Controller is a high-performance CMOS version of the NMOS SAB 8259A-2. The SAB 82C59A-2 is fabricated in Siemens ACMOS technology and compatible with the industry standard 8259A.
The SAB 82C59A-2 handles up to 8 vectored interrupts to the CPU. It is designed to minimize the software and real-time overhead in handling multilevel priority interrupts. It offers several modes, permitting optimization for a variety of system requirements. Packaged in a 28-pin plastic dual-in-line package, the SAB 82C59A-2 as a static CMOS circuit insures low operating power.

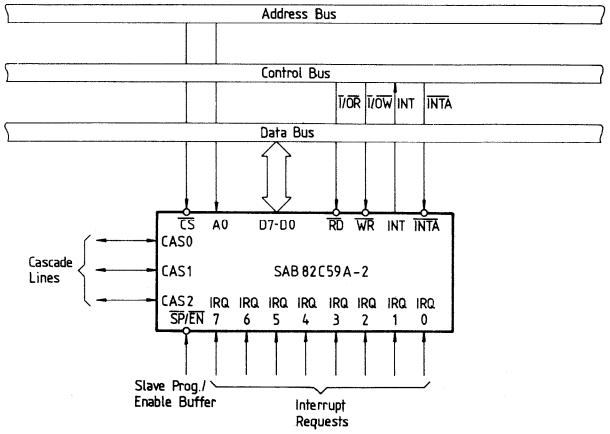
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{CS}$	1	I	$\overline{CHIP\ SELECT}$ A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the SAB 82C59A-2. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	$\overline{WRITE}$ A low on this pin, when $\overline{CS}$ is low, enables the SAB 82C59A-2 to accept command words from the CPU.
$\overline{RD}$	3	I	$\overline{READ}$ A low on this pin, when $\overline{CS}$ is low, enables the SAB 82C59A-2 to release status onto the data bus for the CPU.
D7-D0	4-11	I/O	BIDIRECTIONAL DATA BUS Control, status, and interrupt vector information is transferred via this bus.
CAS0-CAS2	12, 13, 15	I/O	CASCADE LINES The CAS lines form a private SAB 82C59A-2 bus to control a multiple SAB 82C59A-2 structure. These pins are outputs for a master SAB 82C59A-2 and inputs for a slave SAB 82C59A-2.
$\overline{SP}/\overline{EN}$	16	I/O	$\overline{SLAVE\ PROGRAM}/\overline{ENABLE\ BUFFER}$ This is a dual-function pin. When in buffered mode it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in buffered mode it is used as an input to designate a master ($\overline{SP}$ = 1) or slave ($\overline{SP}$ = 0).
INT	17	O	INTERRUPT This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU and is, therefore, connected to the CPU's interrupt pin.
IR0-IR7	18-25	I	INTERRUPT REQUESTS These are asynchronous inputs. An interrupt request can be generated by raising an IR input (low to high) and holding it high until it is acknowledged (edge-triggered mode), or just by a high level on an IR input (level-triggered mode).
$\overline{INTA}$	26	I	$\overline{INTERRUPT\ ACKNOWLEDGE}$ This pin is used to enable SAB 82C59A-2 interrupt vector data onto the data bus. This is done by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	A0 ADDRESS LINE This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. It is used by the SAB 82C59A-2 to distinguish between various command words written by the CPU and the status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for SAB 8086/80186/80286).
V_{CC}	28	–	POWER SUPPLY (+5 V)
GND	14	–	GROUND (0 V)

Functional Block Diagram



Interface to Standard System Bus



Functional Description

General

The SAB 82C59A-2 is a device specifically designed for use in real-time, interrupt-driven microcomputer systems. It manages eight levels of requests and has built-in features for expandability to other SAB 82C59A-2 devices (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the SAB 82C59A-2 can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two cascaded registers: the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during an $\overline{\text{INTA}}$ pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines. The IMR operation is based on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the SAB 8085A/8086/8088/80186/80188/80286 and 80386.

$\overline{\text{INTA}}$ (Interrupt Acknowledge)

$\overline{\text{INTA}}$ pulses will cause the SAB 82C59A-2 to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the SAB 82C59A-2.

Data Bus Buffer

This tristate, bidirectional 8-bit buffer is used to interface the SAB 82C59A-2 to the system data bus. Control words and status information are transferred through the data bus buffer.

Read/Write Control Logic

The function of this block is to accept output commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the SAB 82C59A-2 to be transferred onto the data bus.

$\overline{\text{CS}}$ (Chip Select)

A low on this input enables the SAB 82C59A-2. No reading or writing of the chip will occur unless the device has been selected.

$\overline{\text{WR}}$ (Write)

A low on this input enables the CPU to write control words (ICWs and OCWs) to the SAB 82C59A-2.

$\overline{\text{RD}}$ (Read)

A low on this input enables the SAB 82C59A-2 to send the status of the Interrupt Request Register (IRR), the In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the data bus.

A0

This input signal is used in conjunction with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals to write commands into the various command registers, as well as to read the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all SAB 82C59A-2 devices used in the system. The associated three I/O pins (CAS0-2) are outputs when the SAB 82C59A-2 is used as a master and are inputs when the SAB 82C59A-2 is used as a slave. As a master, the SAB 82C59A-2 sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the data bus during the next one or two consecutive $\overline{\text{INTA}}$ pulses.

Interrupt Sequence

The powerful features of the SAB 82C59A-2 in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

In an SAB 8085A system the events occur as follows:

1. One or more of the interrupt request lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The SAB 82C59A-2 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The SAB 82C59A-2 will also release a "call" instruction code (11001101) onto the 8-bit data bus through its D7-0 pins.
5. This "call" instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the SAB 82C59A-2 from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the SAB 82C59A-2 to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte "call" instruction released by the SAB 82C59A-2. In the AEOI (automatic end of interrupt) mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an SAB 8086/8088/80186/80188/80286 or 80386 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The SAB 82C59A-2 does not drive the data bus during this cycle.
5. The CPU will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the SAB 82C59A-2 releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request duration was too short), the SAB 82C59A-2 will issue an interrupt level 7. Both, the vectoring bytes and the CAS lines will look as if an interrupt level 7 was requested.

Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to V_{CC}+0.5 V
Supply voltage with respect to ground	−0.5 to 7.0 V
Power dissipation	1 W

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; GND = 0V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage	2.2	V_{CC} +0.5	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} −0.4	–	V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{LI}	Interrupt leakage current	–	±1	µA	0 V < V_{IN} < V_{CC}
I_{LOL}	Output leakage current	–	±10	µA	0 V < V_{OUT} < V_{CC}
I_{LIR}	IR input leakage current	–	−300 +10	µA	V_{IN}= 0 V V_{IN} = V_{CC}
I_{CC}	Operating supply current	–	5	mA	[2]
I_{CCS}	Standby supply current	–	10	µA	V_{CC} = 5.5 V, outputs unloaded, V_{IN} = V_{CC} or GND All IR inputs = V_{CC}

Capacitance

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	f_c = 1 MHz Unmeasured pins returned to GND
C_{IO}	I/O capacitance	–	20	pF	
C_{OUT}	Output capacitance	–	15	pF	

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Repeated data input with 8086-2 timings.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; GND = 0 V

Timing Requirements

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AHRL}	A0/$\overline{CS}$ setup to $\overline{RD}$/$\overline{INTA}\downarrow$	0	–	ns	–
t_{RHAX}	A0/$\overline{CS}$ hold after $\overline{RD}$/$\overline{INTA}\uparrow$	0	–	ns	–
t_{RLRH}	$\overline{RD}$ pulse width	160	–	ns	–
t_{AHWL}	A0/$\overline{CS}$ setup to $\overline{WR}\downarrow$	0	–	ns	–
t_{WHAX}	A0/$\overline{CS}$ hold after $\overline{WR}\uparrow$	0	–	ns	–
t_{WLWH}	$\overline{WR}$ pulse width	190	–	ns	–
t_{DVWH}	Data setup to $\overline{WR}\uparrow$	160	–	ns	–
t_{WHDX}	Data hold after $\overline{WR}\uparrow$	0	–	ns	–
t_{JLJH} [1]	Interrupt request width (low)	100	–	ns	–
t_{CVIAL}	Cascade setup to second or third $\overline{INTA}\downarrow$ (slave only)	40	–	ns	–
t_{RHRL}	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160	–	ns	–
t_{WHRL}	End of $\overline{WR}$ to next $\overline{WR}$	190	–	ns	–
t_{CHCL} [2]	End of command to next command (not same command type)	180	–	ns	–
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	400	–	ns	–

Timing Responses

Symbol	Parameter	Limit values		Unit	Test condition[3]
		min.	max.		
t_{RLDV}	Data valid from $\overline{RD}$/$\overline{INTA}\downarrow$	–	120	ns	1
t_{RHDZ}	Data float after $\overline{RD}$/$\overline{INTA}\uparrow$	10	85	ns	2
t_{JHIH}	Interrupt output delay	–	300	ns	1
t_{IALCV}	Cascade valid from first $\overline{INTA}\downarrow$ (master only)	–	360	ns	1
t_{RLEL}	Enable active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$	–	100	ns	1
t_{RHEH}	Enable inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$	–	150	ns	1
t_{AHDV}	Data valid from stable address	–	200	ns	1
t_{CVDV}	Cascade valid to valid data	–	200	ns	1

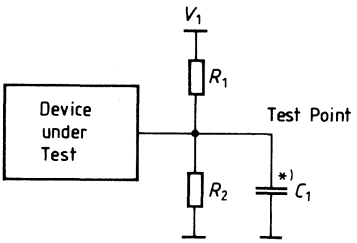
[1]) This is the low time required to clear the input latch in the edge-triggered mode.

[2]) Worst-case timing for t_{CHCL} in an actual microprocessor system is typically much greater than 400 ns.

[3]) See diagrams on next page.

AC Testing

Load Circuit

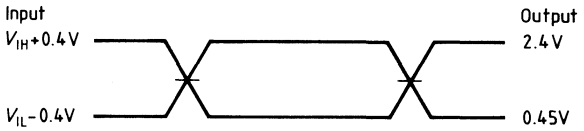


*) Includes Stray and Jig Capacitance

Test Condition Definition

Test Condition	V_1	R_1	R_2	C_1
1	1.7 V	523 Ω	Open	100 pF
2	4.5 V	1.8 kΩ	1.8 kΩ	30 pF

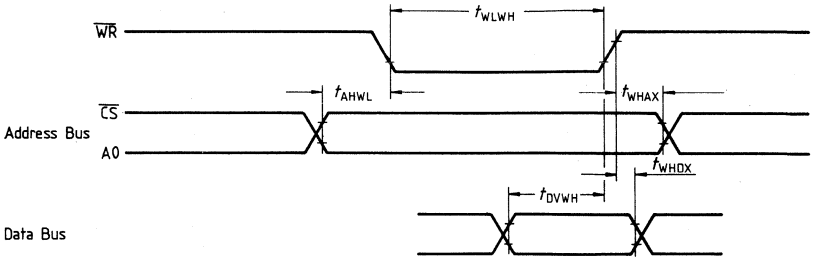
I/O Waveform



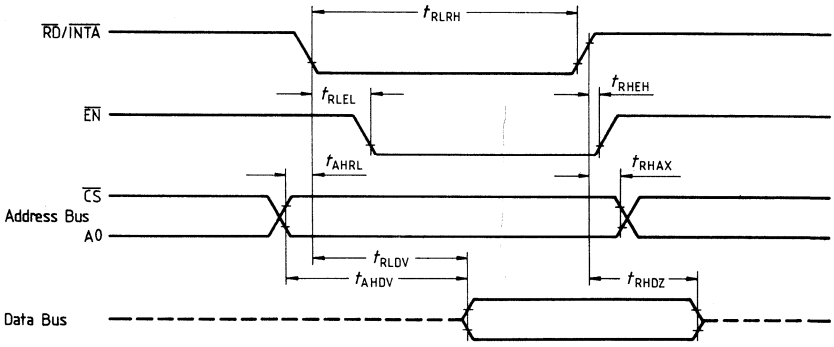
AC testing: All input signals must switch between V_{IL} −0.4 V and V_{IH} + 0.4 V. Input rise and fall times must be ≤15 ns. All timing measurements are made at 2.4 V and 0.45 V.

Waveforms

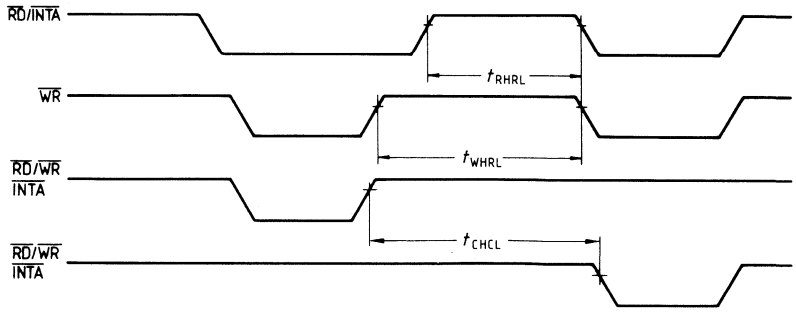
Write



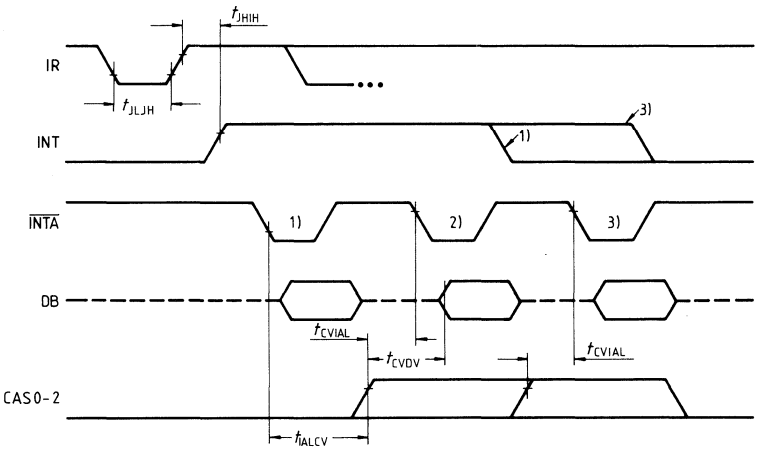
Read/INTA



Other Timings



$\overline{\text{INTA}}$ Sequence

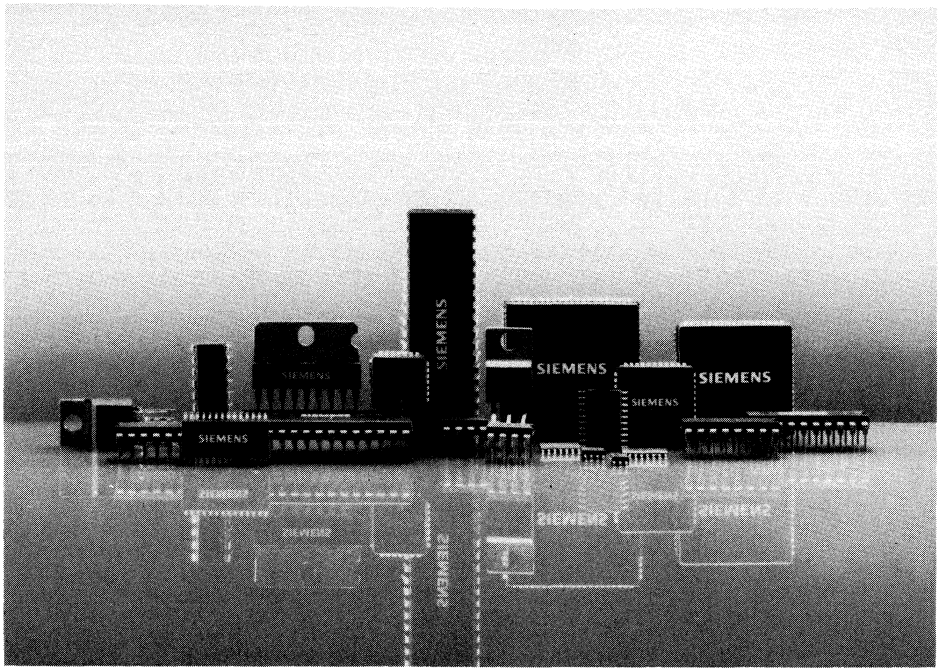


Interrupt output must remain high at least until leading edge of first $\overline{\text{INTA}}$.
[1]) Cycle 1 in SAB 8086/8088/80186/80188/80286 and 80386 systems, the data bus is not active.
[2]) Cycle 2.
[3]) Cycle 3 in SAB 8085 systems only.

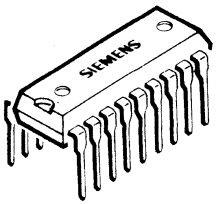
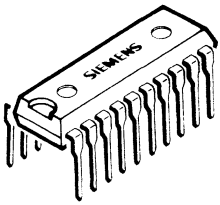
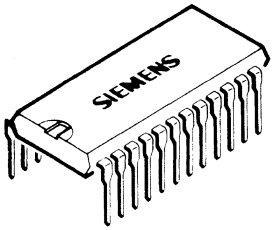
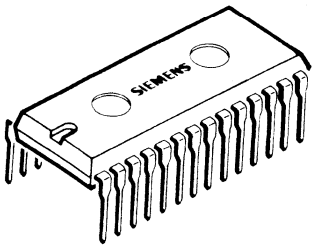
Ordering Information

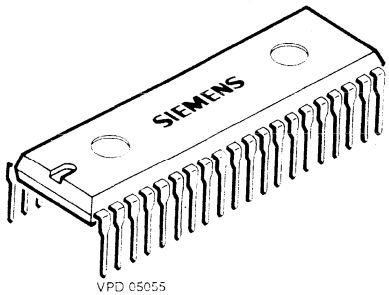
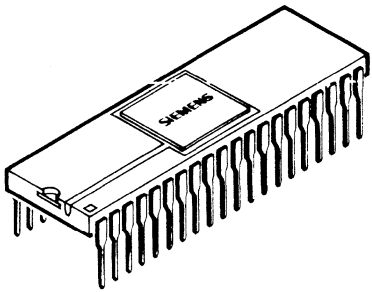
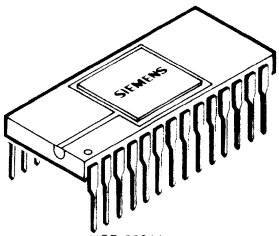
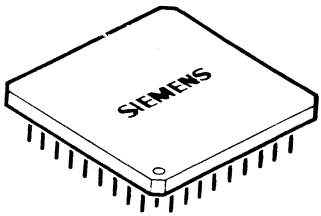
Type	Ordering code	Description
SAB 82C59A-2-P	Q67120-P238	Programmable interrupt controller, 8 MHz, plastic package

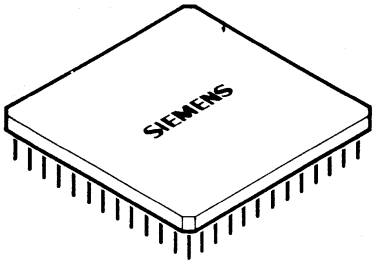
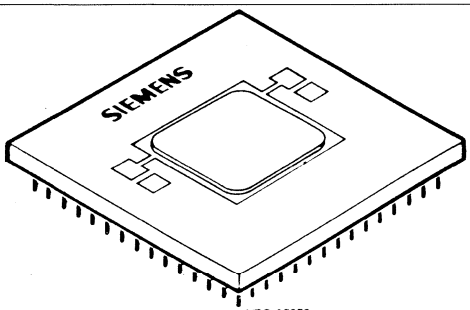
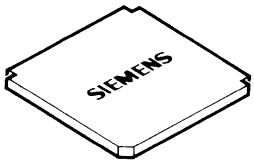
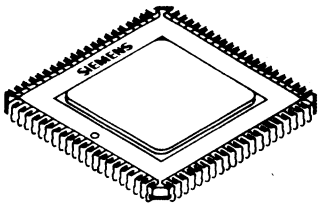
Summary of Package Outlines

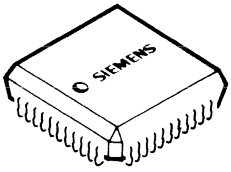
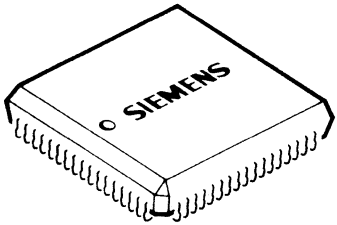
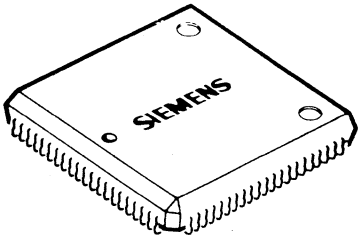
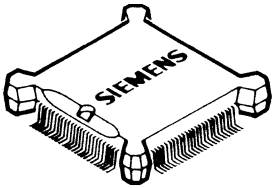


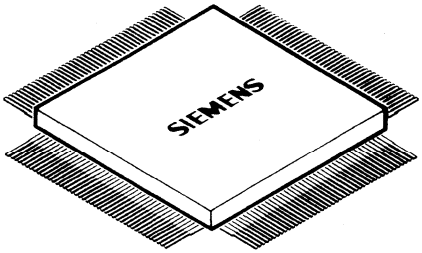
Package Outlines

 VPD 05035	**Plastic Package, P-DIP-18** (dual-in-line package) **20A18 DIN 41870 T9**
 VPD 05091	**Plastic Package, P-DIP-20** (dual-in-line package) **20A20 DIN 41870 T9**
 VRD 05034	**Plastic Package, P-DIP-24** (dual-in-line package) **20A24 DIN 41870 T10**
 VPD 05037	**Plastic Package, P-DIP-28** (dual-in-line package) **20A28 DIN 41870 T10**

 VPD 05055	**Plastic Package, P-DIP-40** (dual-in-line package) **20A40 DIN 41870 T10**
 VCD 05087	**Ceramic Package, C-DIP-40** (dual-in-line package)
 VCD 05044	**Ceramic Package,C-DIP-28** (dual-in-line package)
 VPG 05003	**Ceramic Package,C-PGA-68** (pin-grid-array)

 VPL 05002	**Ceramic Package,C-PGA-88** (pin-grid-array)
 VPG 05058	**Ceramic Package,C-PGA-145** (pin-grid-array)
 VCC 05027	**Ceramic Package,C-CC-68** (chip-carrier)
 VPL 05126	**Ceramic Package,CL-CC-84** (chip-carrier)

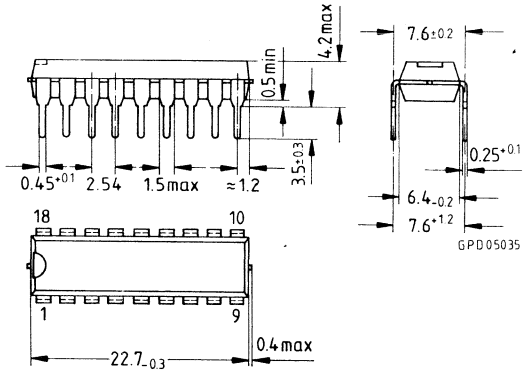
 VPL 05102	**Plastic Package, PL-CC-44** (chip-carrier) – **SMD**
 VPL 05099	**Plastic Package, PL-CC-68** (chip-carrier) – **SMD**
 VPL 05029	**Plastic Package, PL-CC-84** (chip-carrier) – **SMD**
 VPQ 05032	**Plastic Package, P-QFP-100** (Quad-Flat-Pack) **-SMD**



VPQ 05048

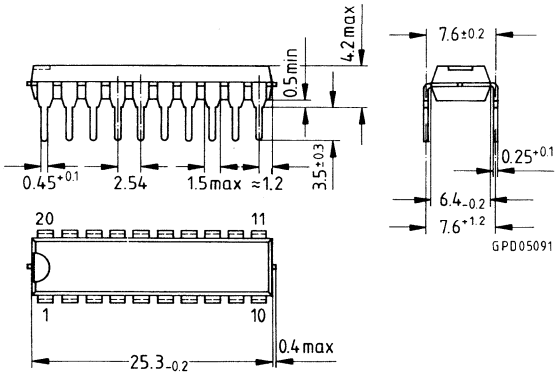
Ceramic Package,C-QFP-172
(Quad-Flat-Pack)

Plastic Package, P-DIP-18
(dual-in-line package)
20A18 DIN 41870 T9



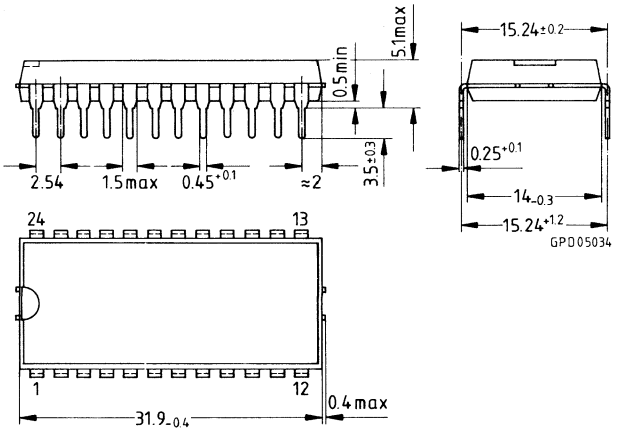
Dimensions in mm

Plastic Package, P-DIP-20
(dual-in-line package)
20A20 DIN 41870 T9



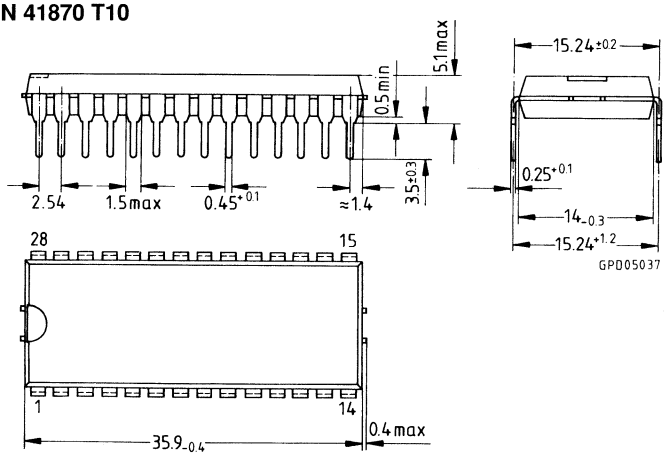
Dimensions in mm

Plastic Package, P-DIP-24
(dual-in-line package)
20A24 DIN 41870 T10



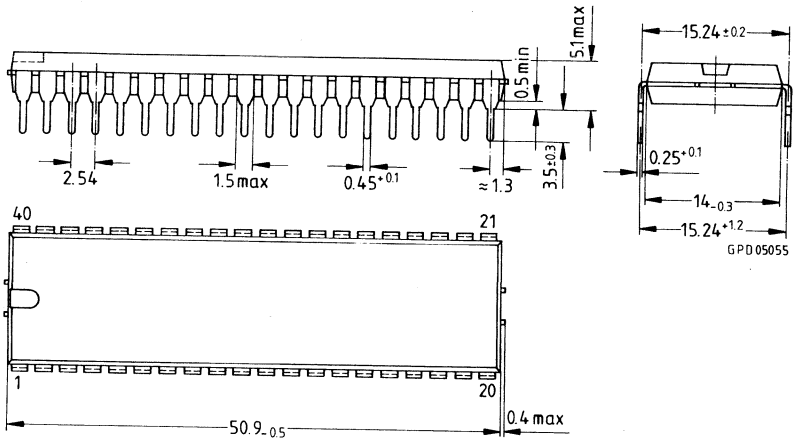
Dimensions in mm

Plastic Package, P-DIP-28
(dual-in-line package)
20A28 DIN 41870 T10



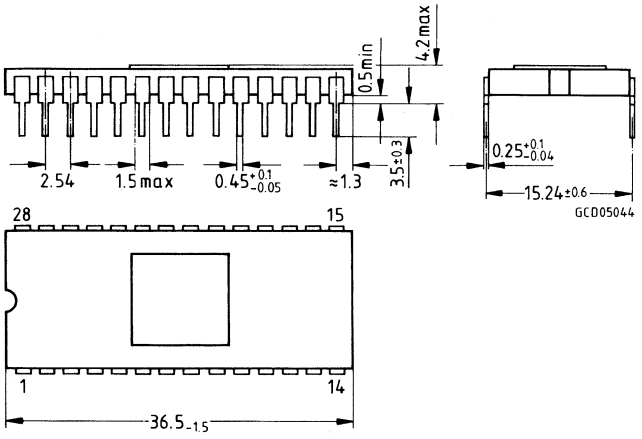
Dimensions in mm

Plastic Package, P-DIP-40
(dual-in-line package)
20A40 DIN 41870 T10



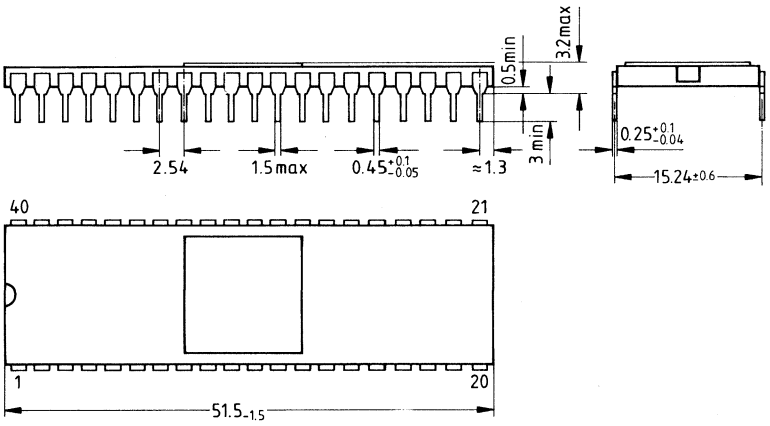
Dimensions in mm

Plastic Package, C-DIP-28
(dual-in-line package)



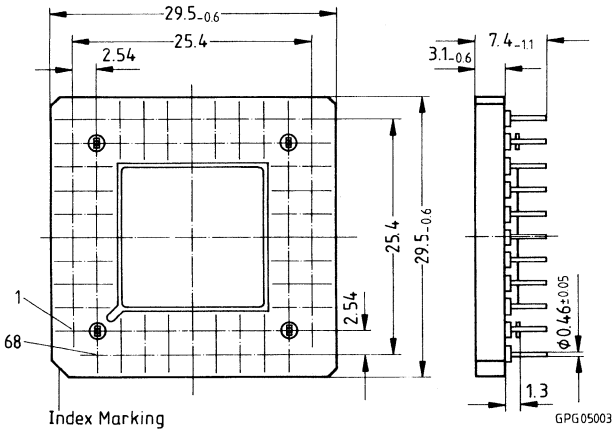
Dimensions in mm

Ceramic Package, C-DIP-40
(dual-in-line package)



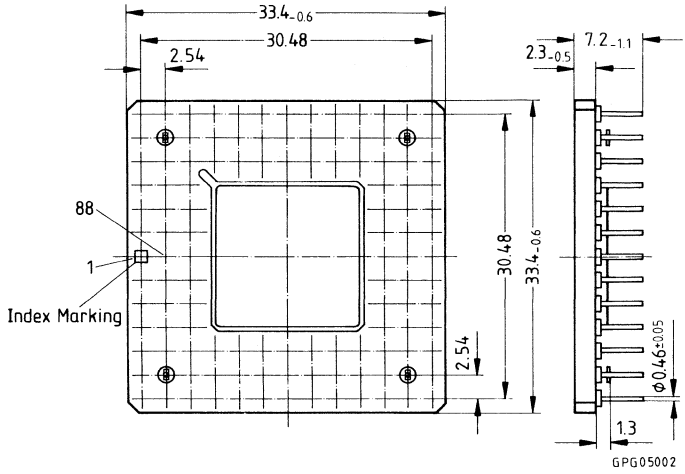
Dimensions in mm

Ceramic Package, C-PGA-68
(pin-grid-array)



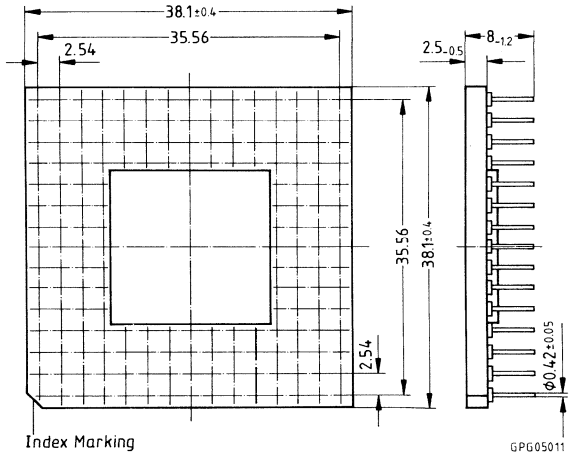
Dimensions in mm

Ceramic Package, C-PGA-88
(pin-grid-array)



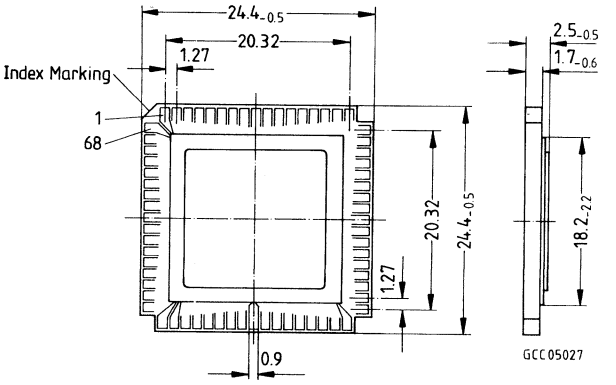
Dimensions in mm

Ceramic Package, C-PGA-145
(pin-grid-array)



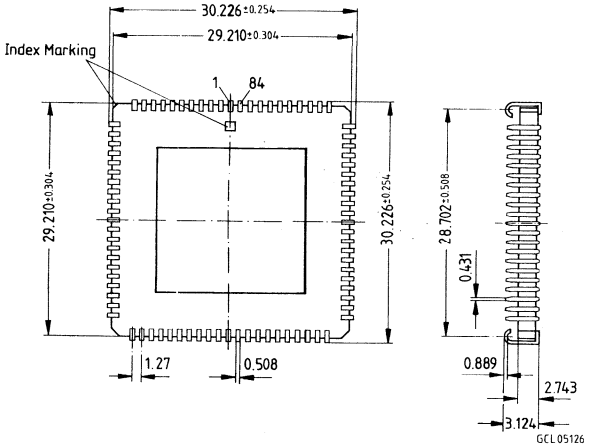
Dimensions in mm

Ceramic Package, C-CC-68
(chip-carrier)



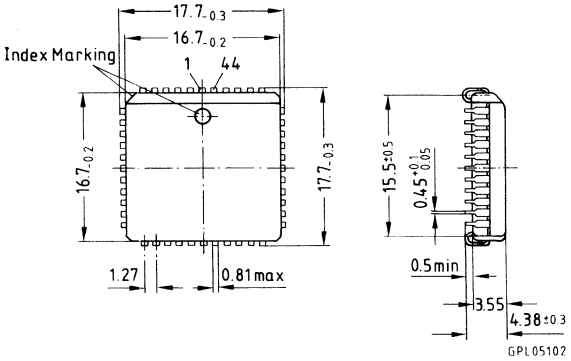
Dimensions in mm

Ceramic Package, CL-CC-84
(chip-carrier)



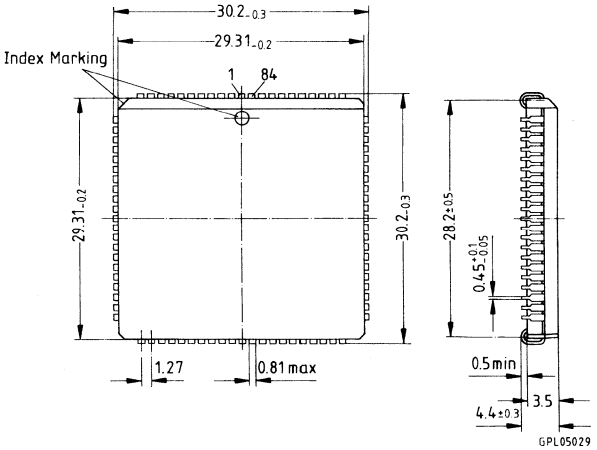
Dimensions in mm

Plastic Package, PL-CC-44
(chip-carrier) – **SMD**



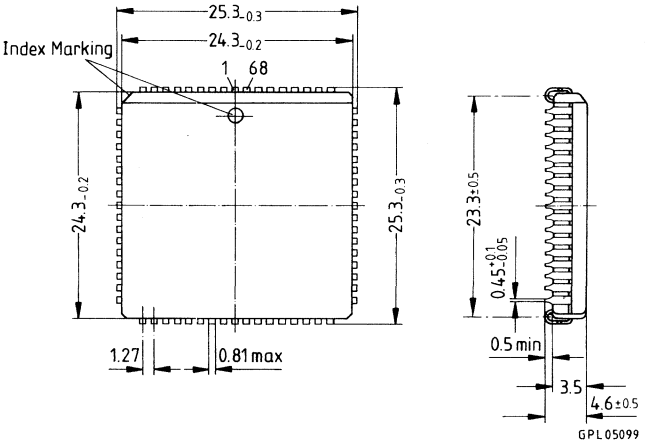
Dimensions in mm

Plastic Package, PL-CC-84
(chip-carrier) – **SMD**



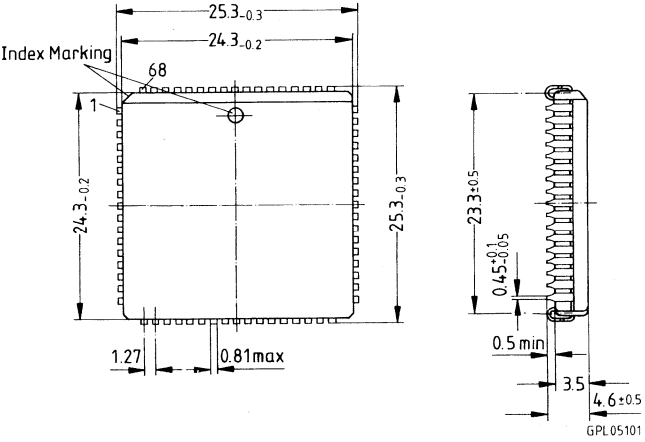
Dimensions in mm

Plastic Package, PL-CC-68
(chip-carrier) – **SMD**



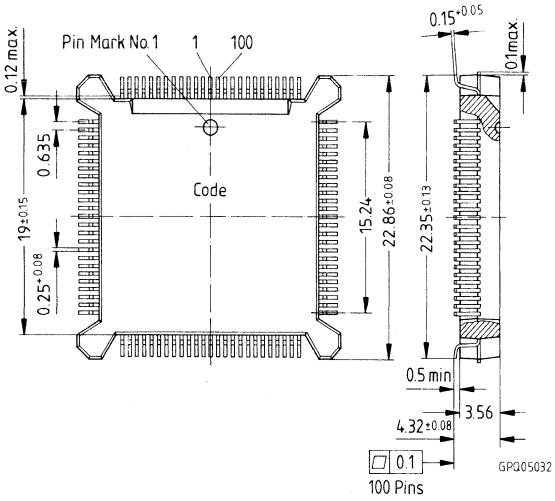
Dimensions in mm

Plastic Package, PL-CC-68
(chip-carrier) – **SMD**



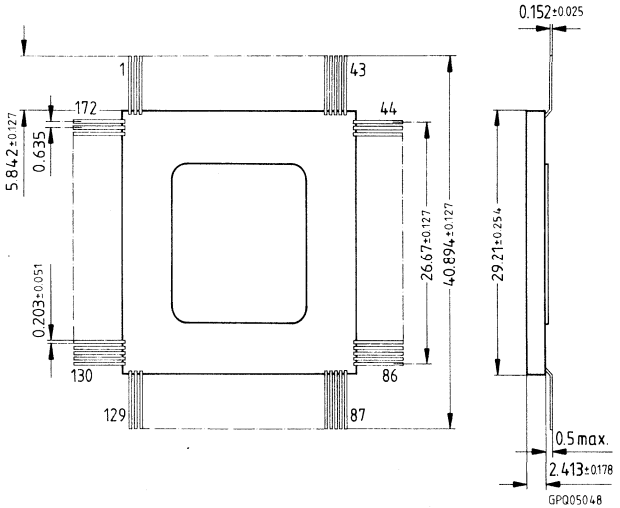
Dimensions in mm

Plastic Package, P-QFP -100
(Quad-Flat-Pack) **- SMD**



Dimensions in mm

Ceramic Package, C-QFP -172
(Quad-Flat-Pack)



Dimensions in mm

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Literaturhinweis
Information on Literature

Titel/Title	Bestell-Nr./Ordering No.	DM
Datenkataloge / Data Catalogs		
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Microprocessors and Support Components	B158-B6256-X-X-7600	20,-
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SAB 80C517/80C537, CMOS, 8-bit Microcontroller	B258-B6075-X-X-7600	15,-
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Addendum to User's Manual SAB 80C166/83C166	B158-H6345-X-X-7600	–
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Titel/Title	Bestell-Nr./Ordering No.	DM
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Published by Semiconductor Group

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Ordering No. B158-B6255-X-X-7600
Printed in Germany
DB 109010.